

$V_{SM} = 4200 \text{ V}$

$I_{TAVM} = 1920 \text{ A}$

$I_{TRMS} = 3020 \text{ A}$

$I_{TSM} = 32000 \text{ A}$

$V_{T0} = 0.96 \text{ V}$

$r_T = 0.285 \text{ m}\Omega$

Bi-Directional Control Thyristor

5STB 18N4200

Doc. No. 5SYA1040-03 Sep. 01

- Two thyristors integrated into one wafer
- Patented free-floating silicon technology
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate.

The electrical and thermal data are valid for one thyristor half of the device.

Blocking

Part Number	5STB 18N4200	5STB 18N4000	5STB 18N3600	Conditions
V_{SM}	4200 V	4000 V	3600 V	$f = 5 \text{ Hz}, t_p = 10\text{ms}$
V_{RM}	4200 V	4000 V	3600 V	$f = 50 \text{ Hz}, t_p = 10\text{ms}$
I_{SM}	$\leq 400 \text{ mA}$			V_{SM}
I_{RM}	$\leq 400 \text{ mA}$			V_{RM}
dV/dt_{crit}	1000 V/ μs			@ Exp. to $0.67 \times V_{SM}$
$T_j = 125^\circ\text{C}$				

V_{RM} is equal to V_{SM} up to $T_j = 110^\circ\text{C}$

Mechanical data

F_M	Mounting force	nom.	90 kN
		min.	81 kN
		max.	108 kN
a	Acceleration		
	Device unclamped		50 m/s ²
	Device clamped		100 m/s ²
m	Weight		2.9 kg
D_S	Surface creepage distance		53 mm
D_a	Air strike distance		22 mm

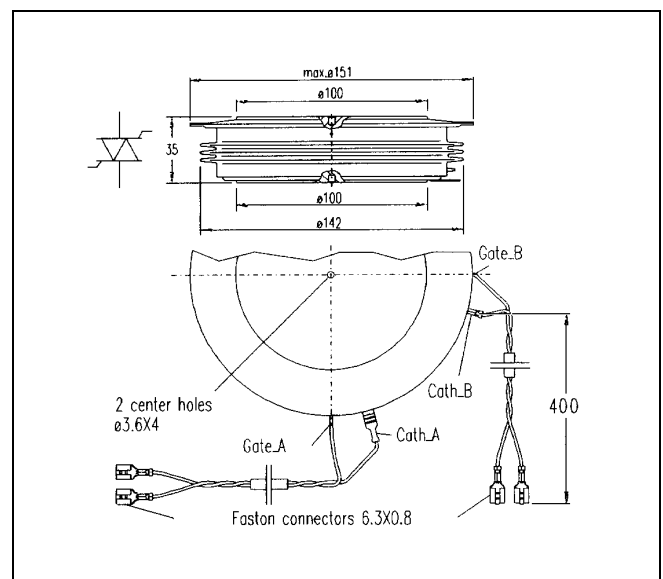


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On-state

I_{TAVM}	Max. average on-state	1920 A	Half sine wave, $T_C = 70^\circ\text{C}$		
I_{TRMS}	Max. RMS on-state current	3020 A			
I_{TSM}	Max. peak non-repetitive surge current	32000 A	$t_p =$	10 ms	$T_j = 125^\circ\text{C}$ After surge: $V_D = V_R = 0\text{V}$
		35000 A	$t_p =$	8.3 ms	
I^2t	Limiting load integral	5120 kA^2s	$t_p =$	10 ms	
		5000 kA^2s	$t_p =$	8.3 ms	
V_T	On-state voltage	1.53 V	$I_T =$	2000 A	$T_j = 125^\circ\text{C}$
V_{T0}	Threshold voltage	0.96 V	$I_T =$	1000 - 3000 A	
r_T	Slope resistance	0.285 $\text{m}\Omega$			
I_H	Holding current	50-250 mA	$T_j = 25^\circ\text{C}$		
		25-150 mA	$T_j = 125^\circ\text{C}$		
I_L	Latching current	100-500 mA	$T_j = 25^\circ\text{C}$		
		50-300 mA	$T_j = 125^\circ\text{C}$		

Switching

di/dt_{crit}	Critical rate of rise of on-state current	250 $\text{A}/\mu\text{s}$	Cont. $f = 50\text{ Hz}$	$V_D \leq 0.67 \cdot V_{DRM}$, $T_j = 125^\circ\text{C}$ $I_{TRM} = 3000\text{ A}$ $I_{FG} = 2\text{ A}$, $t_r = 0.5\ \mu\text{s}$
		500 $\text{A}/\mu\text{s}$	60 sec. $f = 50\text{ Hz}$	
t_d	Delay time	$\leq 3.0\ \mu\text{s}$	$V_D = 0.4 \cdot V_{DRM}$	$I_{FG} = 2\text{ A}$, $t_r = 0.5\ \mu\text{s}$
t_q	Turn-off time	$\leq 550\ \mu\text{s}$	$V_D \leq 0.67 \cdot V_{DRM}$ $dv_D/dt = 20\text{V}/\mu\text{s}$	$I_{TRM} = 3000\text{ A}$, $T_j = 125^\circ\text{C}$ $V_R > 200\text{ V}$, $di_T/dt = -1.5\ \text{A}/\mu\text{s}$
Q_{rr}	Recovery charge	min	2100 μAs	
		max	3200 μAs	

Triggering

V_{GT}	Gate trigger voltage	$\leq 2.6\text{ V}$	$T_j = 25^\circ\text{C}$
I_{GT}	Gate trigger current	$\leq 400\text{ mA}$	$T_j = 25^\circ\text{C}$
V_{GD}	Gate non-trigger voltage	$\geq 0.3\text{ V}$	$V_D = 0.4 \cdot V_{RM}$ $T_j = 125^\circ\text{C}$
I_{GD}	Gate non-trigger current	$\geq 10\text{ mA}$	$V_D = 0.4 \cdot V_{RM}$ $T_j = 125^\circ\text{C}$
V_{FGM}	Peak forward gate voltage	12 V	
I_{FGM}	Peak forward gate current	10 A	
V_{RGM}	Peak reverse gate voltage	10 V	
P_G	Maximum gate power loss	3 W	

Thermal

T_j	Operating junction temperature range	-40...125 °C	
T_{stg}	Storage temperature range	-40...150 °C	
R_{thJC}	Thermal resistance junction to case	22.8 K/kW	
		22.8 K/kW	Cathode side cooled
		11.4 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	4 K/kW	Single side cooled
		2 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/kW)	6.77	2.51	1.34	0.78
τ_i (s)	0.8651	0.1558	0.0212	0.0075

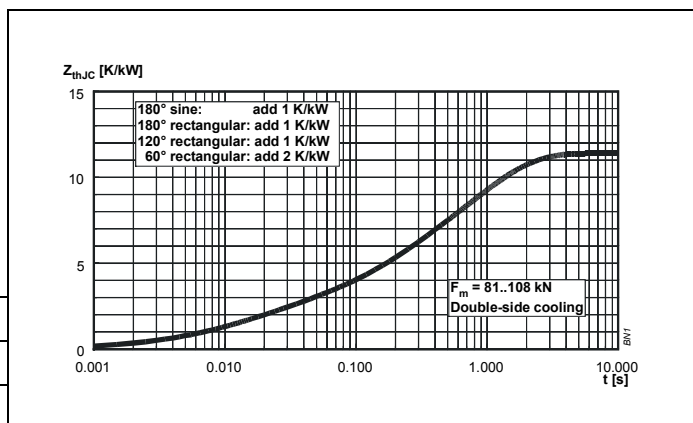


Fig. 1 Transient thermal impedance junction to case.

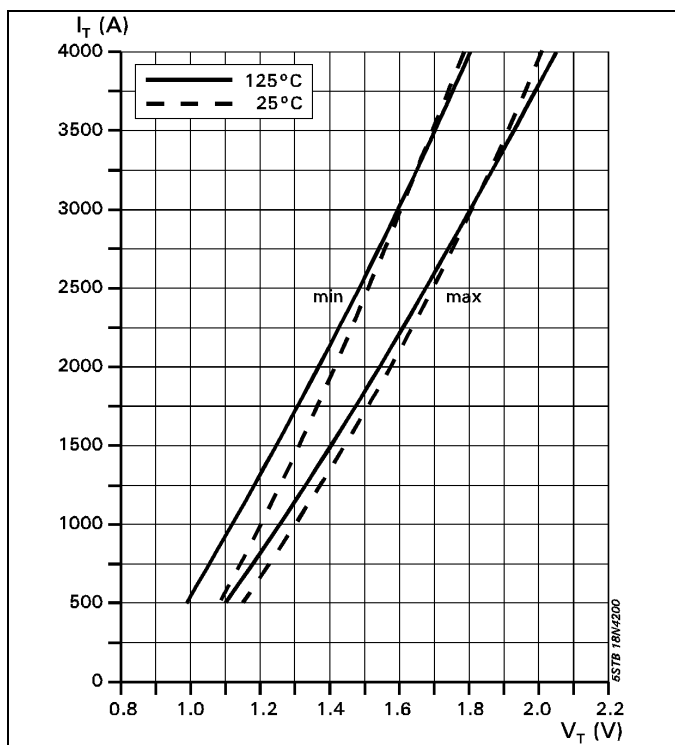


Fig. 2 On-state characteristics.

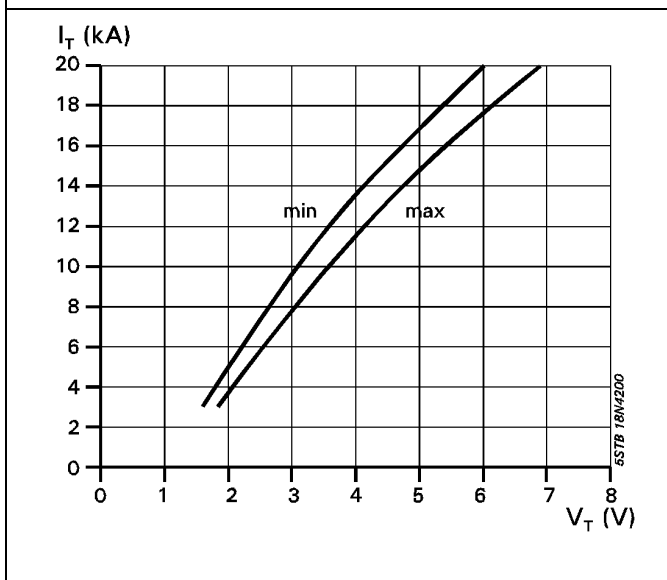


Fig. 3 On-state characteristics.

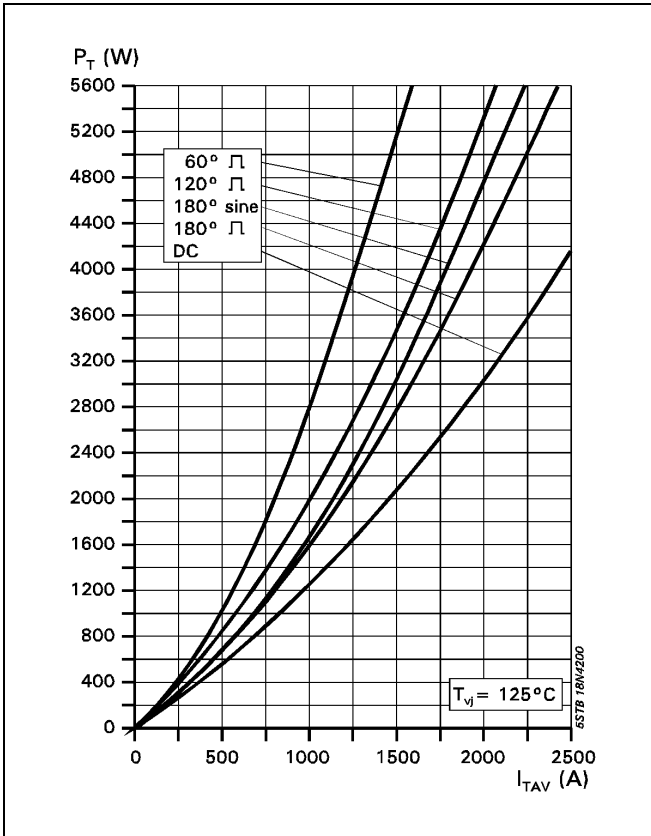


Fig. 4 On-state power dissipation vs. mean on-state current. Turn - on losses excluded.

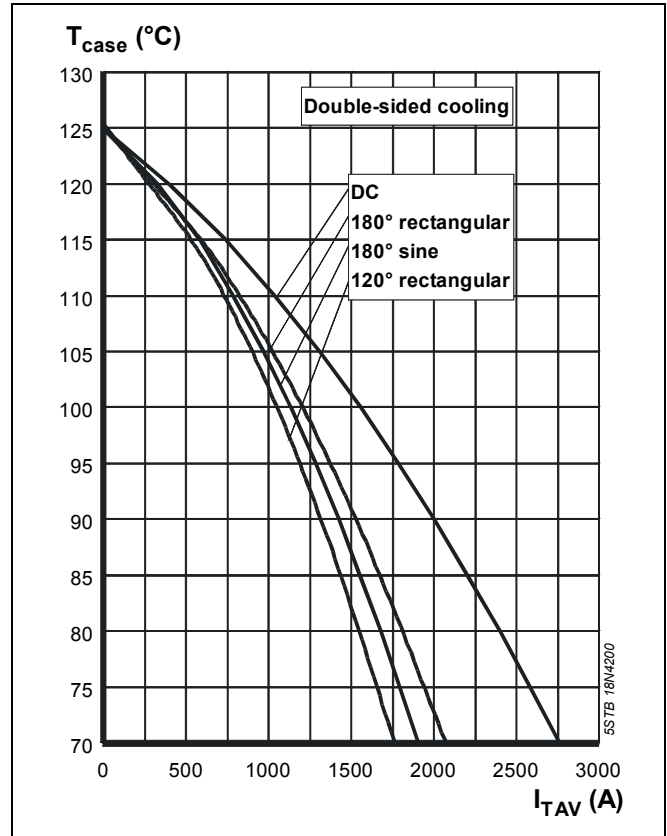


Fig. 5 Max. permissible case temperature vs. mean on-state current.

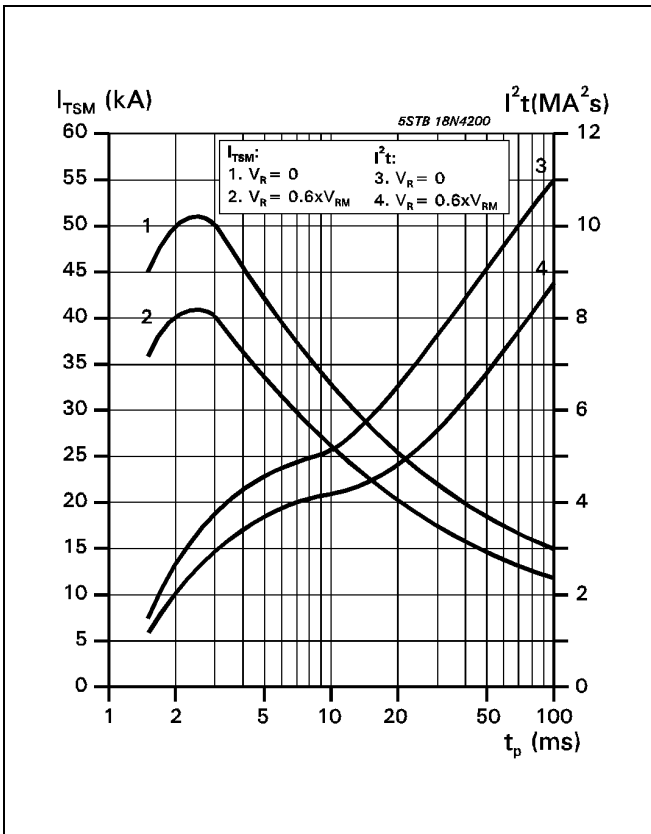


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

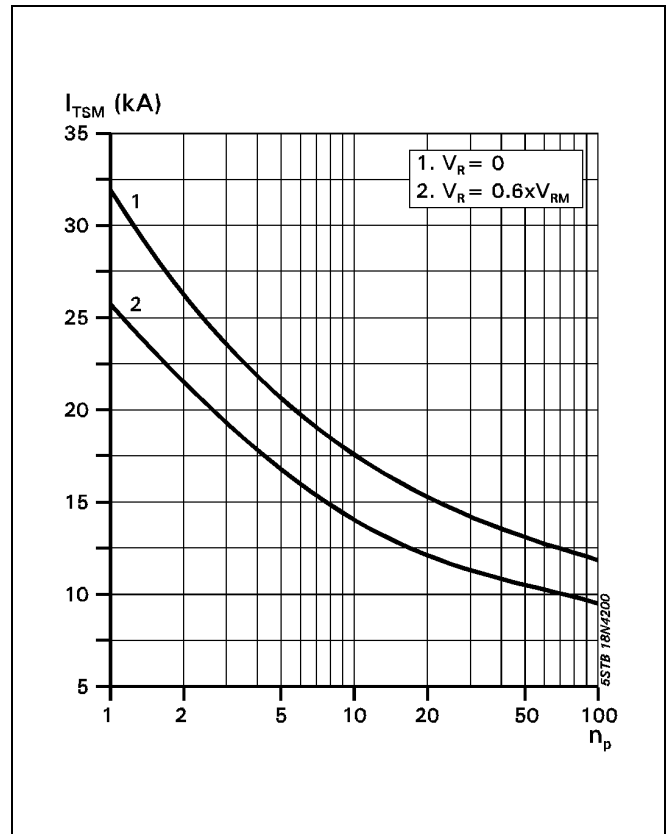


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

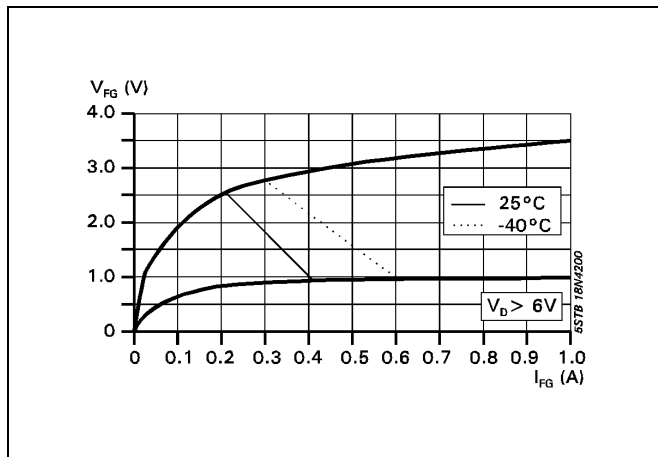


Fig. 8 Gate trigger characteristics.

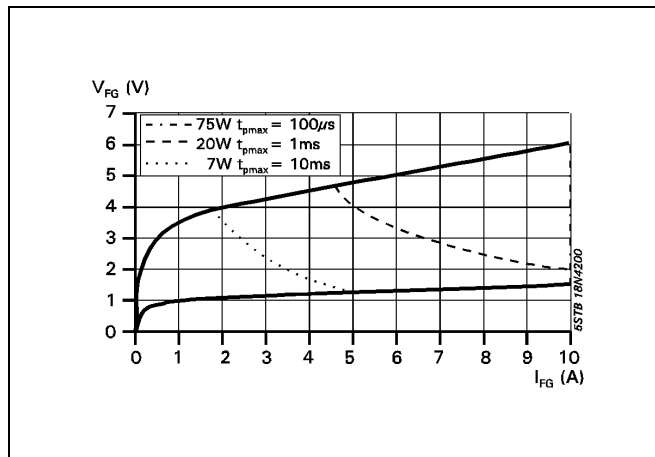


Fig. 9 Max. peak gate power loss.

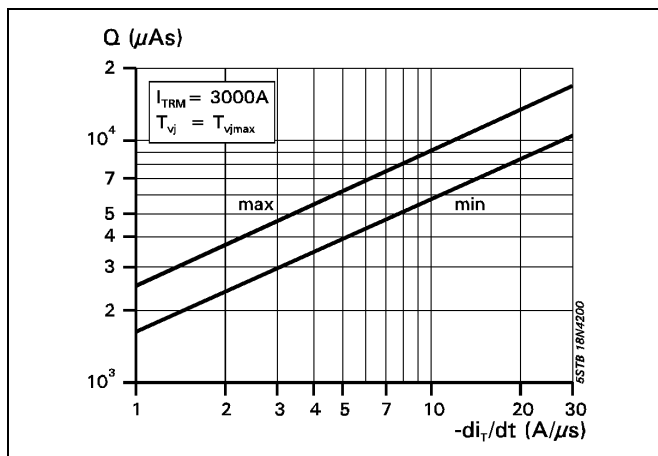


Fig. 10 Recovery charge vs. decay rate of on-state current.

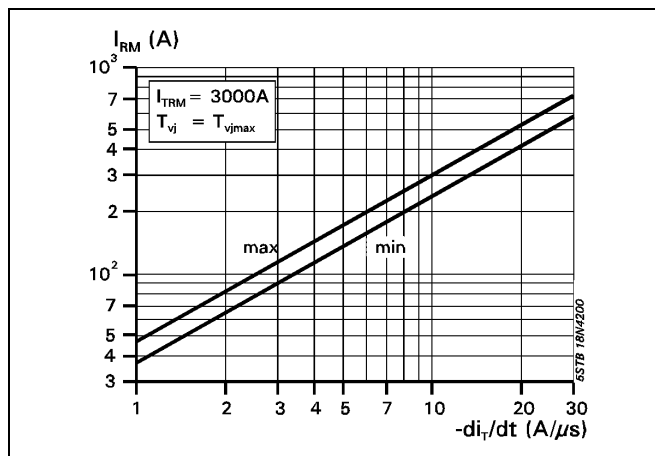


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

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ABB Semiconductors AG
 Fabrikstrasse 3
 CH-5600 Lenzburg, Switzerland

Telephone +41 (0)62 888 6419
 Fax +41 (0)62 888 6306
 Email abbsem@ch.abb.com
 Internet www.abbsem.com