

# TLP558

- Isolated Bus Driver
- High Speed Line Receiver
- Microprocessor System Interfaces
- MOS FET Gate Driver
- Transistor Inverter

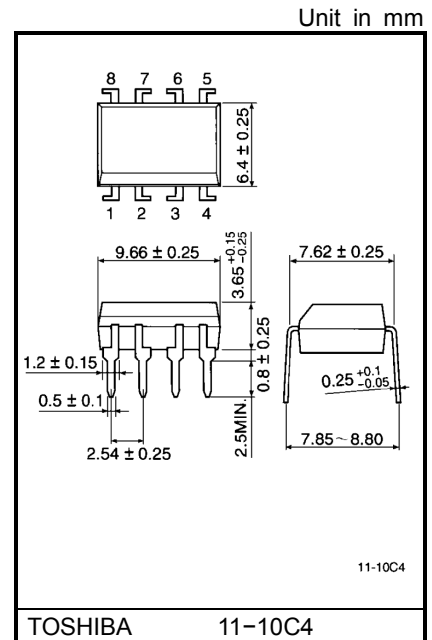
The TOSHIBA TLP558 consists of a GaAlAs light emitting diode and integrated high gain, high speed photodetector. This unit is 8-lead DIP package. The detector has a three state output stage that provides source drive and sink drive, and built-in schmitt trigger. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V /  $\mu$ s. TLP558 is inverter logic type. For buffer logic type, TLP555 is in line-up.

- Input current:  $I_F=1.6\text{mA}(\text{max.})$
- Power supply voltage:  $V_{CC}=4.5\sim 20\text{V}$
- Switching speed:  $t_{pHL}, t_{pLH}=400\text{ns}(\text{max.})$
- Common mode transient immunity:  $\pm 1000\text{V} / \mu\text{s}(\text{min.})$
- Guaranteed performance over temperature:  $-25\sim 85^\circ\text{C}$
- Isolation voltage:  $2500V_{\text{rms}}(\text{min.})$
- UL recognized: UL1577, file No. E67349

### Truth Table(positive logic)

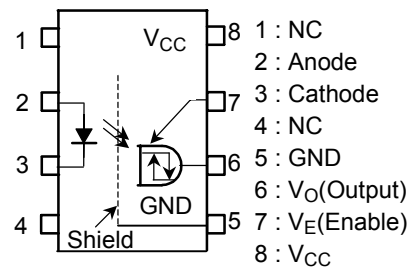
Input	Enable	Output
H	H	L
L	H	H
H	L	Z
L	L	Z

A 0.1 $\mu$ F bypass capacitor must be connected between pins 8 and 5 (see Note 9).

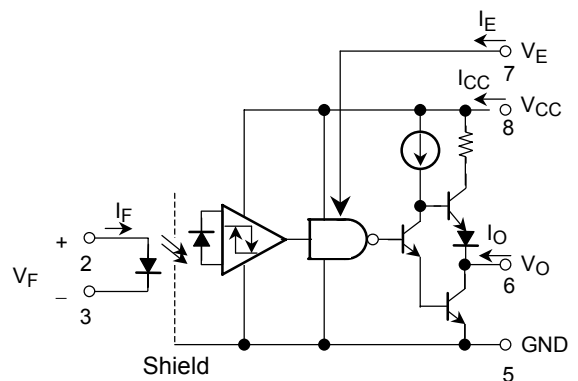


Weight: 0.54 g

### Pin Configuration(top view)



### Schematic



## Maximum Ratings (no derating required up to 85°C unless otherwise noted)

Characteristic		Symbol	Rating	Unit
LED	Forward current	$I_F$	10	mA
	Peak transient forward current (Note 1)	$I_{FPT}$	1	A
	Reverse voltage	$V_R$	5	V
Detector	Output current	$I_O$	40 / -25	mA
	Peak output current (Note 2)	$I_{OP}$	80 / -50	mA
	Output voltage	$V_O$	-0.5~20	V
	Supply voltage	$V_{CC}$	-0.5~20	V
	Three state enable voltage	$V_E$	-0.5~20	V
	Output power dissipation (Note 3)	$P_O$	100	mW
	Total package power dissipation (Note 4)	$P_T$	200	mW
	Operating temperature range	$T_{opr}$	-40~85	°C
Storage temperature range	$T_{stg}$	-55~125	°C	
Lead solder temperature(10s)**	$T_{sol}$	260	°C	
Isolation voltage(AC, 1min., R.H.≤ 60%, Ta=25°C) (Note 5)	$BV_S$	2500	Vrms	

(Note 1) Pulse width ≤ 1μs, 300pps.

(Note 2) Pulse width ≤ 5μs, duty ratio ≤ 0.025.

(Note 3) Derate 1.8mW / °C above 70°C ambient temperature.

(Note 4) Derate 3.6mW / °C above 70°C ambient temperature.

(Note 5) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

\*\*1.6mm below seating plane.

## Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input current, on	$I_{F(ON)}$	2*	—	5	mA
Input voltage, off	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage	$V_{CC}$	4.5	—	20	V
Enable voltage high	$V_{EH}$	2.0	—	20	V
Enable voltage low	$V_{EL}$	0	—	0.8	V
Fan out(TTL load)	N	—	—	4	—
Operating temperature	$T_{opr}$	-25	—	85	°C

\*2mA condition permits at least 20% CTR degradation guardband.

Initial switching threshold is 1.6mA or less.

## Electrical Characteristics(unless otherwise specified, Ta = -25~85°C, VCC = 4.5~20V)

Characteristic	Symbol	Test Condition	Min.	Typ.*	Max.	Unit	
Input forward voltage	V <sub>F</sub>	I <sub>F</sub> =5mA, Ta=25°C	—	1.55	1.7	V	
Temperature coefficient of forward voltage	ΔV <sub>F</sub> / ΔTa	I <sub>F</sub> =5mA	—	-2.0	—	mV / °C	
Input reverse current	I <sub>R</sub>	V <sub>R</sub> =5V, Ta=25°C	—	—	10	μA	
Input capacitance	C <sub>T</sub>	V <sub>F</sub> =0, f=1MHz, Ta=25°C	—	45	—	pF	
Output leakage current (V <sub>O</sub> > V <sub>CC</sub> )	I <sub>OHH</sub>	V <sub>F</sub> =0, V <sub>CC</sub> =4.5V	V <sub>O</sub> =V <sub>E</sub> =5.5V	—	—	100	μA
			V <sub>O</sub> =V <sub>E</sub> =20V	—	0.01	500	
Logic low output voltage	V <sub>OL</sub>	I <sub>OL</sub> =6.4mA, I <sub>F</sub> =1.6mA V <sub>E</sub> =2V	—	0.4	0.5	V	
Logic high output voltage	V <sub>OH</sub>	I <sub>OH</sub> =-2.6mA, V <sub>F</sub> =0.8V V <sub>E</sub> =2V	2.4	3.3	—	V	
Logic low enable current	I <sub>EL</sub>	V <sub>E</sub> =0.4V	—	-0.13	-0.32	mA	
Logic high enable current	I <sub>EH</sub>	V <sub>E</sub> =2.7V	—	—	20	μA	
		V <sub>E</sub> =5.5V	—	—	100		
		V <sub>E</sub> =20V	—	0.01	250		
Logic low enable voltage	V <sub>EL</sub>	—	—	—	0.8	V	
Logic high enable voltage	V <sub>EH</sub>	—	2.0	—	—	V	
Logic low supply current	I <sub>CCL</sub>	I <sub>F</sub> =5mA	V <sub>CC</sub> =V <sub>E</sub> =5.5V	—	4.0	6.0	mA
			V <sub>CC</sub> =V <sub>E</sub> =20V	—	4.6	7.5	
Logic high supply current	I <sub>CCH</sub>	V <sub>F</sub> =0V	V <sub>CC</sub> =V <sub>E</sub> =5.5V	—	4.2	6.0	mA
			V <sub>CC</sub> =V <sub>E</sub> =20V	—	4.7	7.5	
High impedance state output current	I <sub>OZL</sub>	V <sub>F</sub> =0V V <sub>E</sub> =0.8V	V <sub>O</sub> =0.4V	—	—	-20	μA
			V <sub>O</sub> =2.4V	—	—	20	
	I <sub>OZH</sub>	I <sub>F</sub> =5mA V <sub>E</sub> =0.8V	V <sub>O</sub> =5.5V	—	—	100	
			V <sub>O</sub> =20V	—	1	500	
Logic low short circuit output current (Note 6)	I <sub>OSL</sub>	I <sub>F</sub> =5mA V <sub>E</sub> =2V	V <sub>O</sub> =V <sub>CC</sub> =5.5V	25	55	—	mA
			V <sub>O</sub> =V <sub>CC</sub> =20V	40	80	—	
Logic high short circuit output current (Note 6)	I <sub>OSH</sub>	V <sub>F</sub> =0V, V <sub>O</sub> =GND V <sub>E</sub> =2V	V <sub>CC</sub> =5.5V	-10	-25	—	mA
			V <sub>CC</sub> =20V	-25	-60	—	
Input current logic low output	I <sub>FL</sub>	V <sub>E</sub> =2V, I <sub>O</sub> =6.4mA V <sub>O</sub> < 0.4V	—	0.4	1.6	mA	
Input voltage logic high output	V <sub>FH</sub>	V <sub>E</sub> =2V, I <sub>O</sub> =-2.6mA V <sub>O</sub> > 2.4V	0.8	—	—	V	

## Electrical Characteristics(unless otherwise specified, Ta = -25~85°C, VCC = 4.5~20V)

Characteristic	Symbol	Test Condition	Min.	Typ.*	Max.	Unit
Input current hysteresis	I <sub>HYS</sub>	V <sub>CC</sub> =V <sub>E</sub> =5V	—	0.05	—	mA
Resistance (input-output)	R <sub>S</sub>	V <sub>S</sub> =500V, R.H. ≤60% Ta=25°C (Note 5)	5×10 <sup>10</sup>	10 <sup>14</sup>	—	Ω
Capacitance(input-output)	C <sub>S</sub>	V <sub>S</sub> =0, f=1MHz, Ta=25°C (Note 5)	—	1.0	—	pF

\*All typical values are at Ta=25°C, V<sub>CC</sub>=5V, I<sub>F(ON)</sub>=3mA unless otherwise specified.

## Switching Characteristics(unless otherwise specified, VCC = 4.5~20V, Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.*	Max.	Unit
Propagation delay time to logic high output (Note 7)	t <sub>pLH</sub>	1	I <sub>F</sub> =3→0mA	—	250	400	ns
Propagation delay time to logic low output (Note 7)	t <sub>pHL</sub>		I <sub>F</sub> =0→3mA	—	270	400	ns
Output rise time (10~90%)	t <sub>r</sub>		I <sub>F</sub> =3→0mA, V <sub>CC</sub> =5V	—	35	75	ns
Output fall time (90~10%)	t <sub>f</sub>		I <sub>F</sub> =0→3mA, V <sub>CC</sub> =5V	—	20	75	ns
Output enable time to logic high	t <sub>pZH</sub>	2	V <sub>E</sub> =0→3V	—	—	—	ns
Output enable time to logic low	t <sub>pZL</sub>		V <sub>E</sub> =0→3V	—	—	—	ns
Output disable time from logic high	t <sub>pHZ</sub>		V <sub>E</sub> =3→0V	—	—	—	ns
Output disable time from logic low	t <sub>pLZ</sub>		V <sub>E</sub> =3→0V	—	—	—	ns
Common mode transient immunity at logic high output (Note 8)	C <sub>MH</sub>	3	I <sub>F</sub> =0mA, V <sub>CM</sub> =50V V <sub>O(Min.)</sub> =2V	1000	—	—	V / μs
Common mode transient immunity at logic low output (Note 8)	C <sub>M L</sub>		I <sub>F</sub> =1.6mA, V <sub>CM</sub> =50V V <sub>O(Max.)</sub> =0.8V	-1000	—	—	V / μs

\* All typical values are at Ta=25°C, V<sub>CC</sub>=5V

(Note 6) Duration of output short circuit time should not exceed 10ms.

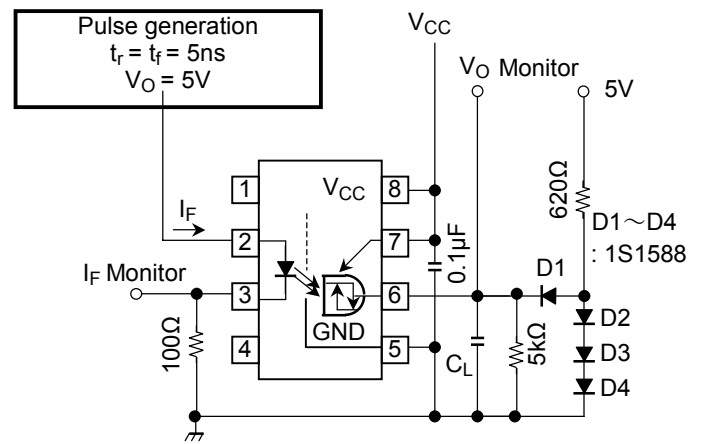
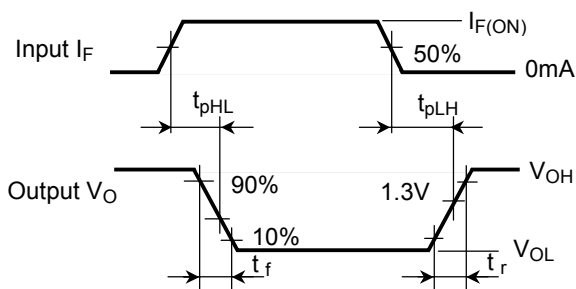
(Note 7) The  $t_{pLH}$  propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The  $t_{pHL}$  propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

(Note 8)  $C_{ML}$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O > 0.8V$ ).

$C_{MH}$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic state ( $V_O > 2.0$ ).

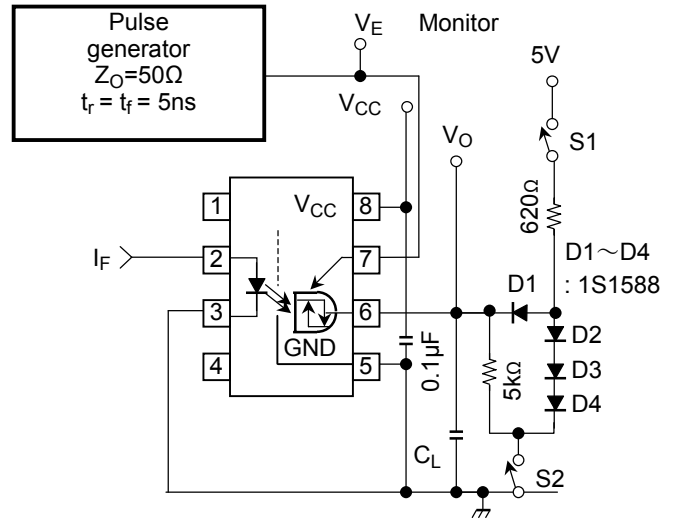
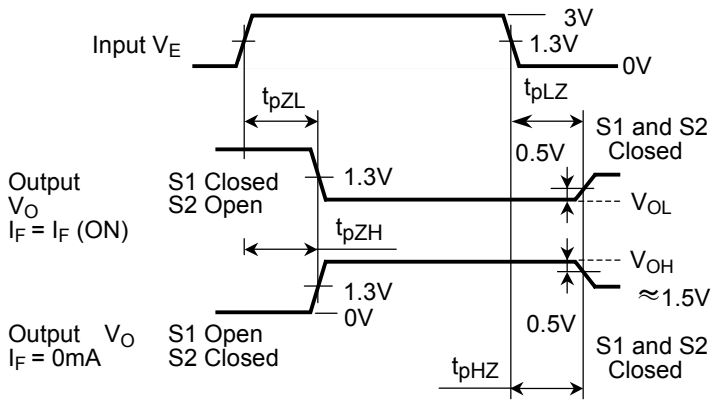
(Note 9) A ceramic capacitor (0.1 $\mu$ F) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

## Test Circuit 1: $t_{pLH}$ , $t_{pHL}$ , $t_r$ And $t_f$



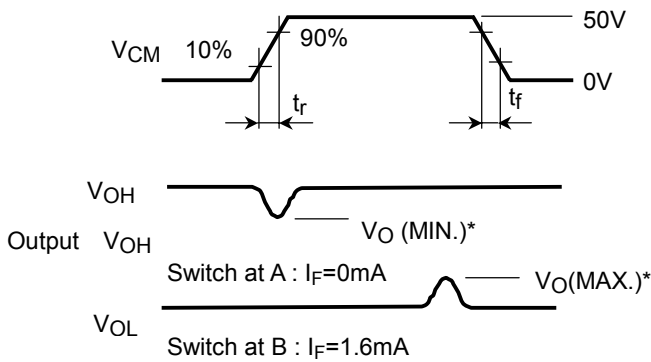
$C_L$  is approximately 15pF which includes probe and stray wiring capacitance.

**Test Circuit 2:  $t_{pHZ}$ ,  $t_{pZH}$ ,  $t_{pLZ}$  And  $t_{pZL}$**

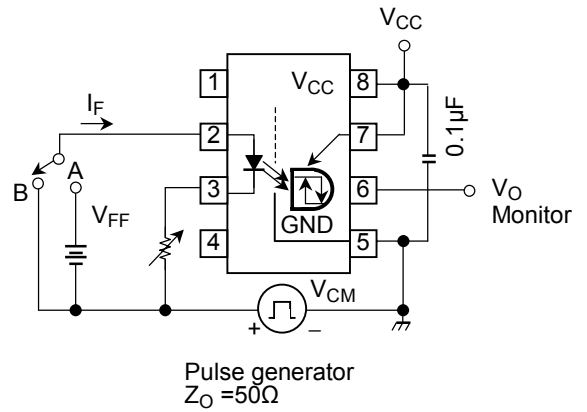


$C_L$  is approximately  $15pF$  which includes probe and stray wiring capacitance.

**Test Circuit 3: Common Mode Transient Immunity**



\* Note 8  
 $CM_H = \frac{45(V)}{t_f(\mu s)}$ ,  $CM_L = \frac{45(V)}{t_f(\mu s)}$



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