

FEATURES

- **High Current Transfer Ratios**
 - at 10 mA: 40–320%
 - at 1 mA: 45% typical (>13)
- **Low CTR Degradation**
- **Good CTR Linearity Depending on Forward Current**
- **Isolation Test Voltage, 5300 VAC_{RMS}**
- **High Collector-Emitter Voltage, V_{CEO}=70 V**
- **Low Saturation Voltage**
- **Fast Switching Times**
- **Field-Effect Stable by TRIOS (TRansparent IO n Shield)**
- **Temperature Stable**
- **Low Coupling Capacitance**
- **End-Stackable, .100" (2.54 mm) Spacing**
- **High Common-Mode Interference Immunity (Unconnected Base)**
- **Underwriters Lab File #52744**
- **VDE 0884 Available with Option 1**
- **SMD Option, See SFH6206 Data Sheet**

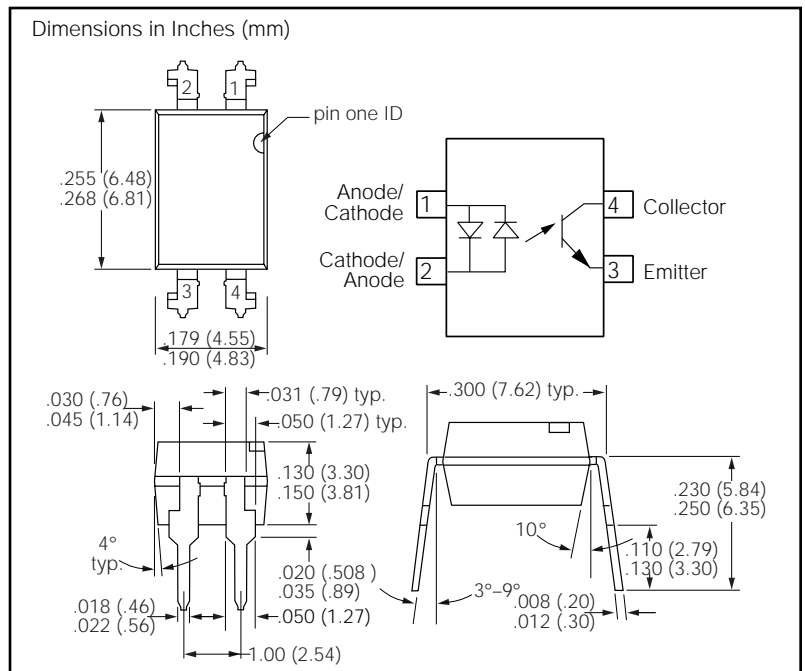
DESCRIPTION

The SFH620A features a high current transfer ratio, low coupling capacitance and high isolation voltage. These couplers have a GaAs infrared emitting diode emitter, which is optically coupled to a silicon planar phototransistor detector, and is incorporated in a plastic DIP-4 package.

The coupling devices are designed for signal transmission between two electrically separated circuits.

The couplers are end-stackable with 2.54 mm spacing.

Creepage and clearance distances of >8 mm are achieved with option 6. This version complies with IEC 950 (DIN VDE 0805) for reinforced insulation up to an operation voltage of 400 V_{RMS} or DC.



Maximum Ratings

Emitter

Reverse Voltage.....	6 V
DC Forward Current.....	±60 mA
Surge Forward Current (t _p ≤10 μs).....	±2.5 A
Total Power Dissipation.....	100 mW

Detector

Collector-Emitter Voltage.....	70 V
Emitter-Collector Voltage.....	7 V
Collector Current.....	50 mA
Collector Current (t _p ≤1 ms).....	100 mA
Total Power Dissipation.....	150 mW

Package

Isolation Test Voltage between Emitter and Detector, refer to Climate DIN 40046, part 2, Nov. 74.....	5300 VAC _{RMS}
Creepage.....	≥7 mm
Clearance.....	≥7 mm
Insulation Thickness between Emitter and Detector.....	≥0.4 mm
Comparative Tracking Index per DIN IEC 112/VDE0 303, part 1.....	175
Isolation Resistance	
V _{IO} =500 V, T _A =25°C.....	≥10 ¹² Ω
V _{IO} =500 V, T _A =100°C.....	≥10 ¹¹ Ω
Storage Temperature Range.....	-55 to +150°C
Ambient Temperature Range.....	-55 to +100°C
Junction Temperature.....	100°C
Soldering Temperature (max. 10 s. Dip Soldering Distance to Seating Plane ≥1.5 mm).....	260°C

Characteristics (T_A=25°C)

Description	Symbol		Unit	Condition
Emitter				
Forward Voltage	V _F	1.25 (≤1.65)	V	I _F =±60 mA
Capacitance	C ₀	50	pF	V _R =0 V, f=1 MHz
Thermal Resistance	R _{thJA}	750	K/W	
Detector				
Capacitance	C _{CE}	6.8	pF	V _{CE} =5 V, f=1 MHz
Thermal Resistance	R _{thJA}	500	K/W	
Package				
Collector-Emitter Saturation Voltage	V _{CESAT}	0.25 (≤0.4)	V	I _F =10 mA, I _C =2.5 mA
Coupling Capacitance	C _C	0.2	pF	

Note: Still air, coupler soldered to PCB or base.

Current Transfer Ratio (I_C/I_F at V_{CE}=5 V) and Collector-Emitter Leakage Current by Dash Number

Description	-1	-2	-3	
I _C / I _F (I _F =±10 mA)	40–125	63–200	100–320	%
I _C / I _F (I _F =±1 mA)	30 (>13)	45 (>22)	70 (>34)	%
Collector-Emitter Leakage Current, I _{CEO} V _{CE} =10 V	2 (≤50)	2 (≤50)	5 (≤100)	nA

Figure 1. Current transfer ratio (typ.) vs. temperature

$I_F = 10 \text{ mA}$, $V_{CE} = 5 \text{ V}$

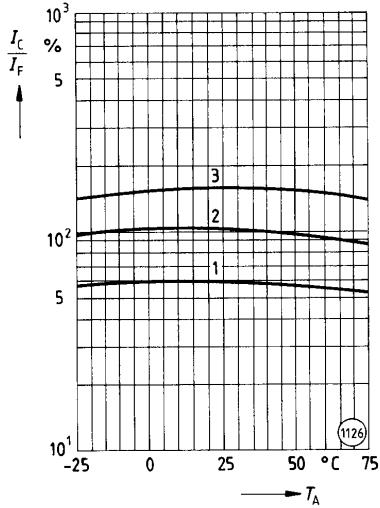


Figure 4. Transistor capacitance (typ.) vs. collector-emitter voltage

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$

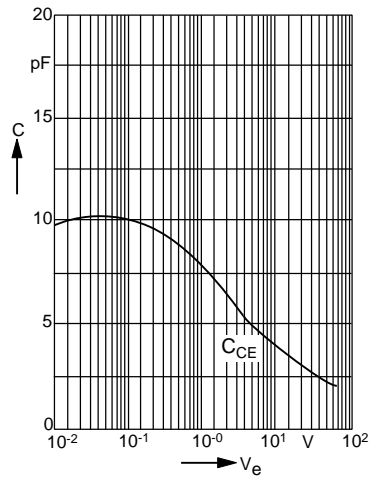


Figure 7. Permissible diode forward current vs. ambient temp.

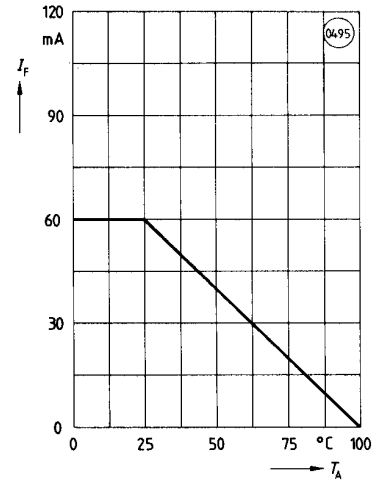


Figure 2. Output characteristics (typ.) Collector current vs. collector-emitter voltage $T_A = 25^\circ\text{C}$

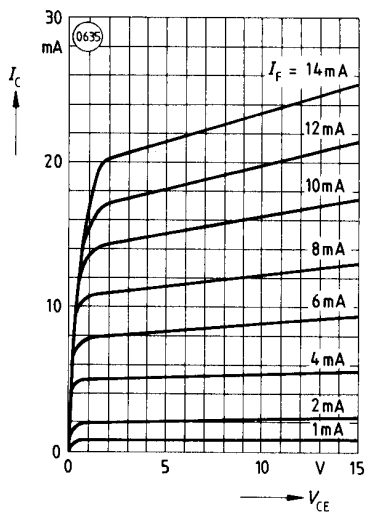


Figure 5. Permissible pulse handling capability. Fwd. current vs. pulse width

Pulse cycle $D = \text{parameter}$, $T_A = 25^\circ\text{C}$

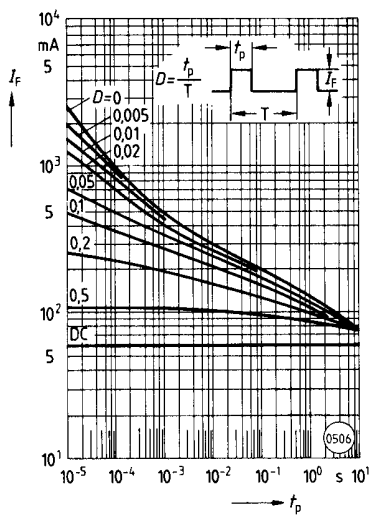
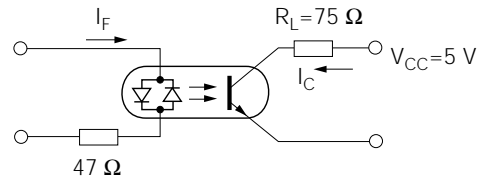


Figure 8. Switching Times Linear Operation (without saturation)



$I_F = 10 \text{ mA}$, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Load Resistance	R_L	75	Ω
Turn-on Time	t_{ON}	3.0	μs
Rise Time	t_r	2.0	μs
Turn-off Time	t_{OFF}	2.3	μs
Fall Time	t_f	2.0	μs
Cut-off Frequency	F_{CO}	250	kHz

Figure 3. Diode forward voltage (typ.) vs. forward current

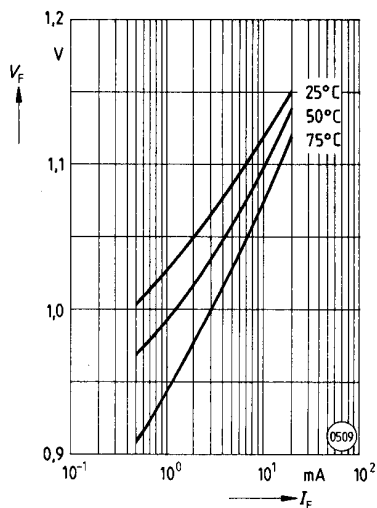


Figure 6. Permissible power dissipation vs. ambient temp.

