

FOD8012

High CMR, Bi-Directional, Logic Gate Optocoupler

Features

- Full Duplex, Bi-Directional
- 20kV/μs Minimum Common Mode Rejection
- High Speed:
 - 15Mbit/sec Data Rate (NRZ)
 - 60ns max. Propagation Delay
 - 15ns max. Pulse Width Distortion
 - 30ns max. Propagation Delay Skew
- 3.3V and 5V CMOS Compatibility
- Extended industrial temperature range, -40 to +110°C temperature range
- Safety and regulatory approvals
 - UL1577, 3750 VAC_{RMS} for 1 min.
 - DIN EN/IEC60747-5-2 (approval pending)

Applications

- Industrial fieldbus communications
 - DeviceNet, CAN, RS485, RS232
- Microprocessor System Interface
 - SPI, I²C
- Programmable Logic Control
- Isolated Data Acquisition System
- Voltage Level Translator

Description

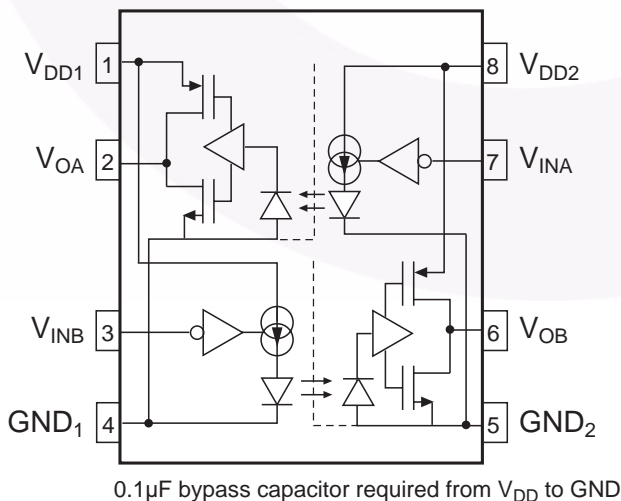
The FOD8012 is a full duplex, bi-directional, high-speed logic gate Optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes Fairchild's proprietary coplanar packaging technology, Optoplanar[®], and opti-IC design to achieve minimum 20kV/μs Common Mode Noise Rejection (CMR) rating.

This high-speed logic gate optocoupler is highly integrated with 2 optically coupled channels arranged in bi-directional configuration, and housed in a compact 8-pin small outline package. Each optocoupler channel consists of a high-speed AlGaAs LED driven by a CMOS buffer IC coupled to a CMOS detector IC. The detector IC comprises of an integrated photodiode, a high-speed trans-impedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled to the high efficiency of the LED achieves low power consumption as well as very high speed (60ns propagation delay, 15ns pulse width distortion).

Related Resources

- [FOD8001, High Noise Immunity, 3.3V/5V Logic Gate Optocoupler Datasheet](#)
- www.fairchildsemi.com/products/opto/

Functional Schematic



Truth Table

| V _{IN} | LED | V _O |
|-----------------|-----|----------------|
| High | OFF | High |
| Low | ON | Low |

Pin Definitions

| Pin Number | Pin Name | Description |
|------------|------------------|--|
| 1 | V _{DD1} | Supply Voltage to Channel-A detector IC and Channel-B buffer IC |
| 2 | V _{OA} | Output Voltage from Channel-A detector IC |
| 3 | V _{INB} | Input Voltage to Channel-B buffer IC |
| 4 | GND ₁ | Ground for Channel-A detector IC and Channel-B buffer IC |
| 5 | GND ₂ | Ground for Channel-A buffer IC and Channel-B detector IC |
| 6 | V _{OB} | Output Voltage from Channel-B detector IC |
| 7 | V _{INA} | Input Voltage to Channel-A buffer IC |
| 8 | V _{DD2} | Supply Voltage to Channel-A buffer IC and Channel-B detector IC |

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Value | Units |
|-------------------------------------|--|-----------------|-------|
| T _{STG} | Storage Temperature | -40 to +125 | °C |
| T _{OPR} | Operating Temperature | -40 to +110 | °C |
| T _J | Junction Temperature | -40 to +130 | °C |
| T _{SOL} | Lead Solder Temperature (Refer to Reflow Temperature Profile) | 260 for 10sec | °C |
| V _{DD1} , V _{DD2} | Supply Voltage | 0 to 6.0 | V |
| V _{IA} , V _{IB} | Input Voltage | -0.5 to VDD+0.5 | V |
| I _{IA} , I _{IB} | Input DC Current | -10 to +10 | µA |
| V _{OA} , V _{OB} | Output Voltage | -0.5 to VDD+0.5 | V |
| I _{OA} , I _{OB} | Average Output Current | 10 | mA |
| PD _I | Input Power Dissipation ⁽¹⁾ | 60 | mW |
| PD _O | Output Power Dissipation ⁽¹⁾ | 60 | mW |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------------------------|---|------|-----------------|------|
| T _A | Ambient Operating Temperature | -40 | +110 | °C |
| V _{DD1} , V _{DD2} | Supply Voltages (3.3V Operation) ⁽²⁾ | 3.0 | 3.6 | V |
| | Supply Voltages (5.0V Operation) ⁽²⁾ | 4.5 | 5.5 | V |
| V _{IH} | Logic High Input Voltage | 2.0 | V _{DD} | V |
| V _{IL} | Logic Low Input Voltage | 0 | 0.8 | V |
| t _r , t _f | Input Signal Rise and Fall Time | | 1.0 | ms |

Isolation Characteristics

Apply over all recommended conditions, typical value is measured at $T_A = 25^\circ\text{C}$

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------|--------------------------------|---|-----------|------|------|-------------|
| V_{ISO} | Input-Output Isolation Voltage | freq = 60Hz, t = 1.0min, $I_{I-O} \leq 10\mu\text{A}^{(3)(4)}$ | 3750 | | | V_{aCRMS} |
| R_{ISO} | Isolation Resistance | $V_{I-O} = 500\text{V}^{(3)}$ | 10^{11} | | | Ω |
| C_{ISO} | Isolation Capacitance | $V_{I-O} = 0\text{V}$, freq = 1.0MHz ⁽³⁾ | | 0.2 | | pF |

Electrical Characteristics

$T_A = -40^\circ\text{C}$ to $+110^\circ\text{C}$, $3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$, unless otherwise specified.

Apply over all recommended conditions, typical value is measured at $V_{DD1} = V_{DD2} = +3.3\text{V}$, $T_A = 25^\circ\text{C}$

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------------|---------------------------|---|------|------|------|---------------|
| I_{DD1L}, I_{DD2L} | Logic Low Supply Current | $V_{IA}, V_{IB} = 0\text{V}$ | | 5.8 | 8.0 | mA |
| I_{DD1H}, I_{DD2H} | Logic High Supply Current | $V_{IA}, V_{IB} = V_{DD}$ | | 2.5 | 4.0 | mA |
| I_{IA}, I_{IB} | Input Current | | -10 | | +10 | μA |
| V_{OH} | Logic High Output Voltage | $I_O = -20\mu\text{A}$, $V_{DD} = 3.3\text{V}$, $V_I = V_{IH}$ | 3.2 | 3.3 | | V |
| | | $I_O = -4\text{mA}$, $V_{DD} = 3.3\text{V}$, $V_I = V_{IH}$ | 3.0 | 3.1 | | V |
| | | $I_O = -20\mu\text{A}$, $V_{DD} = 5\text{V}$, $V_I = V_{IH}$ | 4.9 | 5.0 | | V |
| | | $I_O = -4\text{mA}$, $V_{DD} = 5\text{V}$, $V_I = V_{IH}$ | 4.7 | 4.8 | | V |
| V_{OL} | Logic Low Output Voltage | $I_O = 20\mu\text{A}$, $V_{DD} = 3.3\text{V}$ or 5V , $V_I = V_{IL}$ | | 0 | 0.1 | V |
| | | $I_O = 4\text{mA}$, $V_{DD} = 3.3\text{V}$ or 5V , $V_I = V_{IL}$ | | 0.26 | 0.6 | V |

Switching Characteristics

$T_A = -40^\circ\text{C}$ to $+110^\circ\text{C}$, $3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$, unless otherwise specified.

Apply over all recommended conditions, typical value is measured at $V_{DD1} = V_{DD2} = +3.3\text{V}$, $T_A = 25^\circ\text{C}$

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------|---|---|------|------|------|-------------------|
| Data Rate | | | | | 15 | Mbit/s |
| t_{PHL} | Propagation Delay Time to Logic Low Output | $PW = 66.7\text{ns}$, $C_L = 15\text{pF}$ | | 37 | 60 | ns |
| t_{PLH} | Propagation Delay Time to Logic High Output | $PW = 66.7\text{ns}$, $C_L = 15\text{pF}$ | | 40 | 60 | ns |
| PWD | Pulse Width Distortion, $ t_{PHL} - t_{PLH} $ | $PW = 66.7\text{ns}$, $C_L = 15\text{pF}^{(5)}$ | | 3 | 15 | ns |
| $t_{PSK(CC)}$ | Channel-Channel Skew | $PW = 66.7\text{ns}$, $C_L = 15\text{pF}^{(6)}$ | | 12 | 25 | ns |
| $t_{PSK(PP)}$ | Part-Part Skew | $PW = 66.7\text{ns}$, $C_L = 15\text{pF}^{(7)}$ | | | 30 | ns |
| t_R | Output Rise Time (10% to 90%) | $PW = 66.7\text{ns}$, $C_L = 15\text{pF}$ | | 6.5 | | ns |
| t_F | Output Fall Time (90% to 10%) | $PW = 66.7\text{ns}$, $C_L = 15\text{pF}$ | | 6.5 | | ns |
| $ CM_H $ | Common Mode Transient Immunity at Output High | $V_I = V_{DD1}$, $V_O > 0.8V_{DD1}$, $V_{CM} = 1000\text{V}^{(8)}$ | 20 | 40 | | kV/ μs |
| $ CM_L $ | Common Mode Transient Immunity at Output Low | $V_I = 0\text{V}$, $V_O < 0.8\text{V}$, $V_{CM} = 1000\text{V}^{(8)}$ | 20 | 40 | | kV/ μs |

Notes:

- No derating required.
- 0.1 μF bypass capacitor must be connected between Pin 1 and 4, and 5 and 8. The capacitors should be kept close to the supply pins.
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- 3,750 $V_{AC_{RMS}}$ for 1 minute duration is equivalent to 4,500 $V_{AC_{RMS}}$ for 1 second duration.
- PWD is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen for one channel switching, while holding the other channel output at a low or high state, or while both channels are in synchronous data transmission mode.
- $t_{PSK(CC)}$ is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between the two channels within a single device.
- $t_{PSK(PP)}$ is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between any two units from the same manufacturing date code that are operated at same case temperature, at same operating conditions, with equal loads.
- Common mode transient immunity at output high is the maximum tolerable positive dV_{cm}/dt on the leading edge of the common mode impulse signal, V_{cm} , to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dV_{cm}/dt on the trailing edge of the common pulse signal, V_{cm} , to assure that the output will remain low.

Typical Performance Curves

Fig. 1 Typical Output Voltage vs. Input Voltage (Channel A & B)

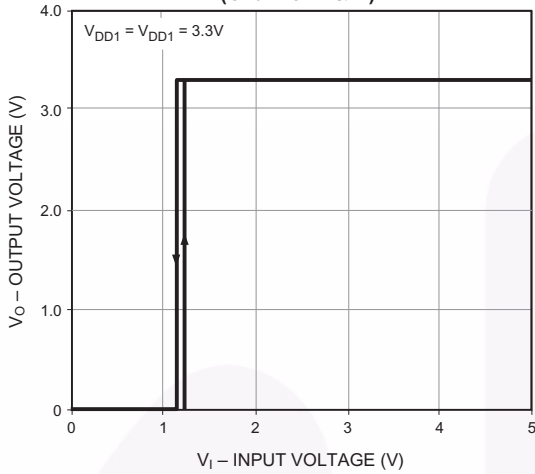


Fig. 2 Typical Input Voltage Switching Threshold vs. Input Supply Voltage (Channel A & B)

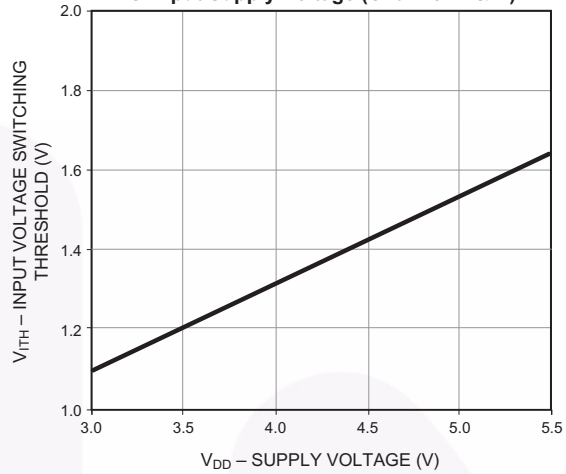


Fig. 3 Typical Propagation Delay vs. Ambient Temperature (Channel A & B)

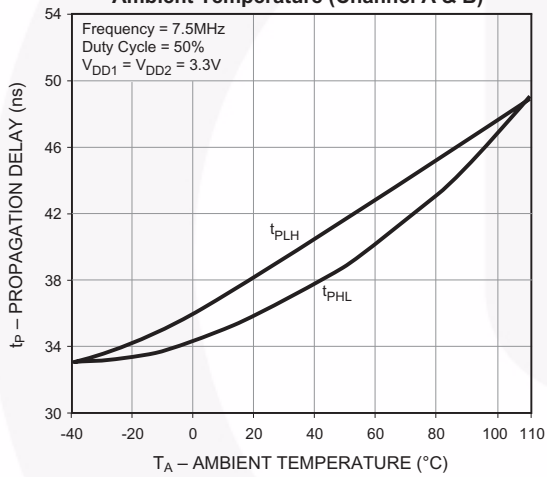


Fig. 4 Typical $t_{PHL} - t_{PLH}$ vs. Ambient Temperature (Channel A & B)

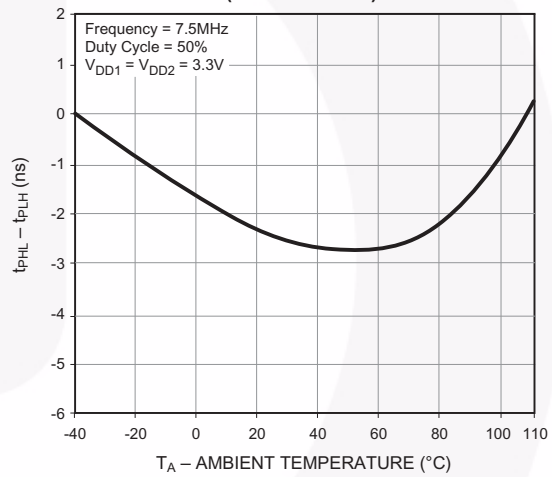


Fig. 5 Typical Rise Time vs. Ambient Temperature (Channel A & B)

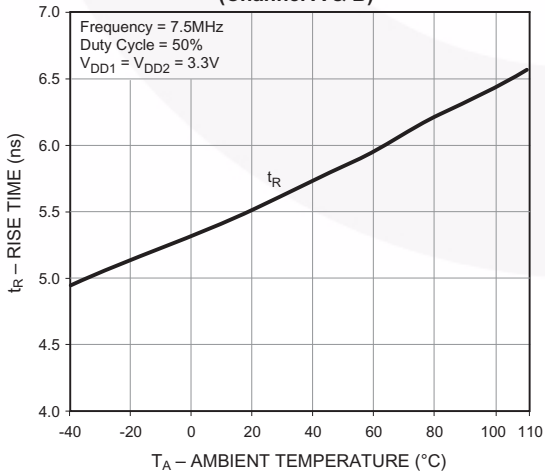
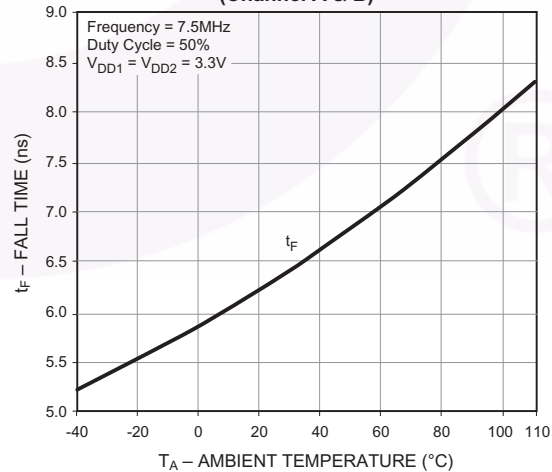


Fig. 6 Typical Fall Time vs. Ambient Temperature (Channel A & B)



Typical Performance Curves (Continued)

Fig. 7 Typical Propagation Delay vs. Output Load Capacitance (Channel A & B)

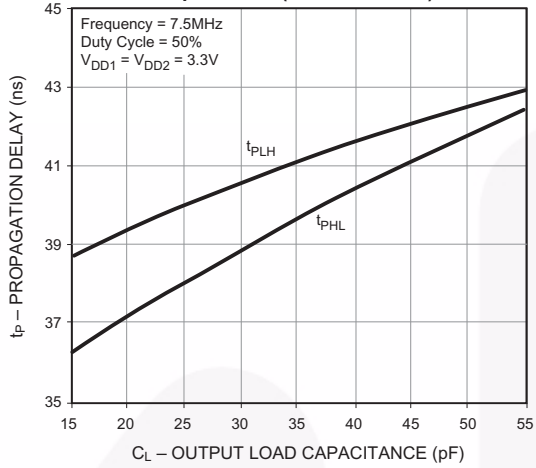


Fig. 8 Typical $t_{PHL} - t_{PLH}$ vs. Output Load Capacitance (Channel A & B)

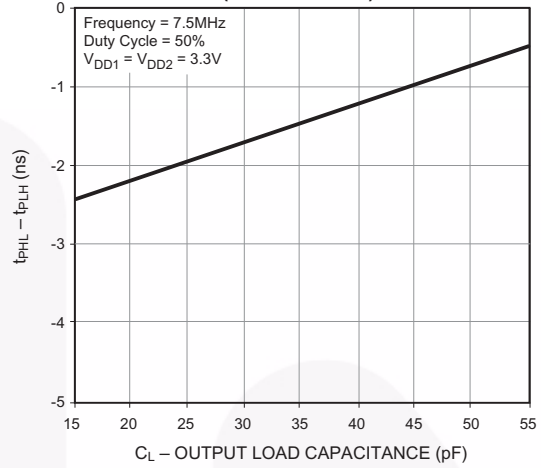


Fig. 9 Typical Rise Time vs. Output Load Capacitance (Channel A & B)

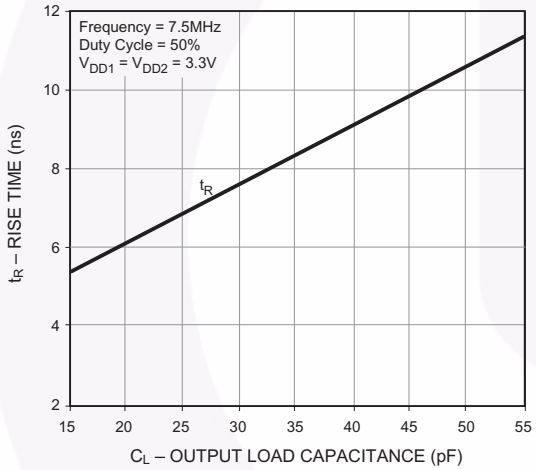
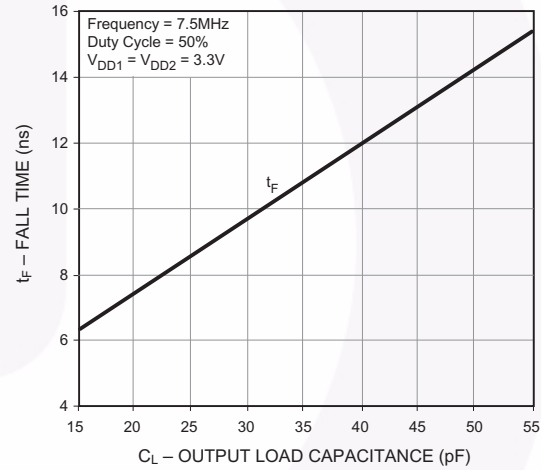


Fig. 10 Typical Fall Time vs. Output Load Capacitance (Channel A & B)



Typical Performance Curves (Continued)

Fig. 11a Typical I_{DD1}/I_{DD2} Supply Current vs. Frequency

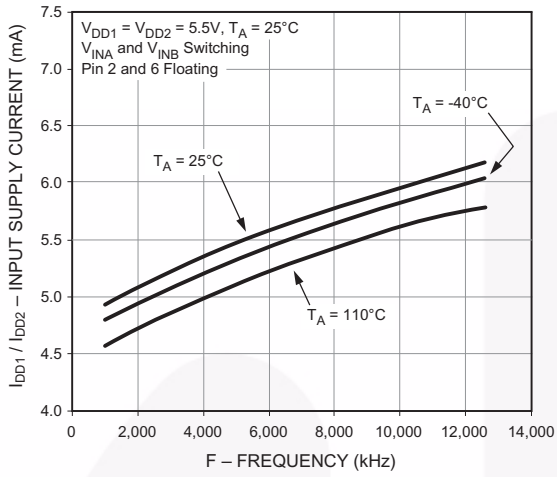


Fig. 11b Typical I_{DD1}/I_{DD2} Supply Current vs. Frequency

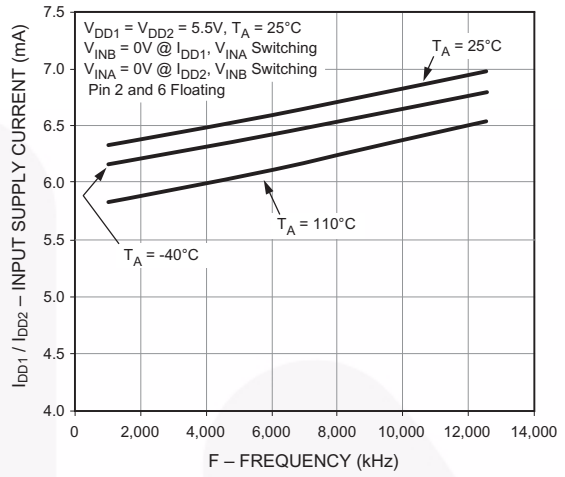
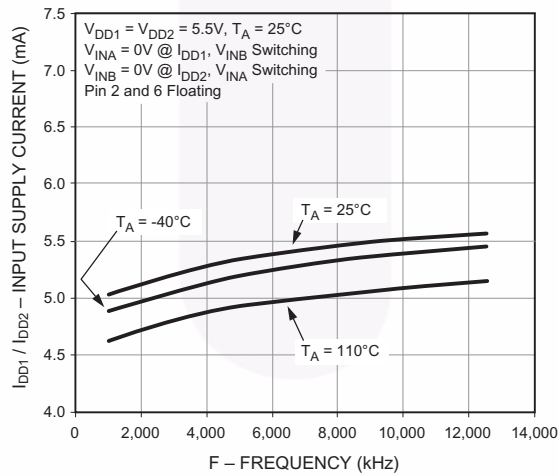


Fig. 11c Typical I_{DD1}/I_{DD2} Supply Current vs. Frequency



Test Circuits

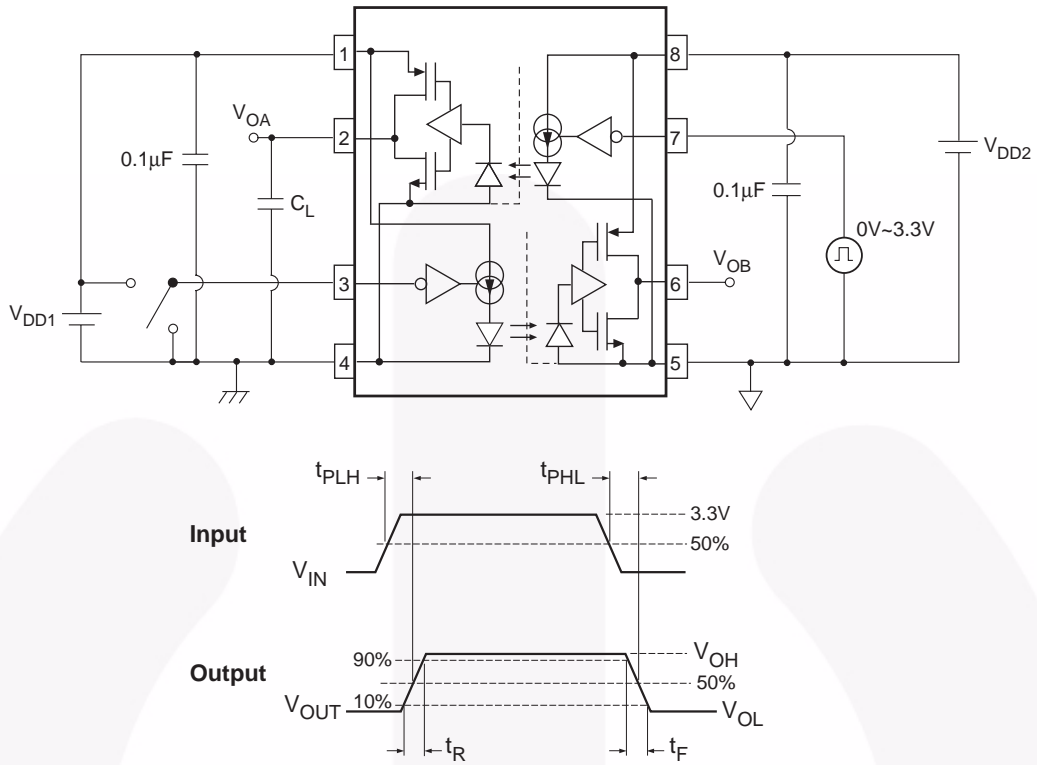


Figure 11. Test Circuit for Propagation Delay Time and Rise Time, Fall Time

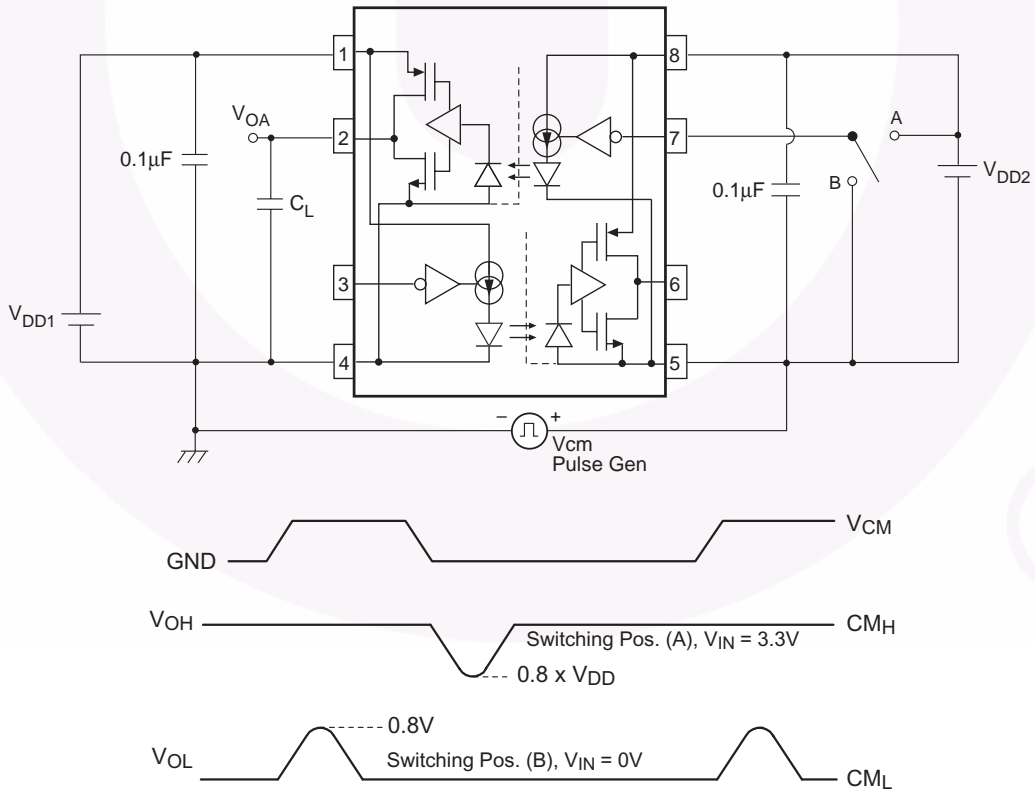
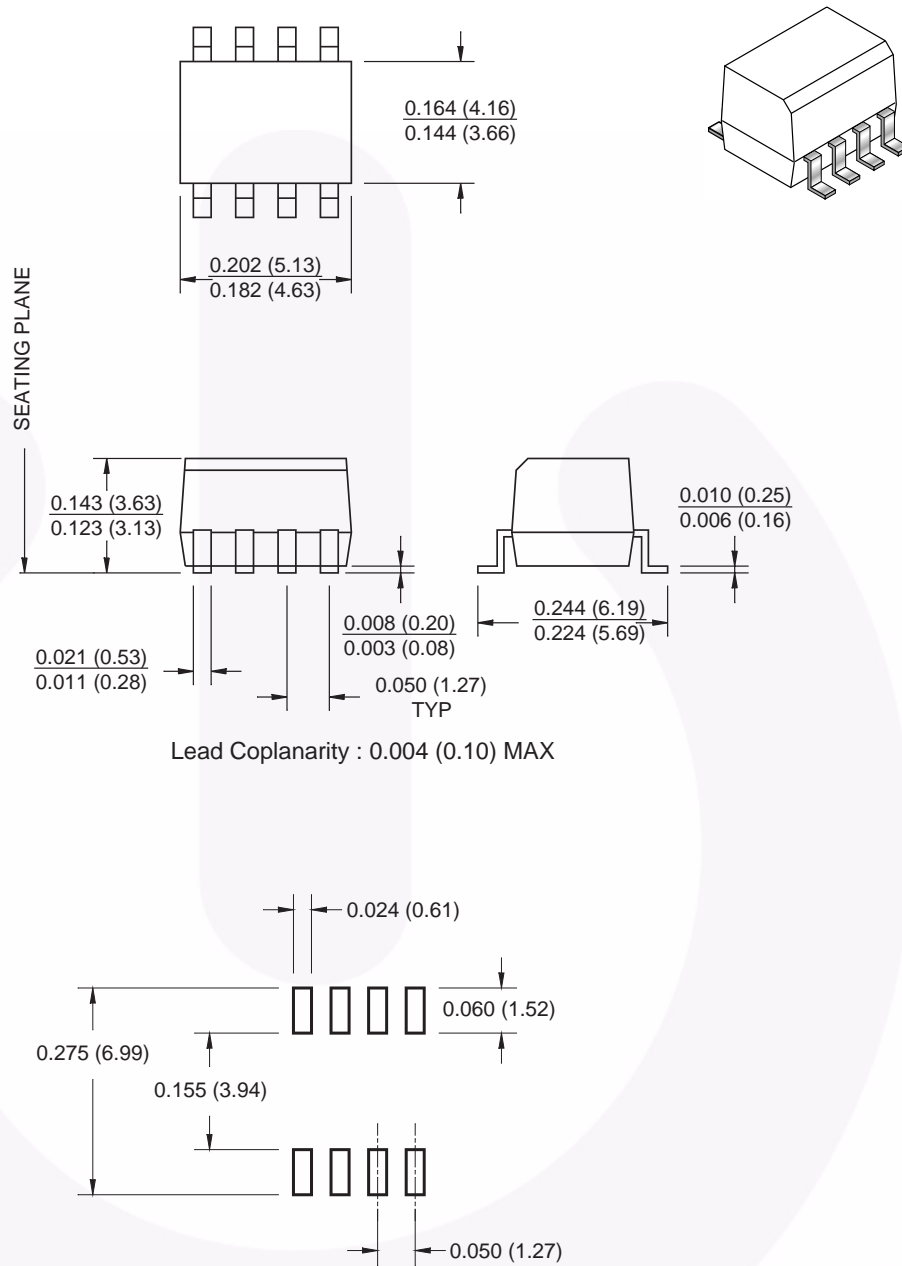


Figure 12. Test Circuit for Instantaneous Common Mode Rejection Voltage

Small Outline Package Dimensions



Note:

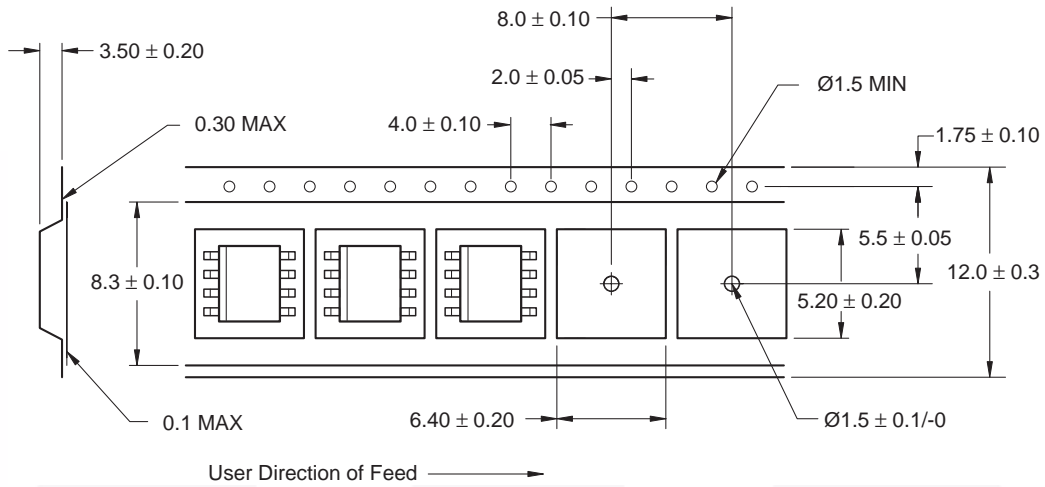
All dimensions are in millimeters.

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Carrier Tape Specification



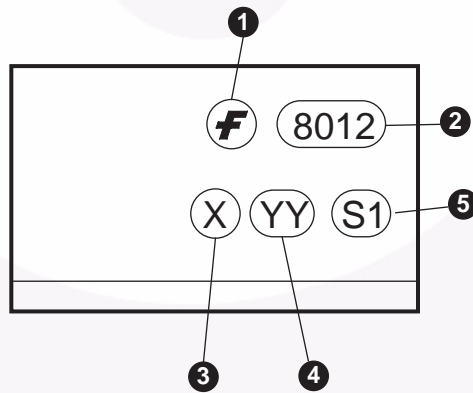
Note:
All dimensions are in millimeters.

Ordering Information

| Option | Order Entry Identifier | Description |
|-----------|------------------------|---|
| No Suffix | FOD8012 | Small outline 8-pin, shipped in tubes (50 units per tube) |
| R2 | FOD8012R2 | Small outline 8-pin, tape and reel (2,500 units per reel) |

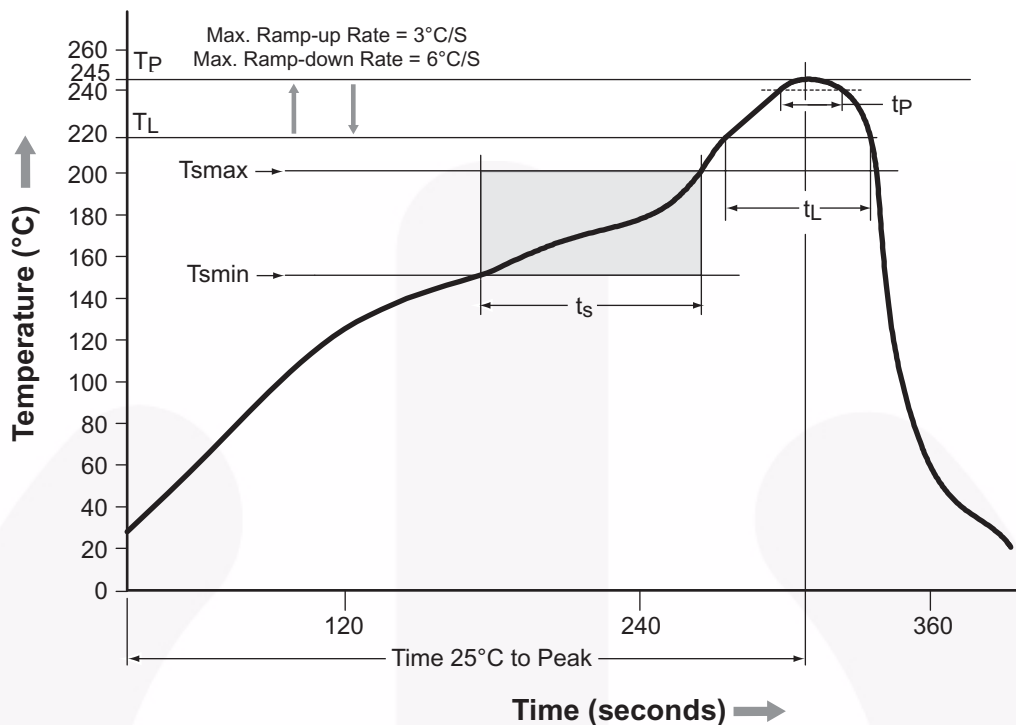
All packages are lead free per JEDEC: J-STD-020B standard.

Marking Information



| Definitions | |
|-------------|---|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | One digit year code, e.g., '8' |
| 4 | Two digit work week ranging from '01' to '53' |
| 5 | Assembly package code |

Reflow Profile



| Profile Feature | Pb-Free Assembly Profile |
|---|--------------------------|
| Temperature Min. (T _{smin}) | 150°C |
| Temperature Max. (T _{smax}) | 200°C |
| Time (t _s) from (T _{smin} to T _{smax}) | 60–120 seconds |
| Ramp-up Rate (t _L to t _p) | 3°C/second max. |
| Liquidous Temperature (T _L) | 217°C |
| Time (t _L) Maintained Above (T _L) | 60–150 seconds |
| Peak Body Package Temperature | 245°C +0°C / -5°C |
| Time (t _p) within 5°C of 245°C | 30 seconds |
| Ramp-down Rate (T _P to T _L) | 6°C/second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |



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| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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