

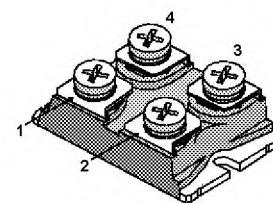
N - CHANNEL ENHANCEMENT MODE  
 POWER MOS TRANSISTOR IN ISOTOP PACKAGE

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STE50N40	400 V	< 0.075 Ω	50 A

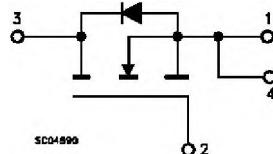
- HIGH CURRENT POWER MODULE
- AVALANCHE RUGGED TECHNOLOGY (SEE IRFP350 FOR RATING)
- VERY LARGE SOA - LARGE PEAK POWER CAPABILITY
- EASY TO MOUNT
- SAME CURRENT CAPABILITY FOR THE TWO SOURCE TERMINALS
- EXTREMELY LOW R<sub>th</sub> JUNCTION TO CASE
- VERY LOW DRAIN TO CASE CAPACITANCE
- VERY LOW INTERNAL PARASITIC INDUCTANCE (TYPICALLY < 5 nH)
- ISOLATED PACKAGE UL RECOGNIZED (FILE No E81743)

**INDUSTRIAL APPLICATIONS:**

- SMPS & UPS
- MOTOR CONTROL
- WELDING EQUIPMENT
- OUTPUT STAGE FOR PWM, ULTRASONIC CIRCUITS



ISOTOP

**INTERNAL SCHEMATIC DIAGRAM**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-Source Voltage (V <sub>GS</sub> = 0)	400	V
V <sub>DGR</sub>	Drain-Gate Voltage (R <sub>GS</sub> = 20 kΩ)	400	V
V <sub>GS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	50	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	34	A
I <sub>DM(•)</sub>	Drain Current (pulsed)	200	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	450	W
	Derating Factor	3.6	W/°C
T <sub>stg</sub>	Storage Temperature	-55 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C
V <sub>ISO</sub>	Insulation Withstand Voltage (AC-RMS)	2500	V

(•) Pulse width limited by safe operating area

# STE50N40

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## THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.27	$^{\circ}\text{C}/\text{W}$
$R_{thc-h}$	Thermal Resistance Case-heatsink With Conductive Grease Applied	Max	0.05	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$ $V_{GS} = 0 \text{ V}$	400			$\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^{\circ}\text{C}$			400 2	$\mu\text{A}$ $\text{mA}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 400$	$\text{nA}$

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$	2		4	$\text{V}$
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}$ $I_D = 30 \text{ A}$			0.075	$\Omega$

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} = 15 \text{ V}$ $I_D = 30 \text{ A}$	28			$\text{s}$
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}$ $f = 1 \text{ MHz}$ $V_{GS} = 0 \text{ V}$			12 2400 1000	$\text{nF}$ $\text{pF}$ $\text{pF}$

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Time Rise Time	$V_{DD} = 200 \text{ V}$ $I_D = 30 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 1)		80 120		$\text{ns}$ $\text{ns}$
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 320 \text{ V}$ $I_D = 50 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 3)		1000		$\text{A}/\mu\text{s}$
$Q_g$	Total Gate Charge	$V_{DD} = 320 \text{ V}$ $I_D = 50 \text{ A}$ $V_{GS} = 10 \text{ V}$		580		$\text{nC}$

**ELECTRICAL CHARACTERISTICS (continued)**  
SWITCHING OFF

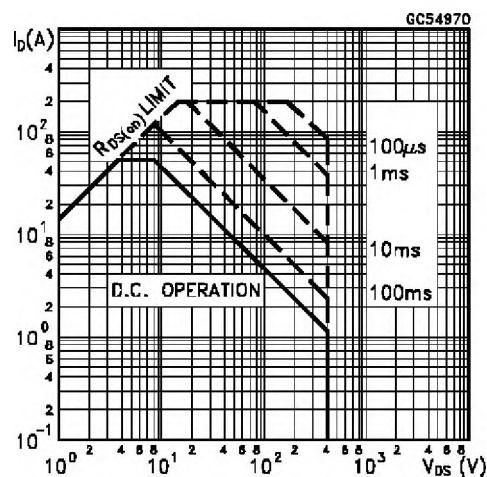
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(V_{off})}$	Off-voltage Rise Time	$V_{DD} = 320 \text{ V}$ $I_D = 50 \text{ A}$		90		ns
$t_f$	Fall Time	$R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$		40		ns
$t_c$	Cross-over Time	(see test circuit, figure 3)		135		ns

## SOURCE DRAIN DIODE

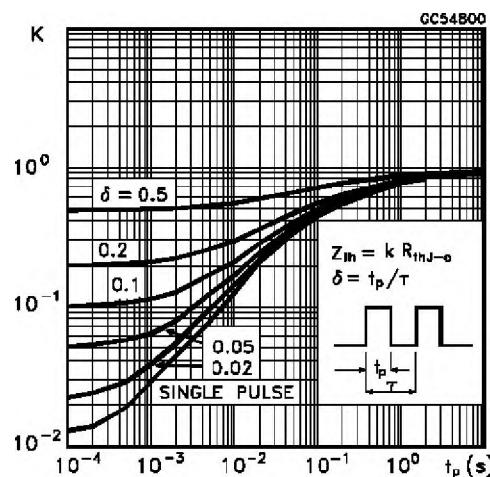
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				50	A
$I_{SDM(\bullet)}$	Source-drain Current (pulsed)				200	A
$V_{SD} (\ast)$	Forward On Voltage	$I_{SD} = 50 \text{ A}$ $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 50 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ $T_j = 150^\circ\text{C}$		980		ns
$Q_{rr}$	Reverse Recovery Charge	(see test circuit, figure 3)		31.8		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			65		A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %( $\bullet$ ) Pulse width limited by safe operating area

## Safe Operating Area

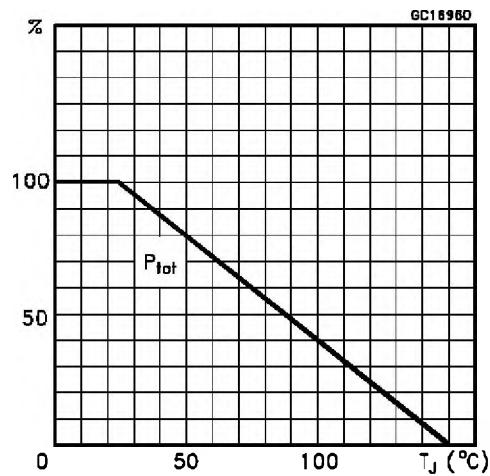


## Thermal Impedance

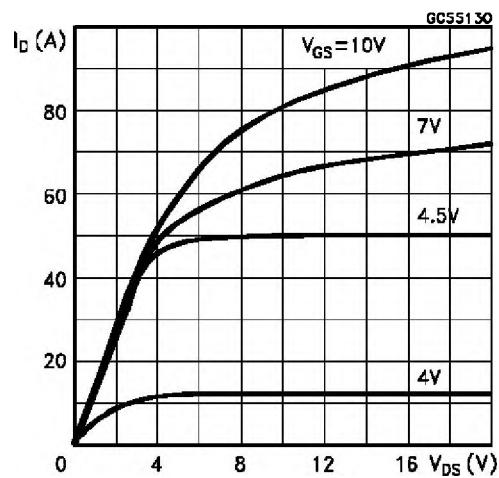


## STE50N40

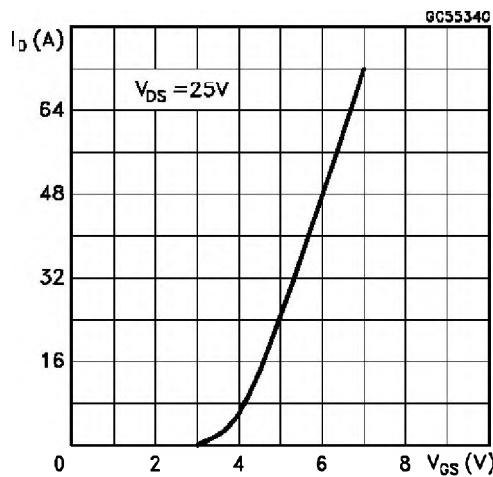
Derating Curve



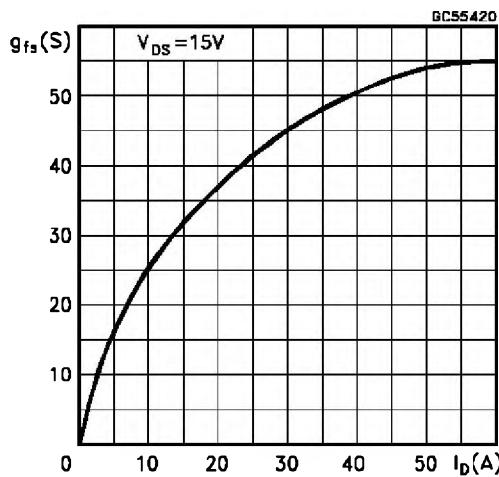
Output Characteristics



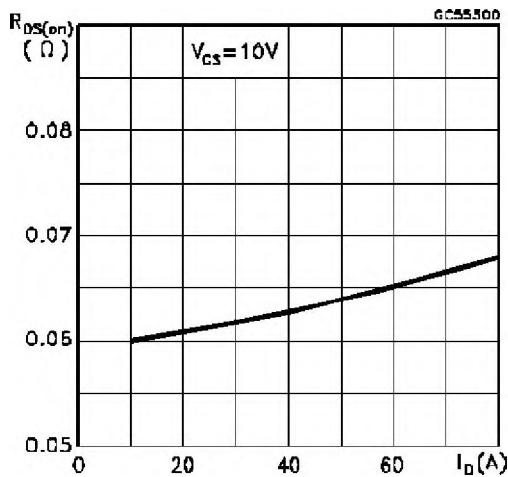
Transfer Characteristics



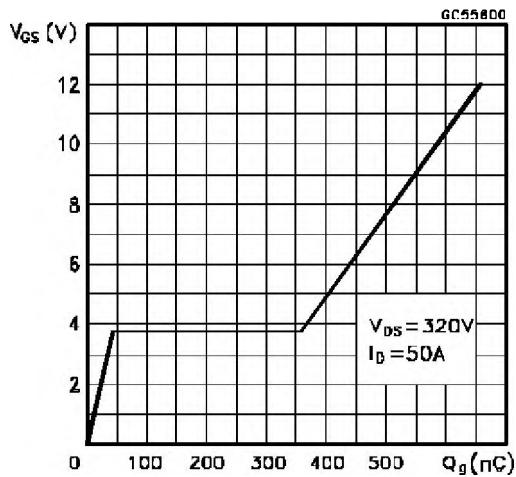
Transconductance



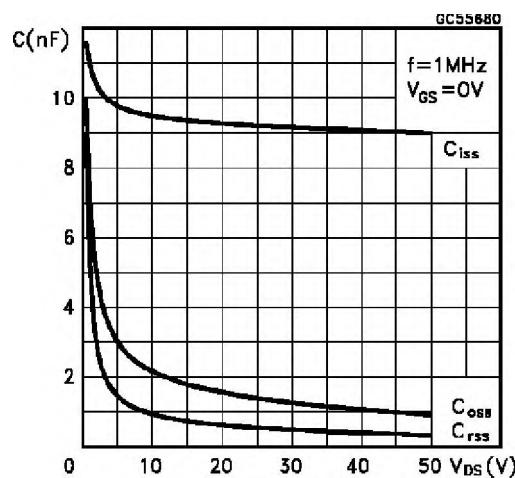
Static Drain-source On Resistance



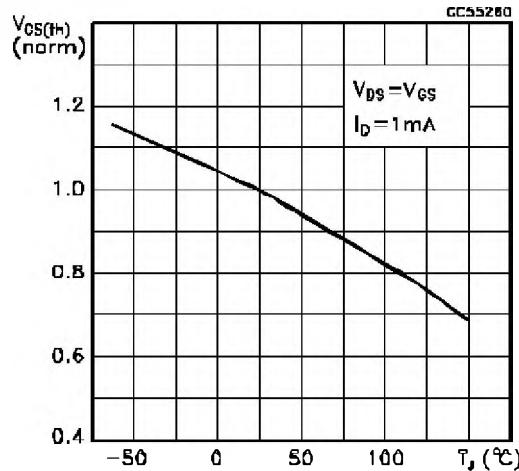
Gate Charge vs Gate-source Voltage



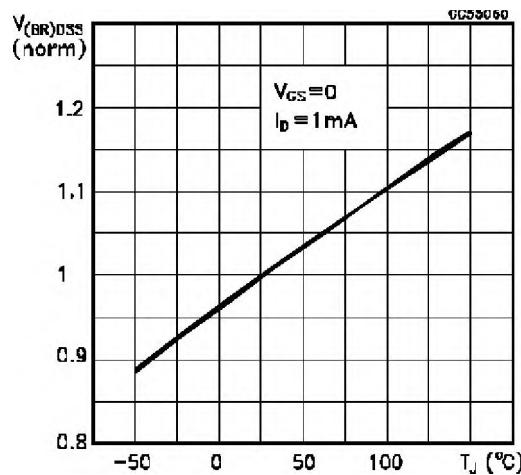
Capacitance Variations



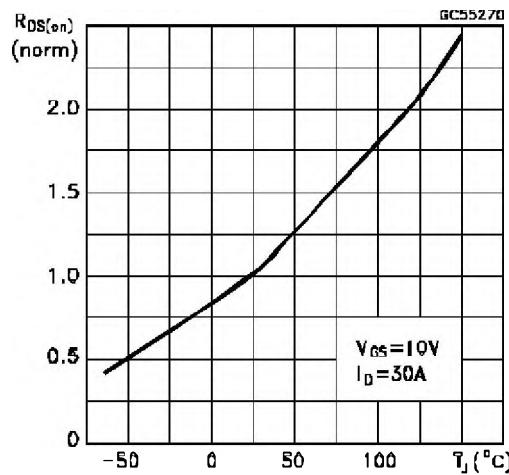
Normalized Gate Threshold Voltage vs Temperature



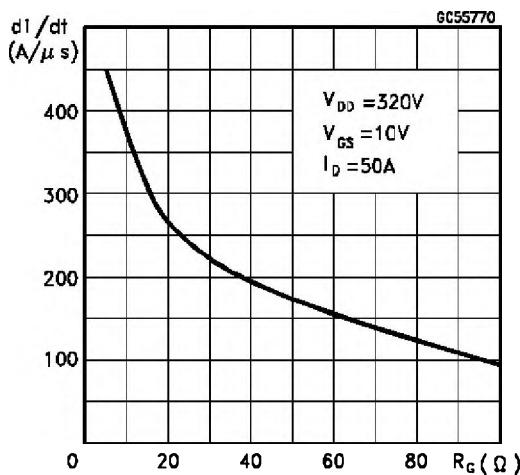
Normalized Breakdown Voltage vs Temperature



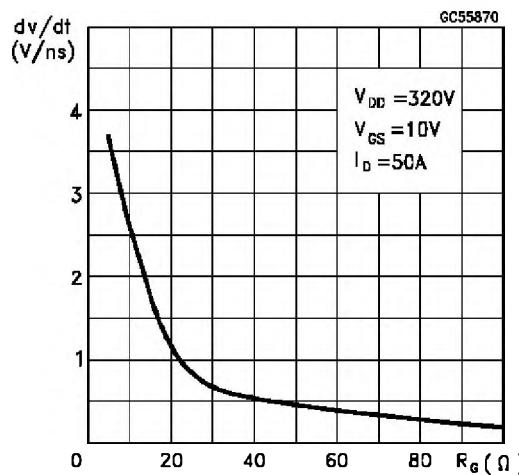
Normalized On Resistance vs Temperature



Turn-on Current Slope

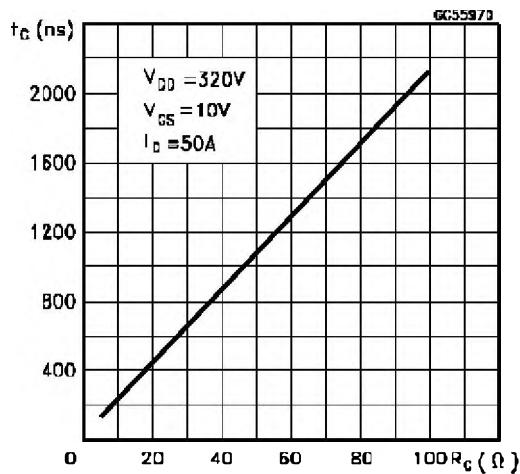


Turn-off Drain-source Voltage Slope

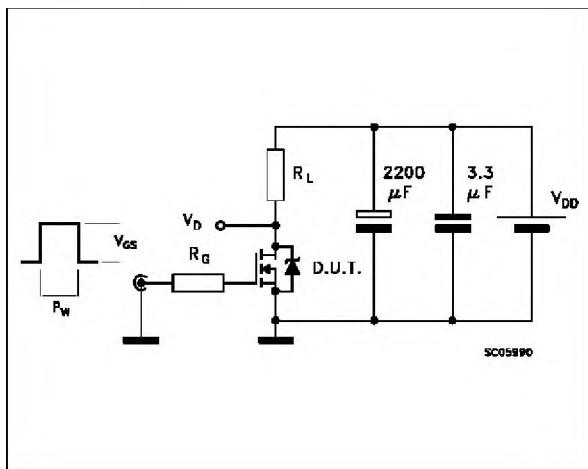


## STE50N40

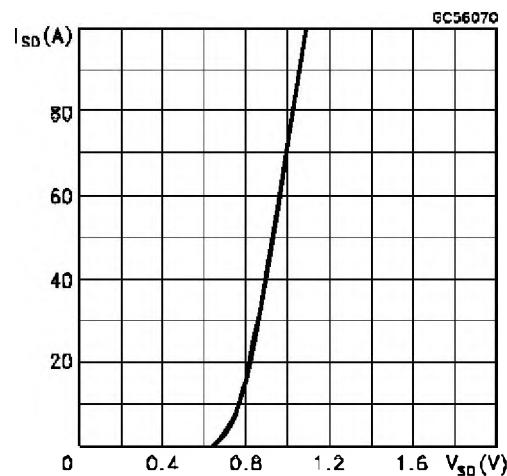
Cross-over Time



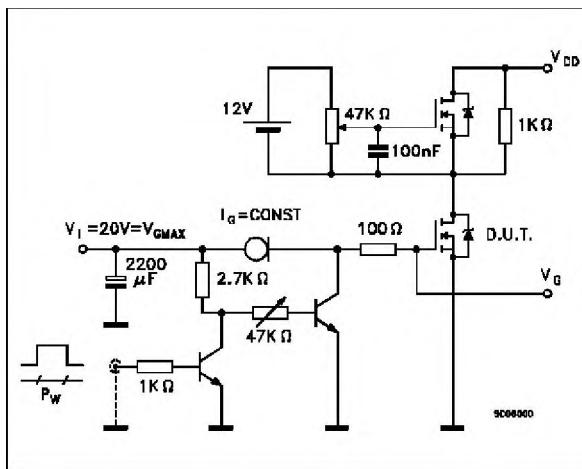
**Fig. 1:** Switching Times Test Circuits For Resistive Load



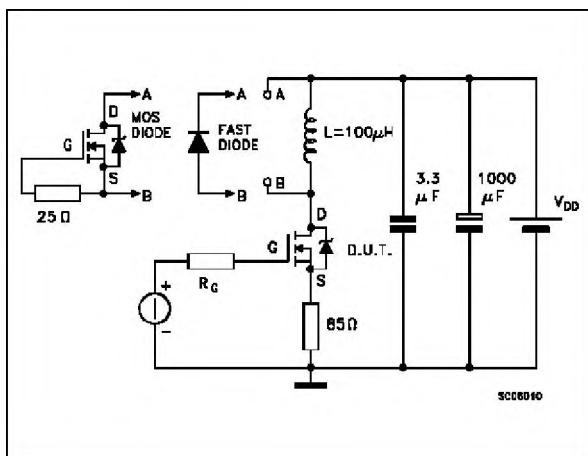
Source-drain Diode Forward Characteristics



**Fig. 2:** Gate Charge Test Circuit

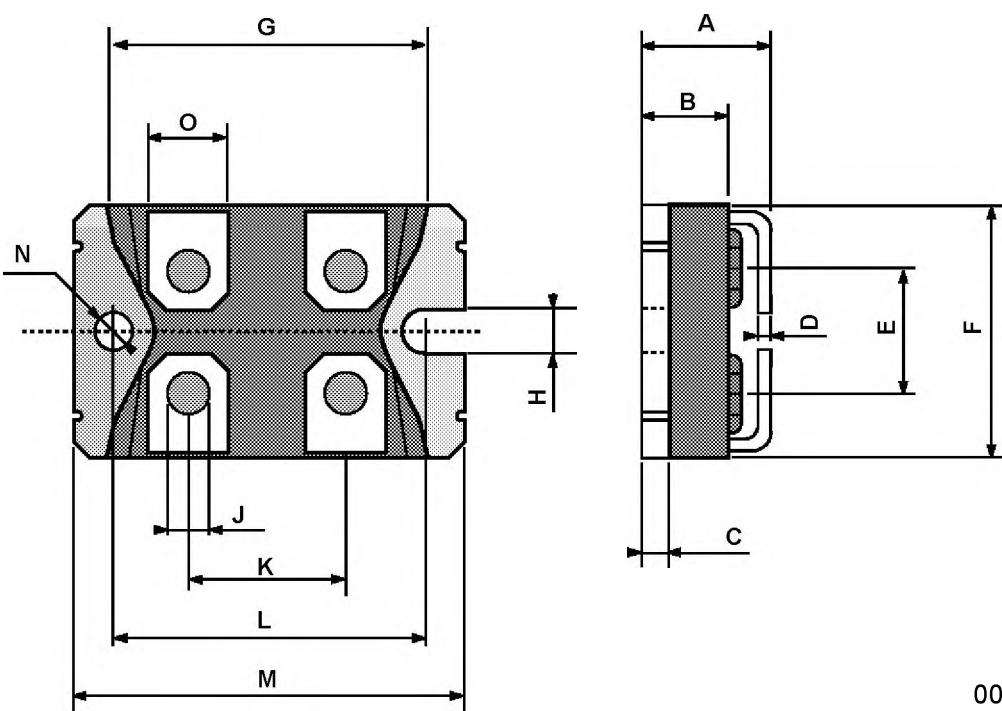


**Fig. 3:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322
P	5.5			0.216		



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