

MOS FIELD EFFECT TRANSISTOR

NP40N06CLC, NP40N06DLC, NP40N06ELC

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
 $R_{DS(on)1} = 27 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 20 \text{ A)}$
 $R_{DS(on)2} = 38 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5.0 \text{ V, } I_D = 18 \text{ A)}$
- Low C_{iss} : $C_{iss} = 1200 \text{ pF TYP.}$
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 40	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 140	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.8	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	84	W
Single Avalanche Current ^{Note2}	I_{AS}	40 / 20 / 5	A
Single Avalanche Energy ^{Note2}	E_{AS}	1.6 / 40 / 125	mJ
Repetitive Avalanche Current ^{Note3}	I_{AR}	20	A
Repetitive Avalanche Energy ^{Note3}	E_{AR}	8.4	mJ
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$

- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$
 2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$
 3. $T_{ch} \leq 175^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, Duty cycle $\leq 3\%$

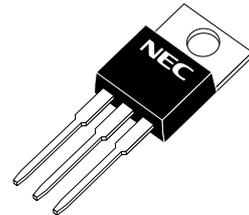
THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	1.79	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

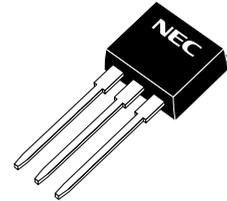
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP40N06CLC	TO-220AB
NP40N06DLC	TO-262
NP40N06ELC	TO-263

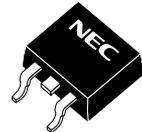
(TO-220AB)



(TO-262)



(TO-263)

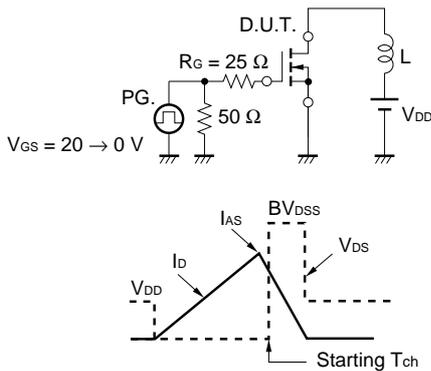


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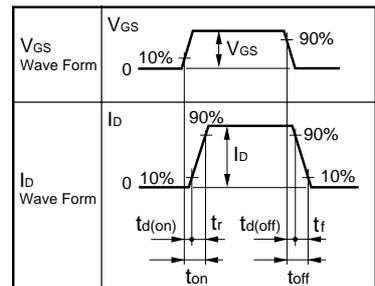
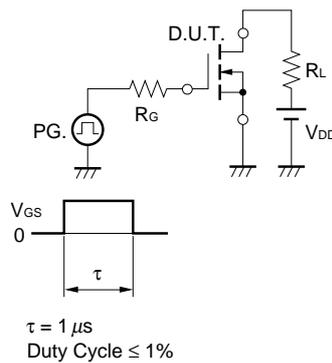
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 18 A	10	23		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 20 A		20	27	mΩ
	R _{DS(on)2}	V _{GS} = 5.0 V, I _D = 18 A		28	38	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 18 A		33	40	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		1200	2650	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		570	860	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		270	500	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 18 A		35	80	ns
Rise Time	t _r	V _{GS} = 10 V		280	700	ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		160	320	ns
Fall Time	t _f			170	430	ns
Total Gate Charge	Q _G	V _{DD} = 48 V		50	80	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		4.5		nC
Gate to Drain Charge	Q _{GD}	I _D = 35 A		22		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 35 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 35 A, V _{GS} = 0 V		70		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		130		nC

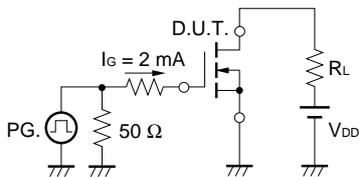
TEST CIRCUIT 1 AVALANCHE CAPABILITY



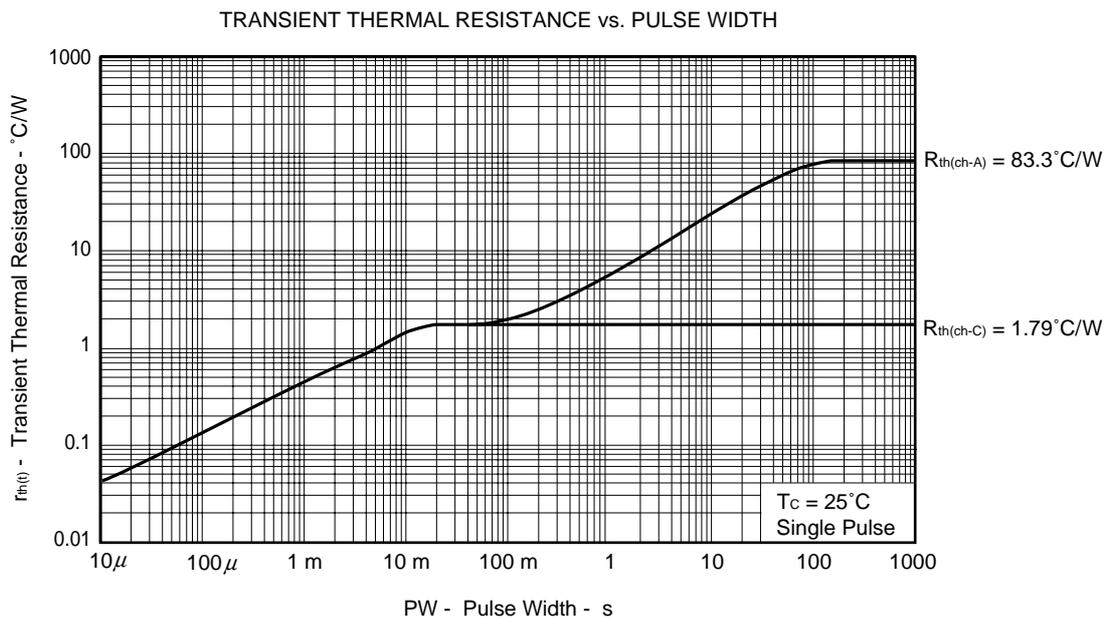
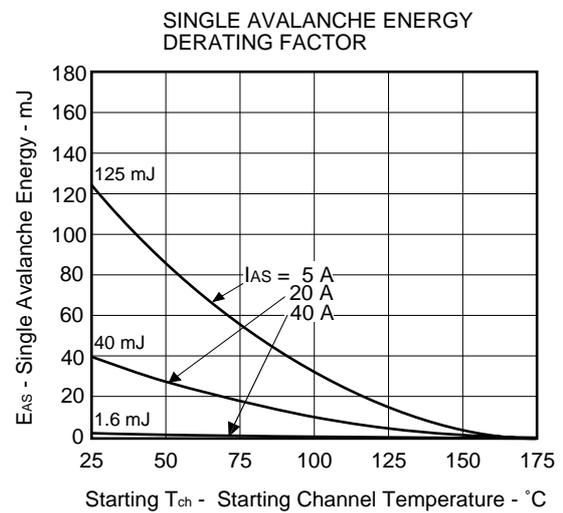
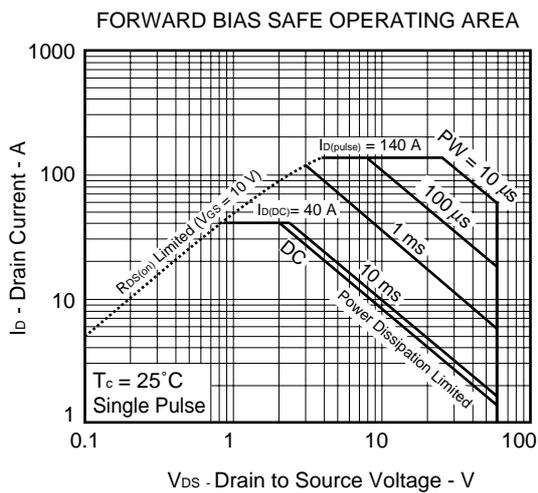
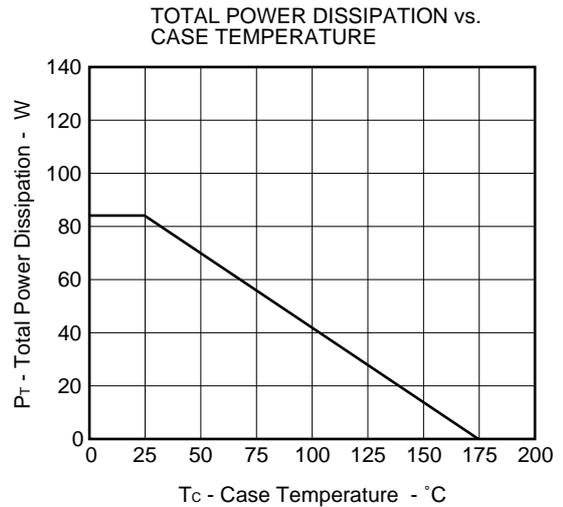
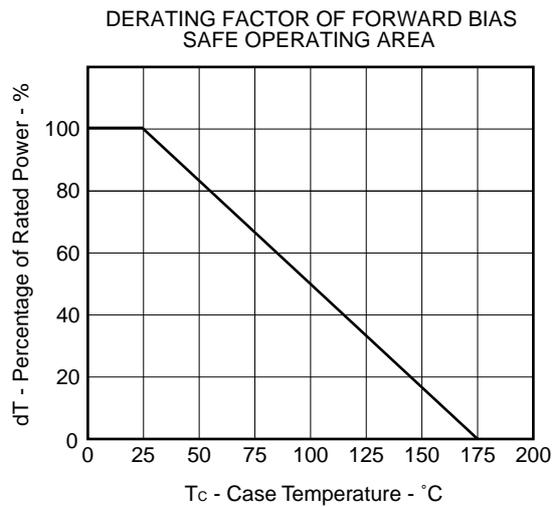
TEST CIRCUIT 2 SWITCHING TIME

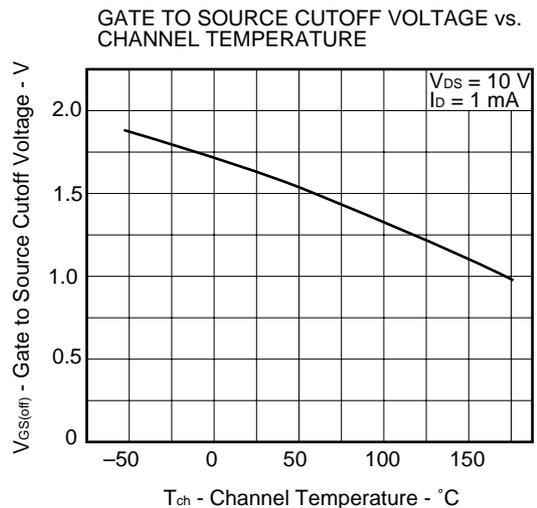
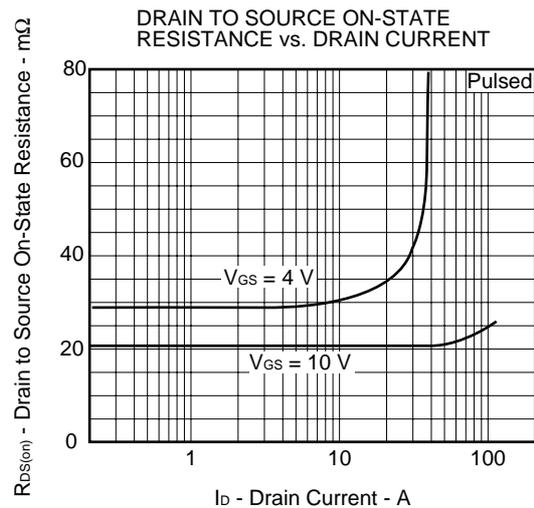
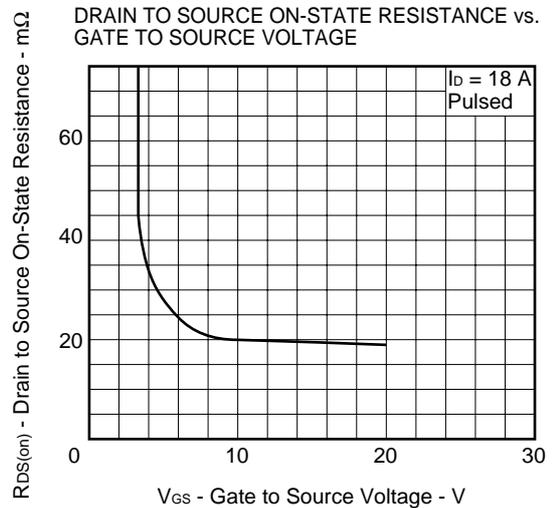
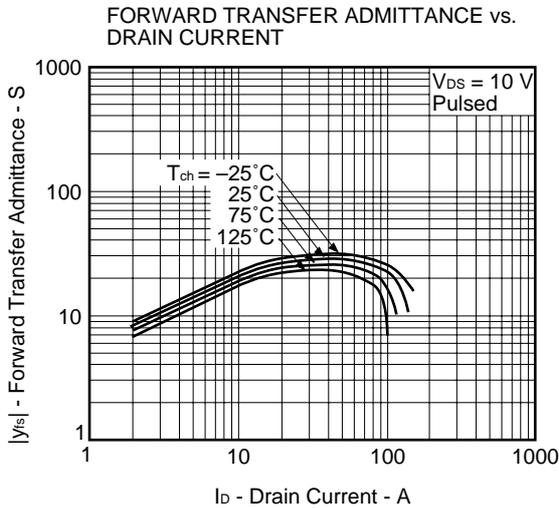
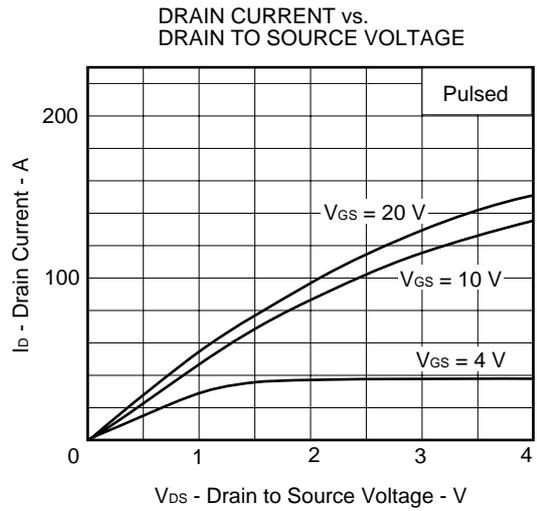
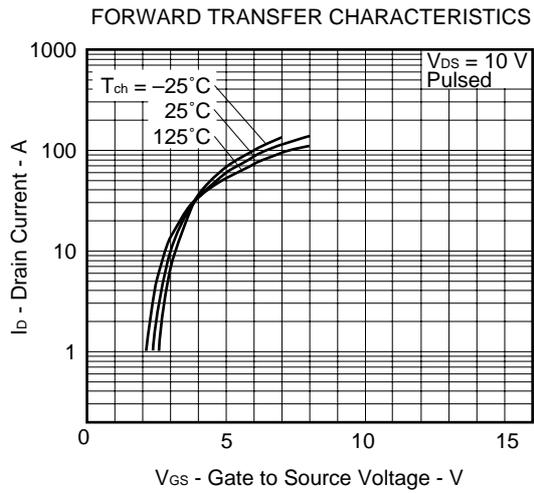


TEST CIRCUIT 3 GATE CHARGE

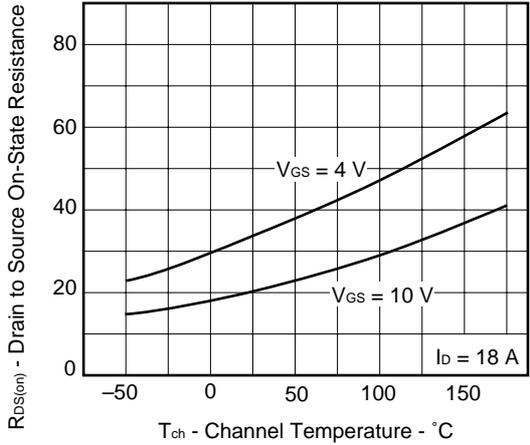


★ TYPICAL CHARACTERISTICS (T_A = 25°C)

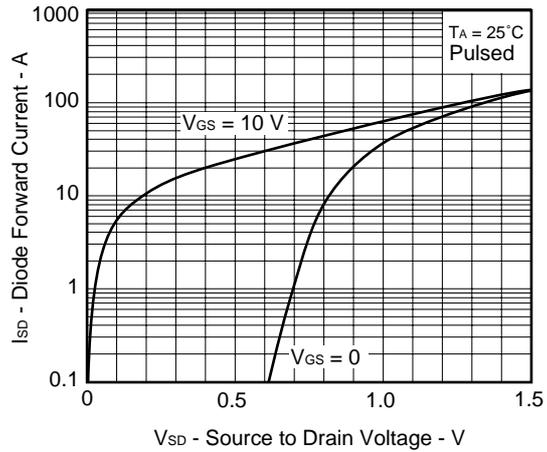




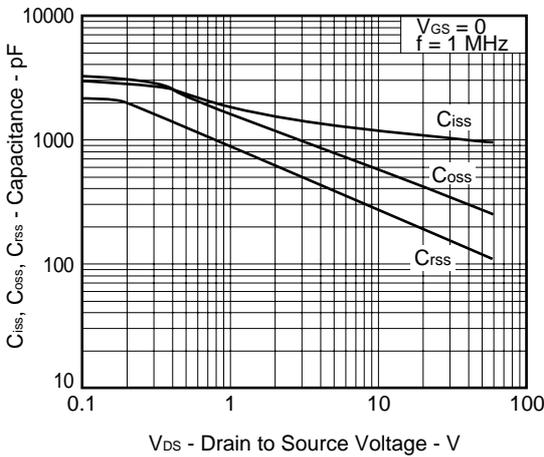
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



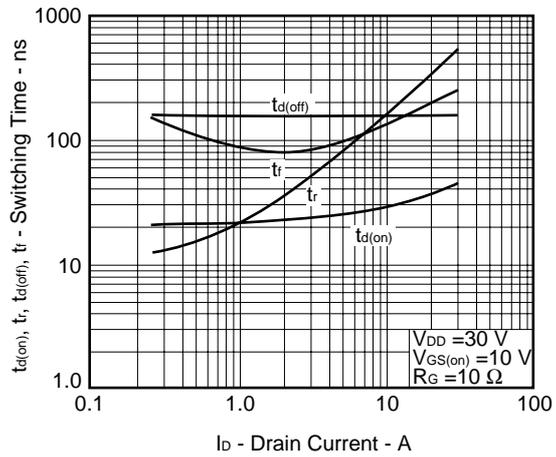
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



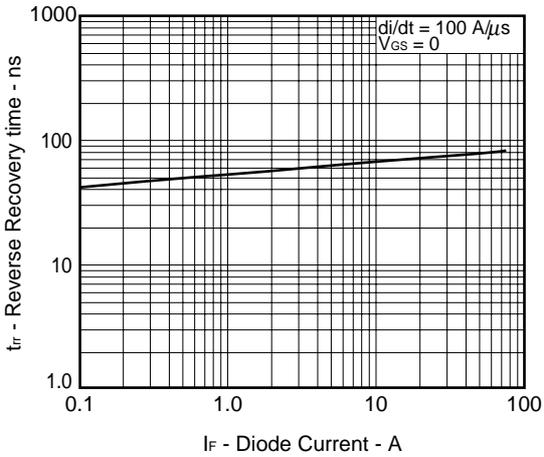
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



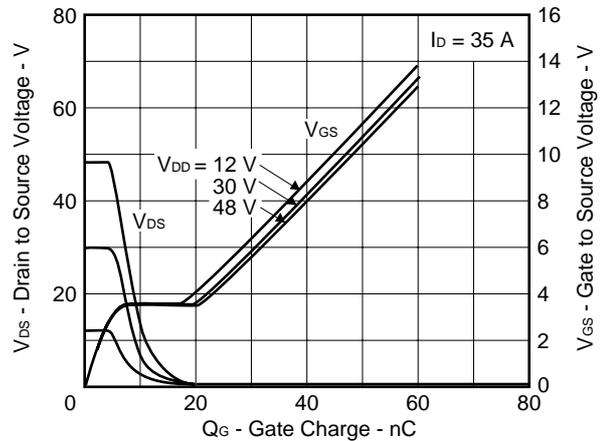
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

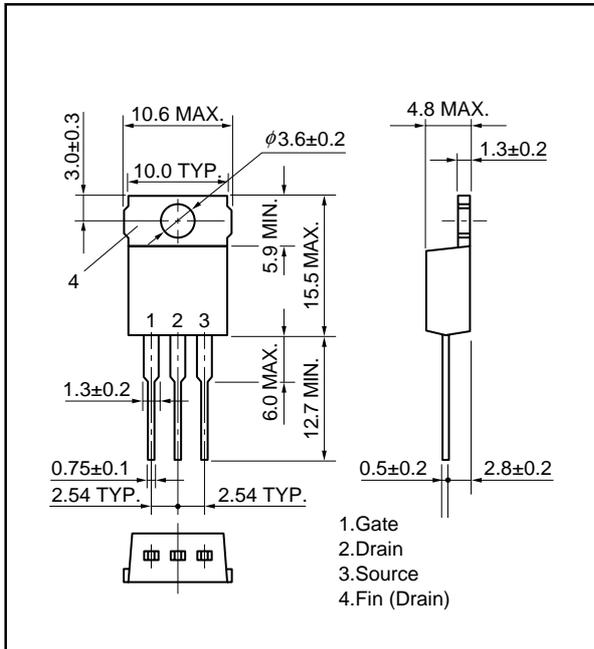


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

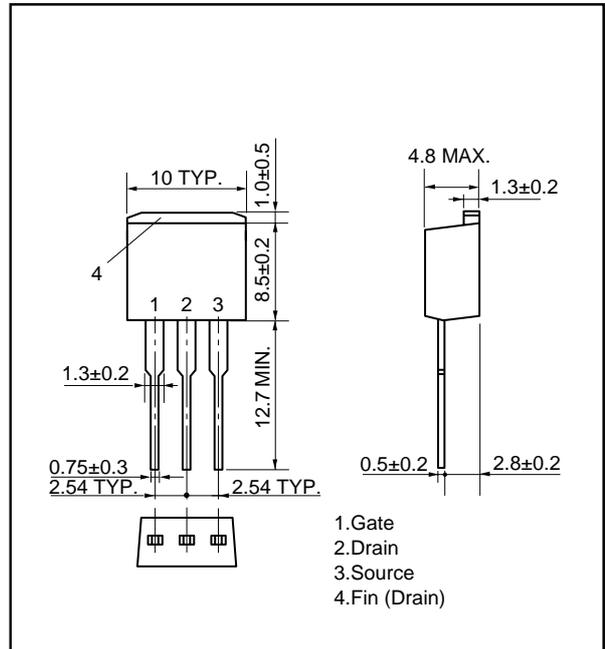


PACKAGE DRAWINGS (Unit: mm)

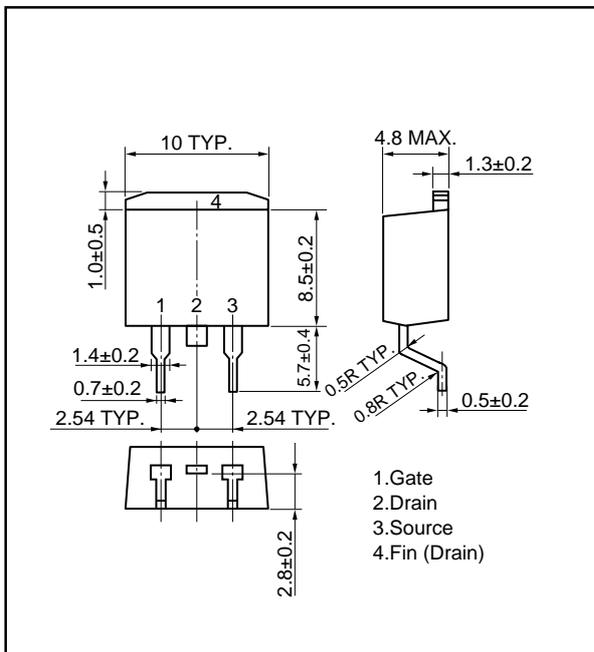
1) TO-220AB (MP-25)



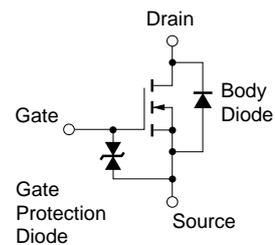
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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