PRELIMINARY DATA SHEET



SILICON POWER MOS FET NE5520379A

3.2 V OPERATION SILICON RF POWER LD-MOS FET FOR GSM/DCS DUAL-BAND PHONE TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE5520379A is an N-channel silicon power MOS FET specially designed as the transmission power amplifier for 3.2 V GSM 900 handsets. Dies are manufactured using NEC's NEWMOS technology (NEC's 0.6 μ m WSi gate lateral-diffusion MOS FET) and housed in a surface mount package. This device can deliver 34.6 dBm output power with 68% power efficiency at 915 MHz under the 2.8 V supply voltage.

FEATURES

High output power
 Pout = 35.5 dBm TYP. (VDS = 3.2 V, VGS = 2.5 V, f = 915 MHz, Pin = 25 dBm)

: $P_{out} = 33.0 \text{ dBm TYP}$. ($V_{DS} = 3.2 \text{ V}$, $V_{GS} = 2.5 \text{ V}$, f = 1.785 MHz, $P_{in} = 25 \text{ dBm}$)

• High power added efficiency : η add = 65% TYP. (VDS = 3.2 V, VGS = 2.5 V, f = 915 MHz, Pin = 25 dBm)

: $\eta_{add} = 35\%$ TYP. (VDS = 3.2 V, VGS = 2.5 V, f = 1 785 MHz, Pin = 25 dBm)

• High linear gain : $G_L = 16.0 \text{ dB TYP.}$ ($V_{DS} = 3.2 \text{ V}$, $V_{GS} = 2.5 \text{ V}$, f = 915 MHz, $P_{in} = 10 \text{ dBm}$)

: GL = 8.5 dB TYP. (VDS = 3.2 V, VGS = 2.5 V, f = 1.785 MHz, Pin = 10 dBm)

Surface mount package : 5.7 × 5.7 × 1.1 mm MAX.

Single supply : VDS = 2.8 to 3.8 V

APPLICATIONS

• Digital cellular phones : 3.2 V GSM/DCS Dual-Band handsets

Others : General purpose amplifiers for 1.6 to 2.0 GHz TDMA applications

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5520379A-T1	79A	АЗ	12 mm wide embossed tapingGate pin face the perforation side of the tapeQty 1 kpcs/reel
NE5520379A-T1A			12 mm wide embossed tapingGate pin face the perforation side of the tapeQty 5 kpcs/reel

Remark To order evaluation samples, consult your NEC sales representative.

Part number for sample order: NE5520379A

Caution Please handle this device at static-free workstation, because this is an electrostatic sensitive device.

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ABSOLUTE MAXIMUM RATINGS (TA = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	Vos	6.0	V
Gate to Source Voltage	Vgso	5.0	V
Drain Current	ΙD	1.5	Α
Drain Current (Pulse Test)	ID Note	3.0	Α
Total Power Dissipation	Ptot	1.6	W
Channel Temperature	Tch	125	°C
Storage Temperature	Tstg	−65 to +125	°C

Note Duty Cycle \leq 50%, Ton \leq 1 ms

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	VDS		2.8	3.2	3.8	٧
Gate to Source Voltage	Vgso		0	2.5	3.5	V
Drain Current (Pulse Test)	ΙD	Duty Cycle ≤ 50%, Ton ≤ 1 ms	1	1.75	2.0	Α
Input Power	Pin	f = 1.8 GHz, V _{DS} = 3.6 V	24	25	26	dBm



ELECTRICAL CHARACTERISTICS (TA = +25°C)

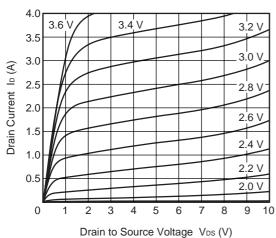
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	Igso	Vess = 5.0 V	=	-	100	nA
Saturated Drain Current (Zero Gate Voltage Drain Current)	Ipss	V _{DSS} = 6.0 V	_	_	100	nA
Gate Threshold Voltage	Vth	V _{DS} = 3.5 V, I _{DS} = 1 mA	1.0	1.35	2.0	V
Transconductance	g _m	V _{DS} = 3.5 V, I _{DS} = 0.8 to 1.0 A	-	2.5	-	S
Drain to Source Breakdown Voltage	BVps	loss = $10 \mu A$	15	20	_	V
Thermal Resistance	Rth	Channel to Case	=	_	5	°C/W
Linear Gain	G∟	$f = 915 \text{ MHz}, P_{in} = 10 \text{ dBm}, \\ V_{DS} = 3.2 \text{ V}, V_{GS} = 2.5 \text{ V}, \textbf{Note}$	-	16.0	-	dB
Output Power	Pout	f = 915 MHz, Pin = 25 dBm,	=	35.5	-	dBm
Operating Current	lop	V _{DS} = 3.2 V, V _{GS} = 2.5 V, Note	-	1 000	-	mA
Drain Efficiency	$\eta_{ extsf{d}}$		-	68	-	%
Power Added Efficiency	η add		_	65	_	%
Linear Gain	G∟	$f = 1 \ 785 \ MHz, \ P_{in} = 10 \ dBm,$ $V_{DS} = 3.2 \ V, \ V_{GS} = 2.5 \ V, \ \textbf{Note}$	-	8.5	-	dB
Output Power	Pout	f = 1 785 MHz, Pin = 25 dBm,	31.0	33.0	-	dBm
Operating Current	lop	V _{DS} = 3.2 V, V _{GS} = 2.5 V, Note	_	750	-	mA
Drain Efficiency	$\eta_{ extsf{d}}$		29	38	-	%
Power Added Efficiency	η add		-	35	-	%

Note DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

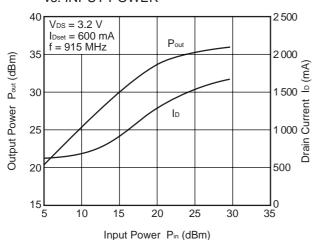
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TYPICAL CHARACTERISTICS (TA = +25°C)

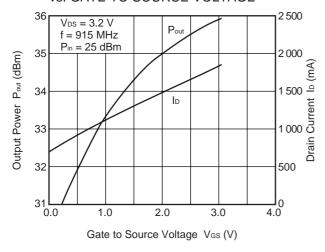




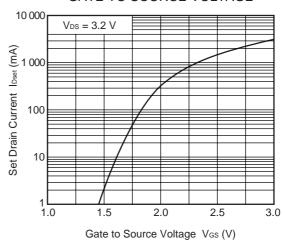
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



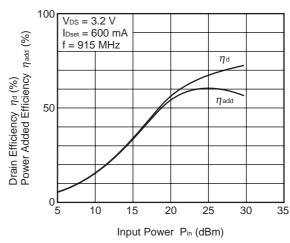
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



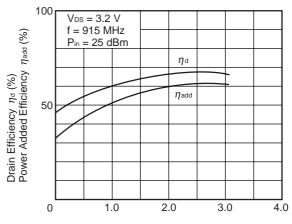
SET DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE

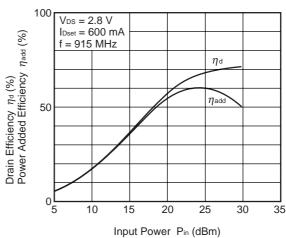


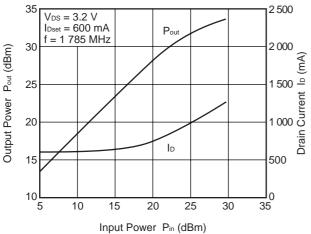
Gate to Source Voltage Vgs (V)



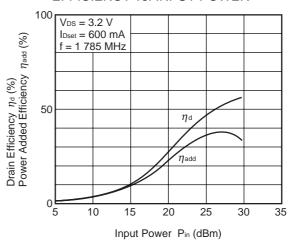
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER 2 500 $V_{DS} = 2.8 \text{ V}$ $I_{Dset} = 600 \text{ mA}$ = 915 MHz 30 2 000 Output Power Pout (dBm) (mA) 1 000 1 000 Drain Current lo (r 25 20 lь 500 15 **_**ე 35 10 15 20 25 30 5 Input Power Pin (dBm) **OUTPUT POWER, DRAIN CURRENT** vs. INPUT POWER 2 500 35 V_{DS} = 3.2 V $I_{Dset} = 600 \text{ mA}$ Pout



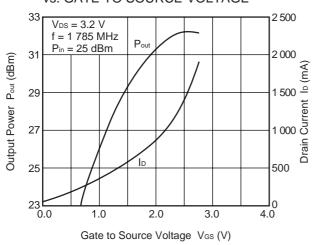




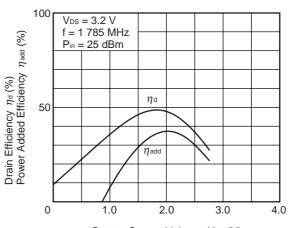
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE

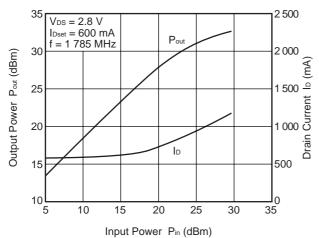


DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE

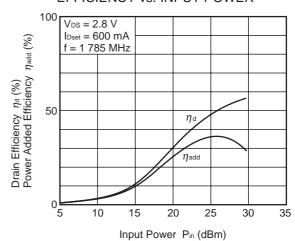


Gate to Source Voltage Vgs (V)

OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

Test Conditions: VDS = 3.5 V, IDS = 300 mA	Test Co	nditions:	$V_{DS} = 3.5$	V.	lps =	300 r	nΑ
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Frequency	9	S ₁₁	S	21	S	12	S	22	MAG Note	MSG Note	K
GHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	dB	dB	
0.1	0.91	-166.0	4.96	91.5	0.02	2.8	0.87	-177.5		24.8	0.12
0.2	0.91	-174.2	2.48	82.3	0.02	-4.8	0.87	-179.7		21.7	0.24
0.3	0.92	-177.5	1.63	75.6	0.02	-9.0	0.87	-179.1		19.8	0.37
0.4	0.92	-179.6	1.20	69.7	0.02	-14.4	0.88	-178.3		18.7	0.50
0.5	0.92	178.8	0.94	64.1	0.02	-18.7	0.88	177.4		17.8	0.63
0.6	0.92	177.4	0.77	58.9	0.01	-19.7	0.88	176.6		17.3	0.87
0.7	0.93	176.1	0.64	53.8	0.01	-24.7	0.89	175.6		16.4	0.93
0.8	0.93	174.9	0.54	49.3	0.01	-27.0	0.89	174.8	14.0		1.12
0.9	0.93	173.6	0.47	44.9	0.01	-29.5	0.90	173.9	12.2		1.33
1.0	0.94	172.4	0.41	40.7	0.01	-31.7	0.90	173.0	10.8		1.61
1.1	0.95	171.2	0.37	36.9	0.01	-33.5	0.91	172.1	9.9		1.85
1.2	0.95	170.0	0.32	33.1	0.01	-35.3	0.91	171.1	9.0		2.08
1.3	0.95	168.9	0.28	29.6	0.01	-38.7	0.91	170.2	8.1		2.43
1.4	0.95	167.7	0.25	26.3	0.01	-40.1	0.91	169.1	7.2		2.88
1.5	0.95	166.6	0.23	23.2	0.01	-40.3	0.92	168.1	6.6		3.31
1.6	0.95	165.5	0.21	20.2	0.01	-42.1	0.92	167.2	5.9		4.05
1.7	0.95	164.3	0.19	17.6	0.01	-41.5	0.92	166.4	5.1		4.91
1.8	0.96	163.3	0.17	15.0	0.00	-41.4	0.92	165.4	4.4		5.68
1.9	0.96	162.2	0.16	12.6	0.00	-40.2	0.93	164.4	3.8		7.09
2.0	0.96	161.2	0.14	10.4	0.00	-35.5	0.93	163.6	3.5		8.29
2.1	0.96	160.1	0.13	8.4	0.00	-30.1	0.93	162.8	2.9		11.07
2.2	0.96	159.2	0.12	6.5	0.00	-21.3	0.93	161.9	2.2		14.89
2.3	0.96	158.3	0.11	4.6	0.00	-15.3	0.94	161.0	1.7		16.85
2.4	0.96	157.4	0.11	3.1	0.00	-2.0	0.94	160.2	1.6		18.02
2.5	0.96	156.5	0.10	1.9	0.00	9.5	0.95	159.6	1.5		16.22
2.6	0.97	155.7	0.09	0.7	0.00	17.4	0.95	158.9	1.0		18.87
2.7	0.97	154.9	0.09	-0.8	0.00	49.6	0.95	158.0	0.6		17.17
2.8	0.97	154.2	0.08	-2.1	0.00	54.6	0.95	157.2	8.0		17.91
2.9	0.97	153.4	0.08	-3.3	0.00	75.7	0.96	156.6	0.9		11.30
3.0	0.97	152.7	0.07	-4.0	0.00	84.8	0.96	155.9	0.7		12.00

$$\begin{aligned} \textbf{Note} \ \ & \text{When K} \geq 1 \text{, the MAG (Maximum Available Gain) is used.} \qquad \text{MAG} = \left| \frac{S_{21}}{S_{12}} \right| \left(\mathsf{K} - \sqrt{\left(\mathsf{K}^2 - 1 \right)} \, \right) \\ & \text{When K} < 1 \text{, the MSG (Maximum Stable Gain) is used.} \qquad \text{MSG} = \left| \frac{S_{21}}{S_{12}} \right| \text{, K} = \frac{1 + \left| \Delta \right|^2 - \left| S_{11} \right|^2 - \left| S_{22} \right|^2}{2 \cdot \left| S_{12} \right| \cdot \left| S_{21} \right|}, \end{aligned}$$

 $\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$

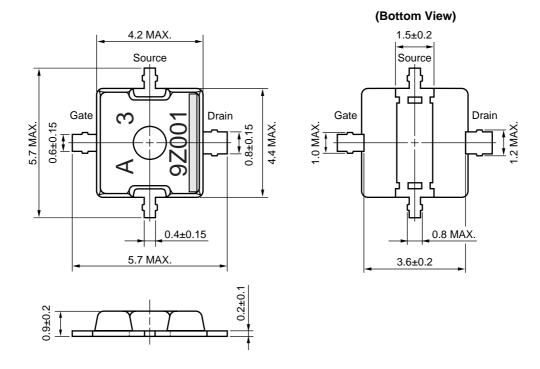
LARGE SIGNAL IMPEDANCE (VDS = 3.2 V, IDset = 600 mA, Pin = 25 dBm)

f (MHz)	$Z_{in}\left(\Omega\right)$	$Z_OL\left(\Omega ight)^Note$
1 785	TBD	TBD

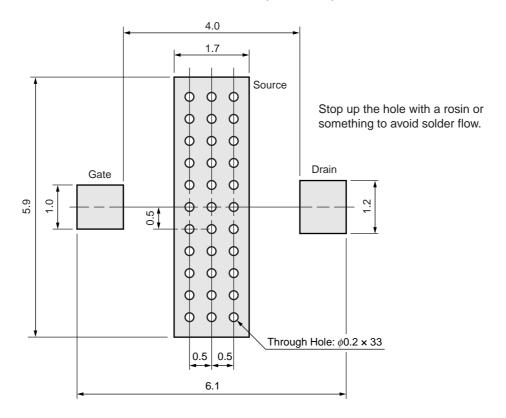
Note ZoL is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)





RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below, Time: 30 seconds or less (at 210°C or higher), Count: 2 times or less, Exposure: limit: None Note	IR35-00-2
Partial Heating	Pin temperature: 260°C or below, Time: 5 seconds or less (per pin row) Exposure: limit: None Note	-

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

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NEC NE5520379A

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