PRELIMINARY DATA SHEET



SILICON POWER MOS FET NE5500479A

3.5 V OPERATION SILICON RF POWER LD-MOS FET FOR 900 MHz 1 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE5500479A is an N-channel silicon power MOS FET specially designed as the transmission power amplifier for cellular handsets. Dies are manufactured using NEC's NEWMOS technology (NEC's $0.6~\mu m$ WSi gate lateral-diffusion MOS FET) and housed in a surface mount package. The device can deliver 31.5 dBm output power with 62% power added efficiency at 900 MHz as AMPS final output stage amplifier under the 3.5 V supply voltage. It also can deliver 35 dBm output power with 62% power added efficiency at 4.8 V, as GSM 900 class 4 final stage amplifiers.

FEATURES

High output power : Pout = 31.5 dBm TYP. (VDS = 3.5 V, IDset = 300 mA, f = 900 MHz, Pin = 20 dBm)
 High power added efficiency : ηadd = 62% TYP. (VDS = 3.5 V, IDset = 300 mA, f = 900 MHz, Pin = 20 dBm)
 High linear gain : GL = 15.0 dB TYP. (VDS = 3.5 V, IDset = 300 mA, f = 900 MHz, Pin = 10 dBm)

Surface mount package : 5.7 × 5.7 × 1.1 mm MAX.
 Single supply : Vps = 3.0 to 6.0 V

APPLICATIONS

• Analog cellular phones : 3.5 V AMPS handsets

• Digital cellular phones : 4.8 V GSM 900 class 4 handsets

Others : General purpose amplifiers for 800 to 1 000 MHz TDMA applications

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5500479A-T1	79A	R4	12 mm wide embossed tapingGate pin face the perforation side of the tapeQty 1 kpcs/reel

Remark To order evaluation samples, consult your NEC sales representative.

Part number for sample order: NE5500479A

Caution Please handle this device at static-free workstation, because this is an electrostatic sensitive device.

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ABSOLUTE MAXIMUM RATINGS (TA = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	Vos	8.5	V
Gate to Source Voltage	Vgso	5.0	V
Drain Current	ΙD	1.0	Α
Drain Current (Pulse Test)	ID Note	2.0	Α
Total Power Dissipation	Ptot	1.6	W
Channel Temperature	Tch	125	°C
Storage Temperature	Tstg	-65 to +125	°C

Note Duty Cycle \leq 50%, Ton \leq 1 ms

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	VDS		3.0	3.5	6.0	V
Gate to Source Voltage	Vgso		0	2.0	3.5	V
Drain Current	lσ			600	700	mA
Input Power	Pin	f = 900 MHz, Vps = 3.5 V	18	20	22	dBm

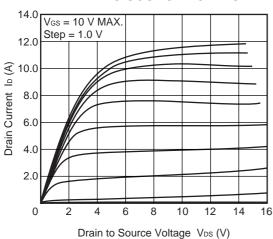
ELECTRICAL CHARACTERISTICS (TA = +25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	Igso	Vgss = 5.0 V	-	-	100	nA
Saturated Drain Current (Zero Gate Voltage Drain Current)	loss	V _{DSS} = 8.5 V	-	-	100	nA
Gate Threshold Voltage	Vth	V _{DS} = 4.8 V, I _{DS} = 1 mA	1.0	1.35	2.0	V
Transconductance	g m	V _{DS} = 4.8 V, I _{DS} = 600 mA	-	1.43	-	S
Drain to Source Breakdown Voltage	BV _{DS}	$loss = 10 \mu A$	20	24	-	V
Thermal Resistance	Rth	Channel to Case	1	10	-	°C/W
Linear Gain	G∟	$f = 900 \; \text{MHz}, \; P_{\text{in}} = 10 \; \text{dBm}, \\ V_{\text{DS}} = 3.5 \; \text{V}, \; I_{\text{Dset}} = 300 \; \text{mA}, \; \textbf{Note}$	-	15.0	-	dB
Output Power	Pout	f = 900 MHz, Pin = 20 dBm,	30.5	31.5	-	dBm
Operating Current	lop	V _{DS} = 3.5 V, I _{Dset} = 300 mA, Note	-	600	-	mA
Power Added Efficiency	η add		55	62	_	%

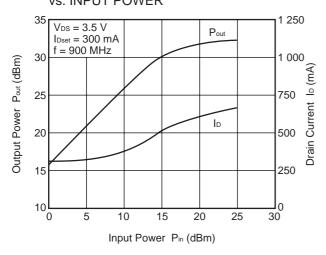
Note DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

TYPICAL CHARACTERISTICS (TA = +25°C)

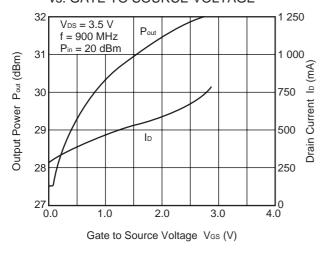
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



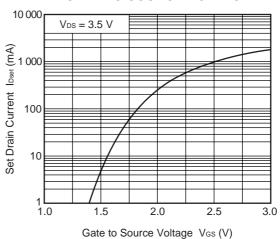
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



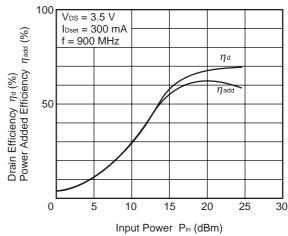
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



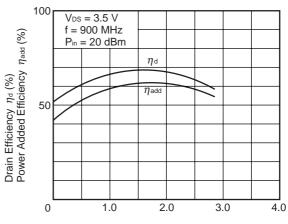
SET DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



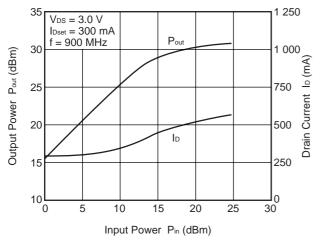
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



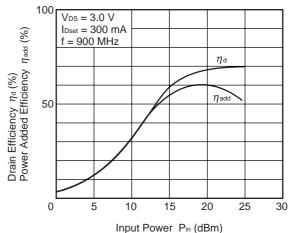
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



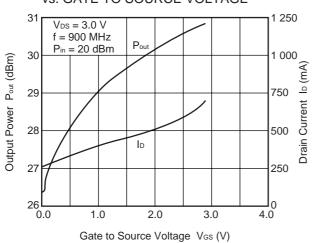
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



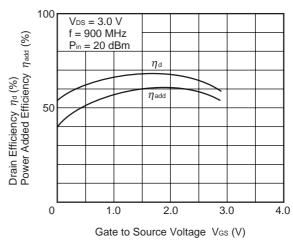
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



Remark The graphs indicate nominal characteristics.



S-PARAMETERS

Test Conditions: VDS = 3.5 V, IDset = 400 mA

Frequency	S	S ₁₁		S ₂₁			S 12		S	S ₂₂	MAG Note	MSG Note	K
GHz	MAG.	ANG.	dB	MAG.	ANG.	dB	MAG.	ANG.	MAG.	ANG.	dB	dB	
0.1	0.873	-151.3	19.2	9.13	98.9	-33.2	0.022	11.2	0.850	-172.8		26.2	
0.2	0.859	-166.3	13.3	4.65	87.0	-33.2	0.022	0.7	0.858	-177.0		23.3	
0.3	0.859	-171.8	9.7	3.05	81.5	-32.8	0.023	-3.5	0.871	-178.4		21.2	
0.4	0.857	-174.6	7.0	2.24	75.8	-33.6	0.021	-8.4	0.869	-179.5		20.3	
0.5	0.858	-176.5	5.1	1.79	71.2	-33.6	0.021	-12.0	0.883	179.5		19.3	0.03
0.6	0.864	-178.2	3.2	1.44	67.3	-34.0	0.020	-14.6	0.884	179.0		18.6	0.21
0.7	0.870	-179.3	1.8	1.23	63.2	-34.4	0.019	-13.6	0.891	178.4		18.1	0.31
0.8	0.886	179.2	0.3	1.04	59.8	-35.4	0.017	-16.5	0.895	177.6		17.9	0.43
0.9	0.890	178.1	-0.7	0.92	55.8	-35.9	0.016	-19.3	0.908	177.0		17.6	0.44
1.0	0.903	176.3	-1.8	0.81	52.9	-35.9	0.016	-19.2	0.924	175.4		17.0	0.21
1.1	0.915	174.0	-2.7	0.73	48.2	-37.1	0.014	-27.6	0.934	174.0		17.2	0.17
1.2	0.911	172.0	-3.9	0.64	45.9	-37.1	0.014	-19.3	0.922	172.1		16.6	0.59
1.3	0.905	170.6	-4.9	0.57	41.3	-38.4	0.012	-22.5	0.915	171.2	13.3		1.33
1.4	0.902	169.2	-5.7	0.52	39.6	-39.2	0.011	-21.5	0.917	169.9	11.7		1.77
1.5	0.902	167.8	-6.6	0.47	36.0	-39.2	0.011	-24.3	0.919	169.2	10.6		1.98
1.6	0.905	166.3	-7.3	0.43	35.0	-40.9	0.009	-25.7	0.917	167.6	9.3		2.89
1.7	0.904	164.4	-8.4	0.38	32.1	-41.9	0.008	-18.7	0.912	166.8	7.5		4.24
1.8	0.914	162.8	-8.9	0.36	29.4	-43.1	0.007	-9.0	0.927	164.6	8.4		3.75
1.9	0.905	160.4	-9.6	0.33	26.6	-44.4	0.006	-15.5	0.925	163.4	6.8		5.76
2.0	0.910	158.7	-9.9	0.32	24.9	-43.1	0.007	0.1	0.928	162.0	7.1		4.48
2.1	0.910	155.6	-11.1	0.28	22.8	-50.5	0.003	11.1	0.922	160.2	5.1		14.50
2.2	0.910	154.2	-11.7	0.26	21.1	-48.0	0.004	12.7	0.926	158.4	4.7		10.94
2.3	0.912	152.2	-12.8	0.23	17.5	-46.0	0.005	39.4	0.925	156.3	3.8		9.72
2.4	0.909	149.7	-12.4	0.24	16.4	-43.1	0.007	37.7	0.936	154.4	4.9		5.56
2.5	0.911	147.5	-13.6	0.21	14.4	-46.0	0.005	48.9	0.923	152.8	2.8		11.15
2.6	0.916	145.3	-13.6	0.21	13.7	-44.4	0.006	43.4	0.928	150.7	3.4		8.02
2.7	0.909	143.2	-15.4	0.17	12.5	-41.9	0.008	73.4	0.917	148.4	0.6		9.33
2.8	0.911	141.1	-14.9	0.18	8.5	-41.9	0.008	68.2	0.939	146.4	2.7		6.13
2.9	0.917	138.9	-15.9	0.16	8.9	-40.0	0.010	76.4	0.925	145.0	1.0		6.33
3.0	0.917	137.1	-16.5	0.15	8.3	-40.0	0.010	68.2	0.935	143.2	1.1		5.81

Note When K \geq 1, the MAG (Maximum Available Gain) is used. $MAG = \left| \frac{S_{21}}{S_{12}} \right| \left(K - \sqrt{\left(K^2 - 1 \right)} \right)$ When K < 1, the MSG (Maximum Stable Gain) is used. $MSG = \left| \frac{S_{21}}{S_{12}} \right|, K = \frac{1 + \left| \Delta \right|^2 - \left| S_{11} \right|^2 - \left| S_{22} \right|^2}{2 \cdot \left| S_{12} \right| \cdot \left| S_{21} \right|},$

 $\Delta = \mathsf{S}_{11} \cdot \mathsf{S}_{22} - \mathsf{S}_{21} \cdot \mathsf{S}_{12}$

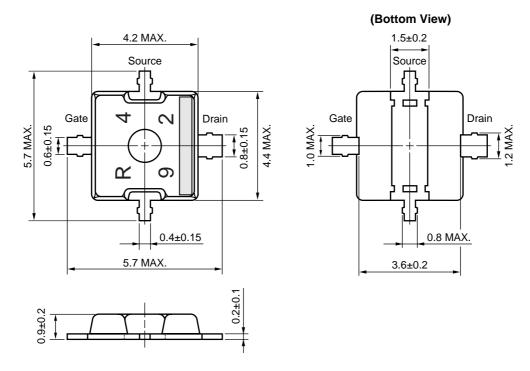
LARGE SIGNAL IMPEDANCE (VDS = 3.5 V, IDset = 300 mA, Pin = 20 dBm)

f (MHz)	$Z_{in}(\Omega)$	Z ol $(\Omega)^{Note}$		
900	TBD	TBD		

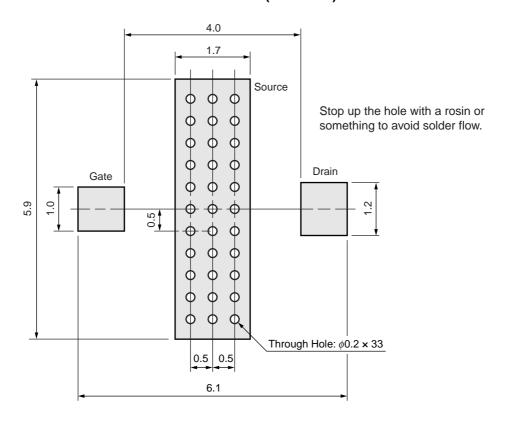
Note ZoL is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)





RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below, Time: 30 seconds or less (at 210°C or higher), Count: 2 times or less, Exposure: limit: None Note	IR35-00-2
Partial Heating	Pin temperature: 260°C or below, Time: 5 seconds or less (per pin row) Exposure: limit: None Note	_

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

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M8E 00.4