



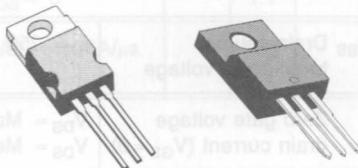
**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTORS**

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
MTP3N60	600 V	2.5 Ω	3 A
MTP3N60FI	600 V	2.5 Ω	2.5 A

- HIGH VOLTAGE FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING TIMES FOR OPERATION AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE
- INDUSTRIAL APPLICATIONS**
- SWITCHING POWER SUPPLIES

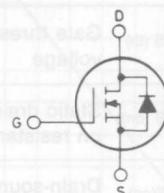
N - channel enhancement mode POWER MOS field effect transistors. Easy drive and fast switching times make these POWER MOS ideal for very high speed switching applications. Typical uses include SMPS and uninterruptible power supplies.



TO-220

ISOWATT220

INTERNAL SCHEMATIC
DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220	ISOWATT220	
V _{DS}	Drain-source voltage (V _{GS} = 0)	600	600	V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 kΩ)	600	600	V
V _{GS}	Gate-source voltage	±20	±20	V
I _D	Drain current (cont.) at T _c = 25°C	3	2.5	A
I _{DM}	Drain current (pulsed)	10	10	A
P _{tot}	Total dissipation at T _c < 25°C	75	35	W
	Derating factor	0.6	0.28	W/°C
T _{stg}	Storage temperature	-65 to 150		
T _j	Max. operating junction temperature	150		

THERMAL DATA

TO-220 | ISOWATT220

R_{thj} - case	Thermal resistance junction-case	max	1.67	3.57	$^{\circ}\text{C}/\text{W}$
R_{thj} - amb	Thermal resistance junction-ambient	max	62.5		$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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Note: Dimensions in micrometers. Use lead-free external packaging and surface-mount technology.

OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$	$V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^{\circ}\text{C}$		200			μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$		1000			μA
				± 100			nA

Note: Dimensions in micrometers. Use lead-free external packaging and surface-mount technology.

ON

$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ $V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ $T_c = 100^{\circ}\text{C}$	2		4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $I_D = 1.5 \text{ A}$	1.5		4	V
$V_{DS(on)}$	Drain-source on voltage	$V_{GS} = 10 \text{ V}$ $I_D = 3 \text{ A}$ $V_{GS} = 10 \text{ V}$ $I_D = 1.5 \text{ A}$ $T_c = 100^{\circ}\text{C}$			2.5	Ω
					9	V
					7.5	V

DYNAMIC

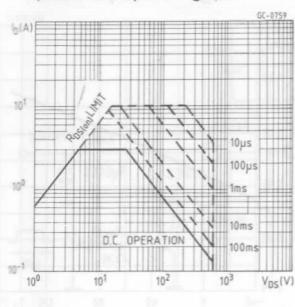
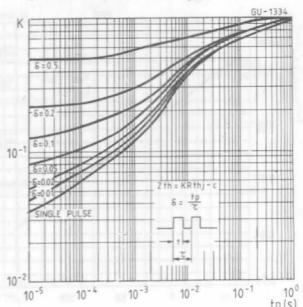
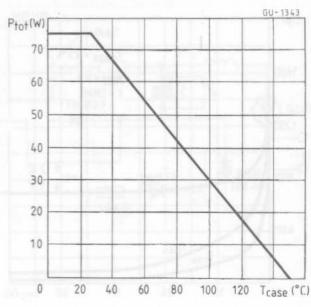
g_{fs}	Forward transconductance	$V_{DS} = 15 \text{ V}$ $I_D = 1.5 \text{ A}$	1.5			mho
C_{iss}	Input capacitance					
C_{oss}	Output capacitance					
C_{rss}	Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$ $f = 1 \text{ MHz}$ $V_{GS} = 0$			1000	pF
					300	pF
					80	pF

SWITCHING

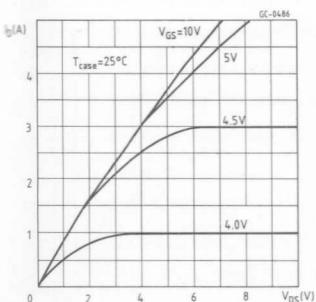
$t_d(\text{on})$	Turn-on time	$V_{DD} = 25 \text{ V}$ $I_D = 1.5 \text{ A}$	50		ns
t_r	Rise time		100		ns
$t_d(\text{off})$	Turn-off delay time		180		ns
t_f	Fall time	$R_i = 50 \Omega$ $V_i = 10 \text{ V}$	80		ns

ELECTRICAL CHARACTERISTICS (Continued)

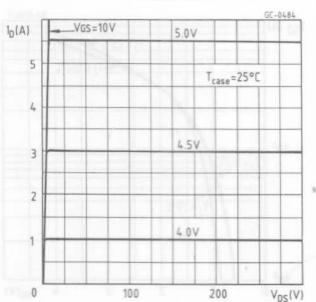
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD}	Source-drain current			3	A
I_{SDM}	Source-drain current (pulsed)			10	A
V_{SD}	Forward on voltage	$I_{SD} = 3 \text{ A}$	$V_{GS} = 0$	1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 3 \text{ A}$	$dI/dt = 100 \text{ A}/\mu\text{s}$	165	ns

Safe operating areas
(standard package)Thermal impedance
(standard package)Derating curve
(standard package)

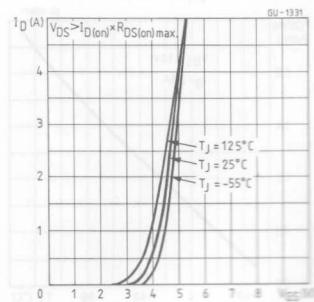
Output characteristics



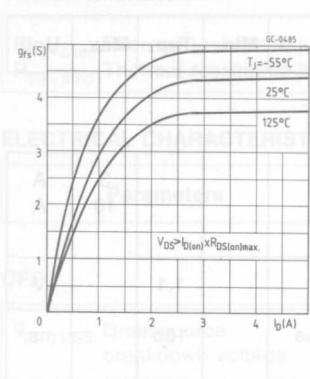
Output characteristics



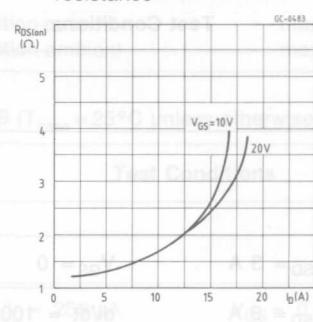
Transfer characteristics



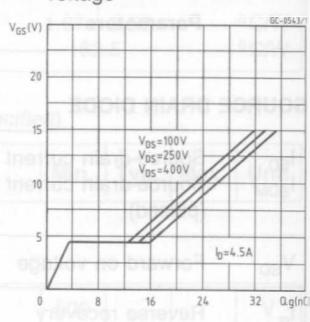
Transconductance



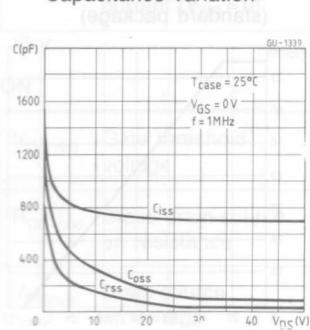
Static drain-source on resistance



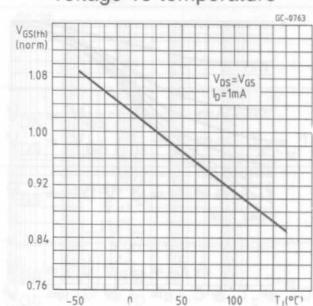
Gate charge vs gate-source voltage



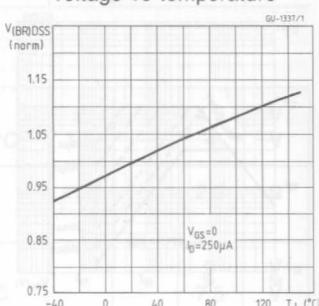
Capacitance variation



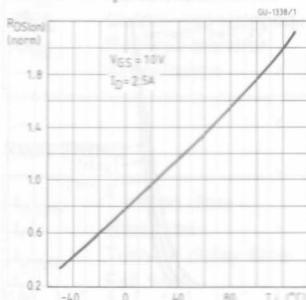
Normalized gate threshold voltage vs temperature



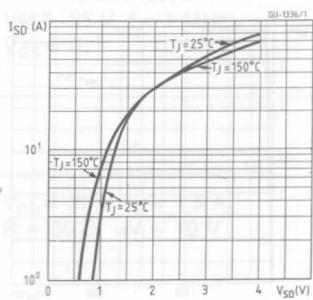
Normalized breakdown voltage vs temperature



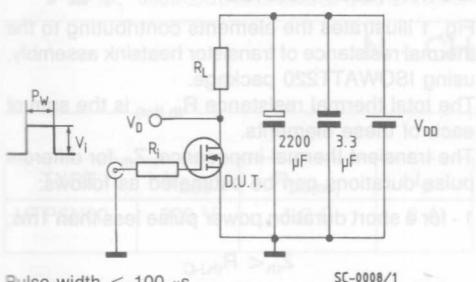
Normalized on resistance vs temperature



Source-drain diode forward characteristics

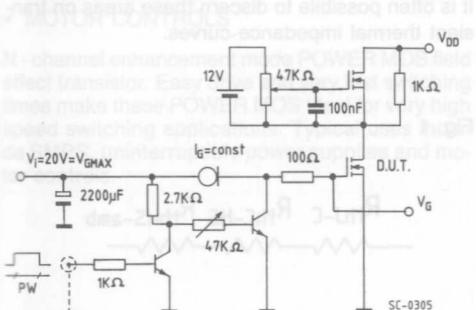


Switching times test circuit for resistive load

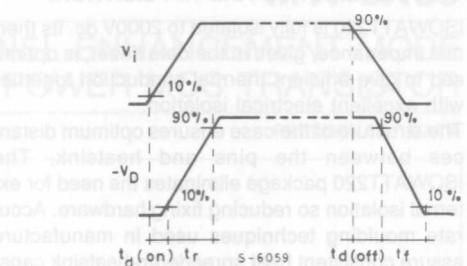
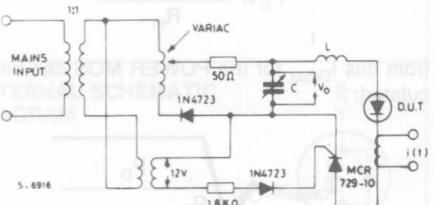


* ULTRA FAST SWITCHING TIMES FOR
* EASY DRIVE FOR REDUCED COST AND
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Gate charge test circuit



Switching time waveforms for resistive load

Body-drain diode t_{rr} measurement
Jedec test circuit

ABSOLUTE MAXIMUM RATINGS

V_{DS} Drain-source voltage ($V_{GS} = 0$)

V_{GDS} Drain-gate voltage ($V_{DS} = 0$)

V_{GSS} Gate-source voltage

I_{DS} Drain current ($V_{GS} = 0$)

I_{DS} drain current (self-heated)

T_J Junction temperature

T_{SD} Storage temperature

T_{SO} Operating junction temperature

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.

ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

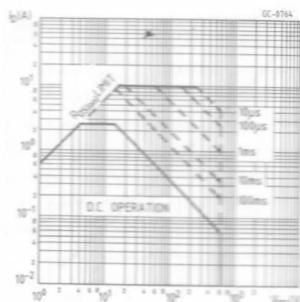
$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

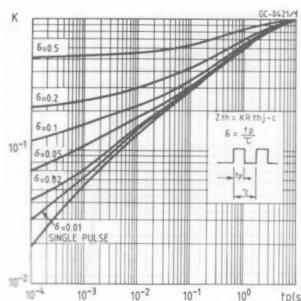
$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)} \text{ (at } 150^\circ\text{C)}}}$$

ISOWATT DATA

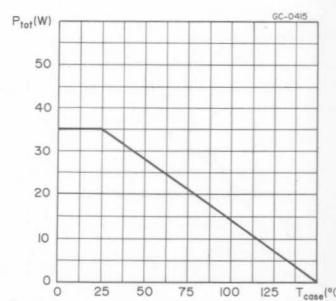
Safe operating areas



Thermal impedance



Derating curve



THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.

The total thermal resistance $R_{th(\text{tot})}$ is the sum of each of these elements.

The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

It is often possible to discern these areas on transient thermal impedance curves.

Fig. 1

