

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3386 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)1} = 21 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 17 \text{ A)}$
 $R_{DS(on)2} = 36 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 17 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2100 \text{ pF TYP.}$
- Built-in Gate Protection Diode
- TO-251/TO-252 package

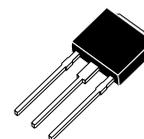
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3386	TO-251
2SK3386-Z	TO-252

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 34	A
★ Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 120	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_T	40	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	28	A
Single Avalanche Energy ^{Note2}	E_{AS}	78	mJ

(TO-251)



(TO-252)



Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

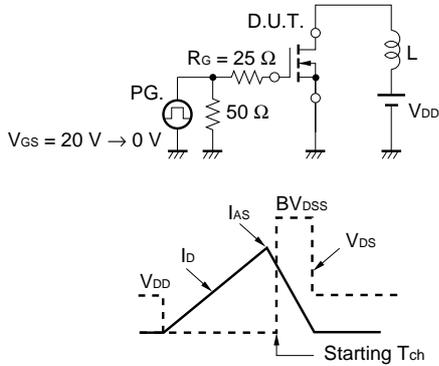
2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

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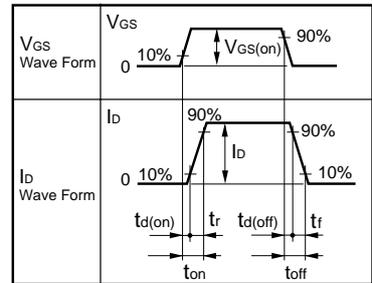
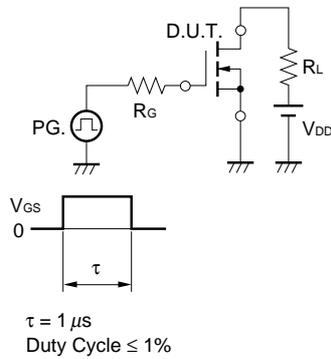
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 17 A	10	19		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 17 A		17	21	mΩ
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 17 A		25	36	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		2100		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		340		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		170		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 17 A		32		ns
Rise Time	t _r	V _{GS(on)} = 10 V		310		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		98		ns
Fall Time	t _f			100		ns
Total Gate Charge	Q _G	V _{DD} = 48 V		39		nC
Gate to Source Charge	Q _{GS}	V _{GS(on)} = 10 V		7.0		nC
Gate to Drain Charge	Q _{GD}	I _D = 34 A		12		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 34 A, V _{GS} = 0 V		0.87		V
Reverse Recovery Time	t _{rr}	I _F = 34 A, V _{GS} = 0 V		46		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		84		nC

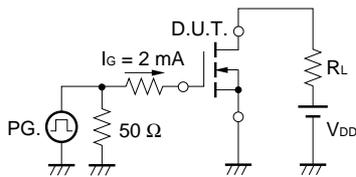
TEST CIRCUIT 1 AVALANCHE CAPABILITY



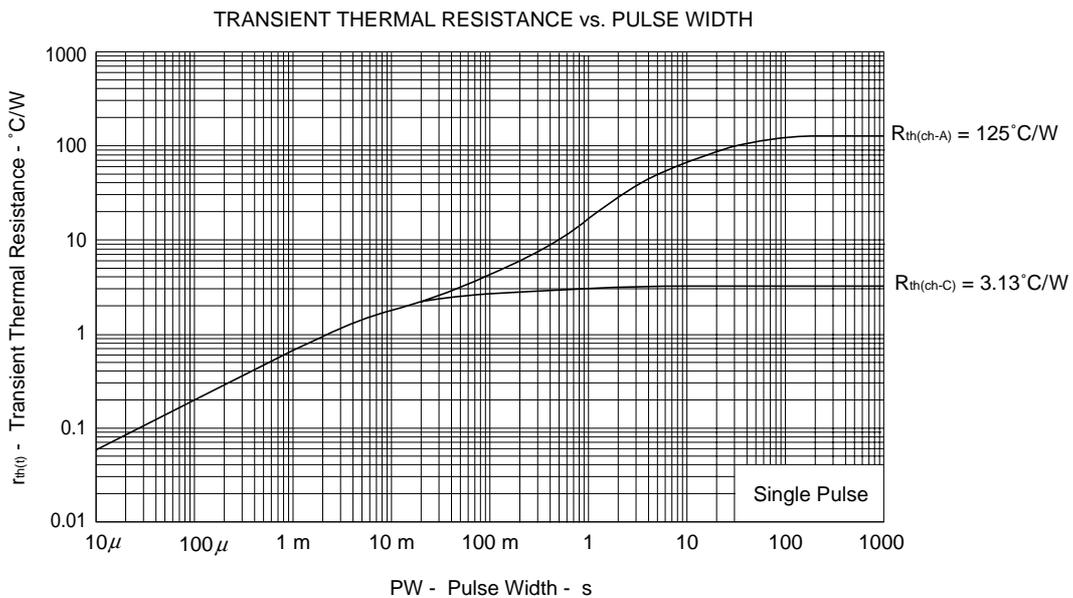
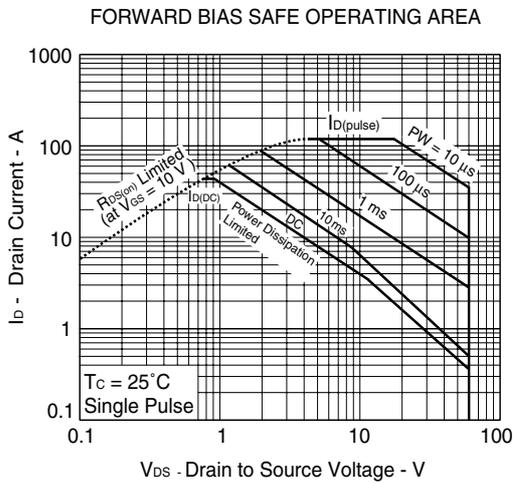
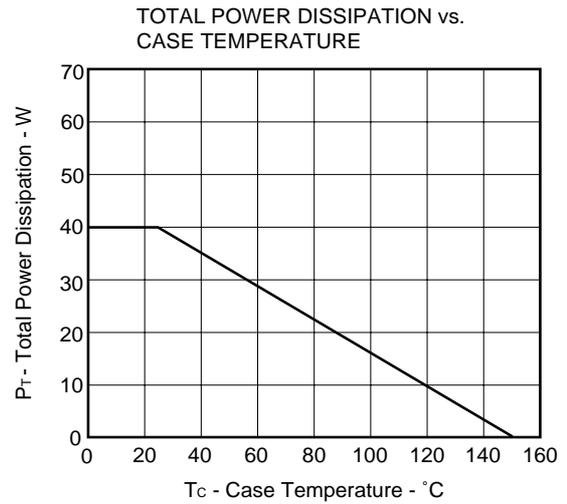
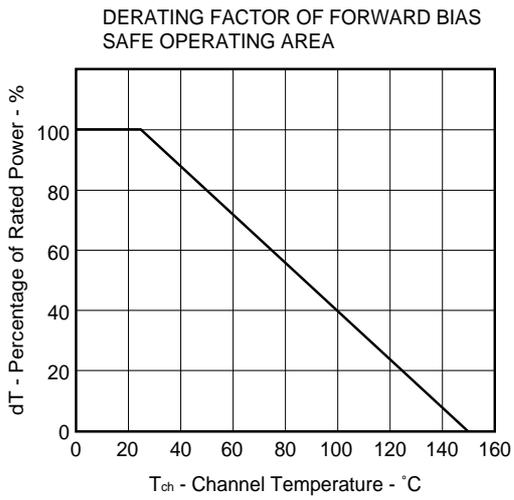
TEST CIRCUIT 2 SWITCHING TIME



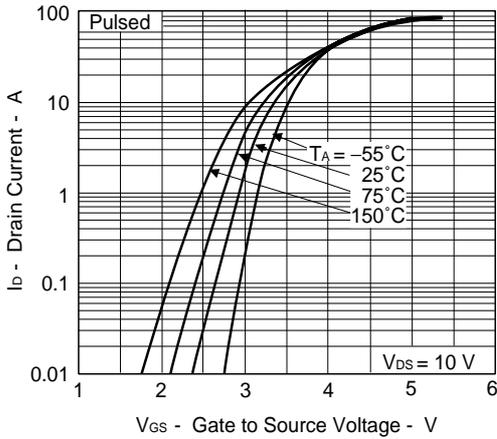
TEST CIRCUIT 3 GATE CHARGE



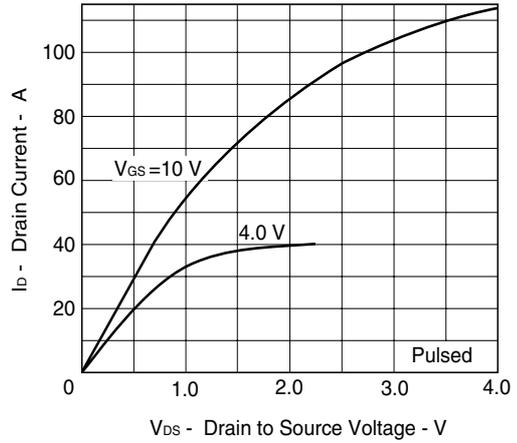
★ TYPICAL CHARACTERISTICS (T_A = 25°C)



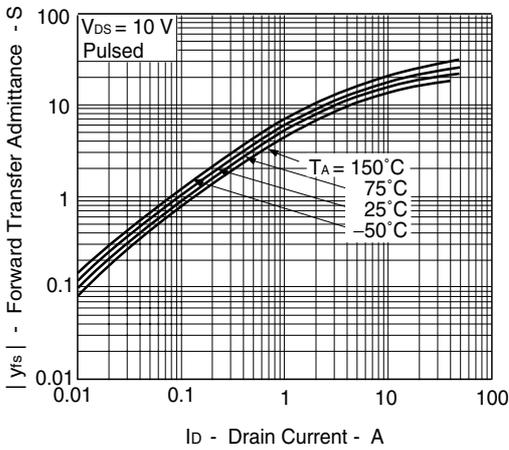
FORWARD TRANSFER CHARACTERISTICS



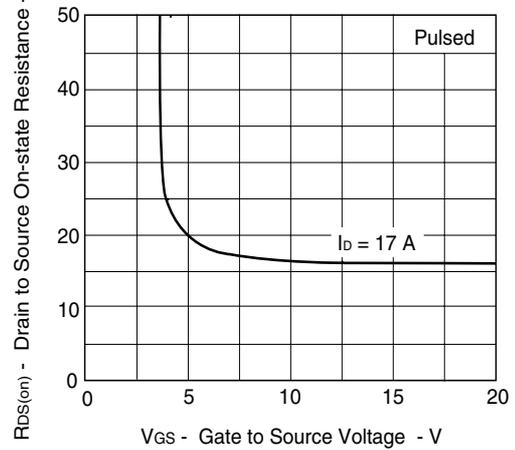
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



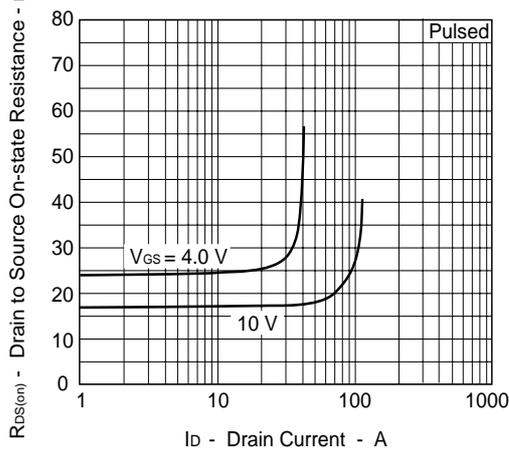
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



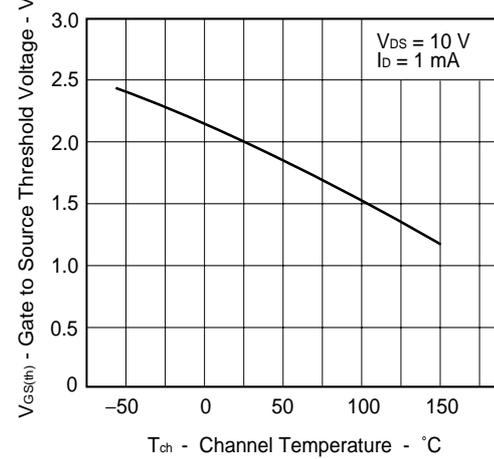
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

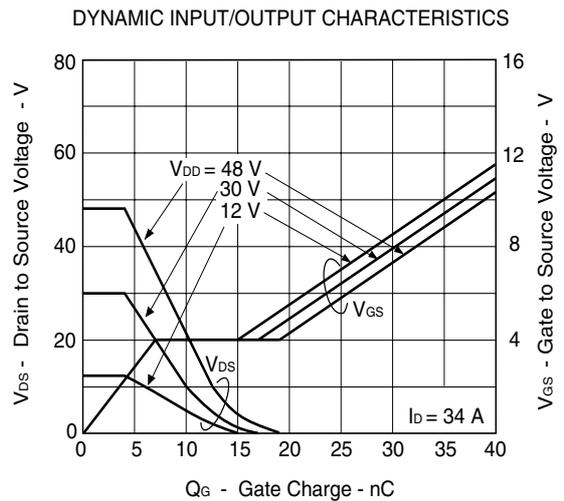
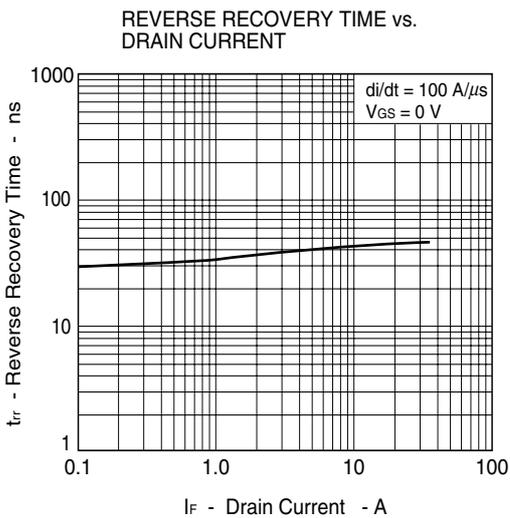
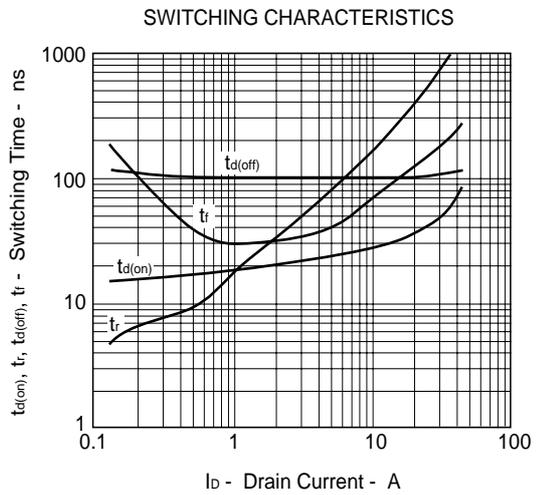
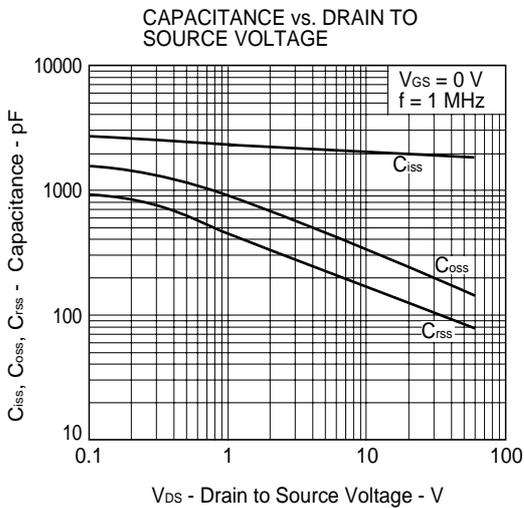
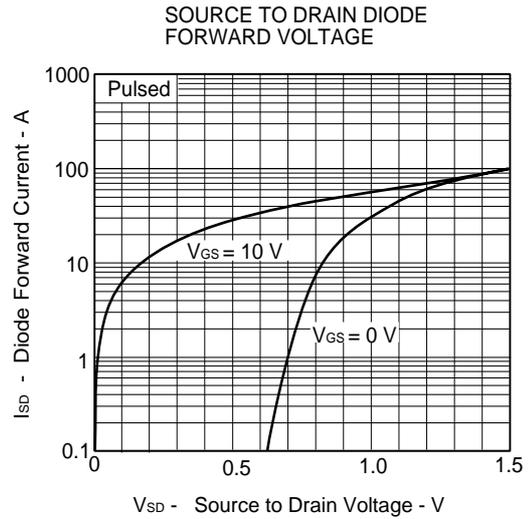
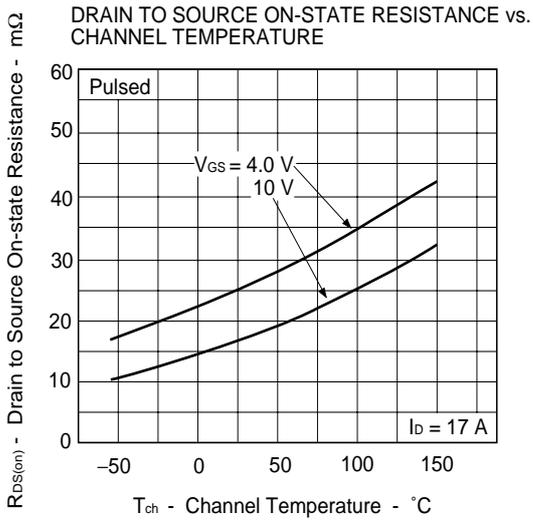


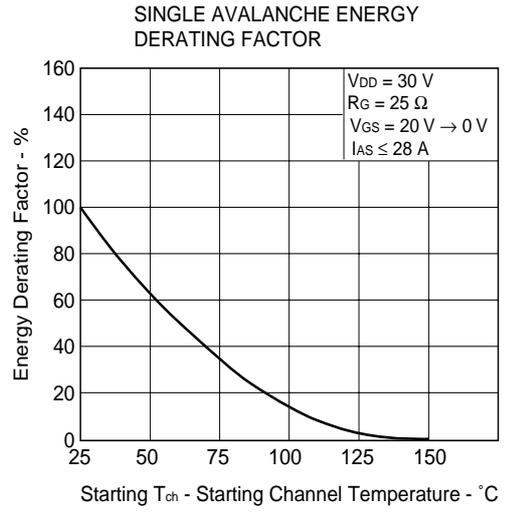
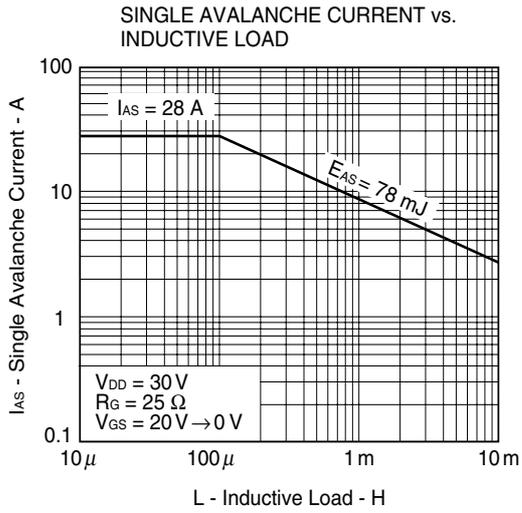
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

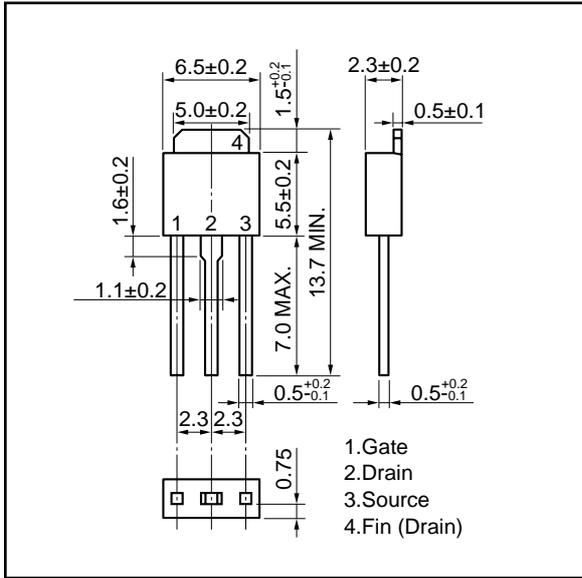




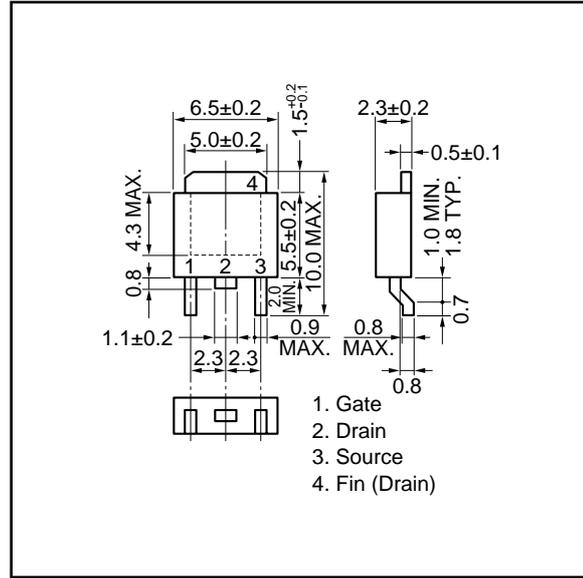


PACKAGE DRAWINGS (Unit: mm)

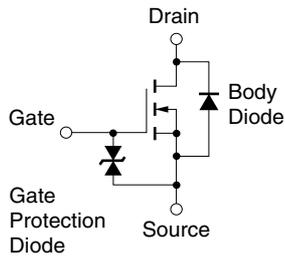
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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