Silicon N-Channel MOS FET Low Frequency Power Switching

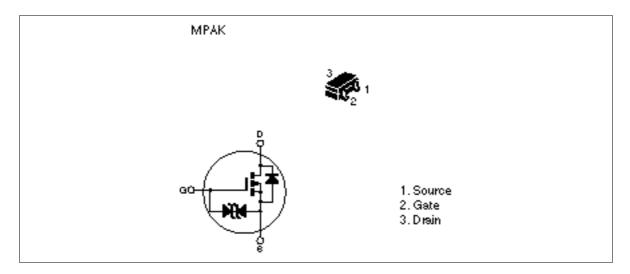


ADE-208-571 1st. Edition

Features

- Low on-resistance $R_{DS(on)}=0.\ 2\Omega \ typ. \ (V_{GS}=4 \ V, \ I_D=500 \ mA)$
- 2.5V gate drive devices.
- Small package (MPAK)

Outline





Absolute Maximum Ratings (Ta = 25° C)

Item	Symbol	Ratings	Unit	
Drain to source voltage	V _{DSS}	30	V	
Gate to source voltage	V _{GSS}	+12	V	
		-10	V	
Drain current	ID	1.0	А	
Drain peak current	I _{D(pulse)} * ¹	4	А	
Channel dissipation	Pch * ²	0.8	W	
Channel temperature	Tch	150	°C	
Storage temperature	Tstg	-55 to +150	°C	

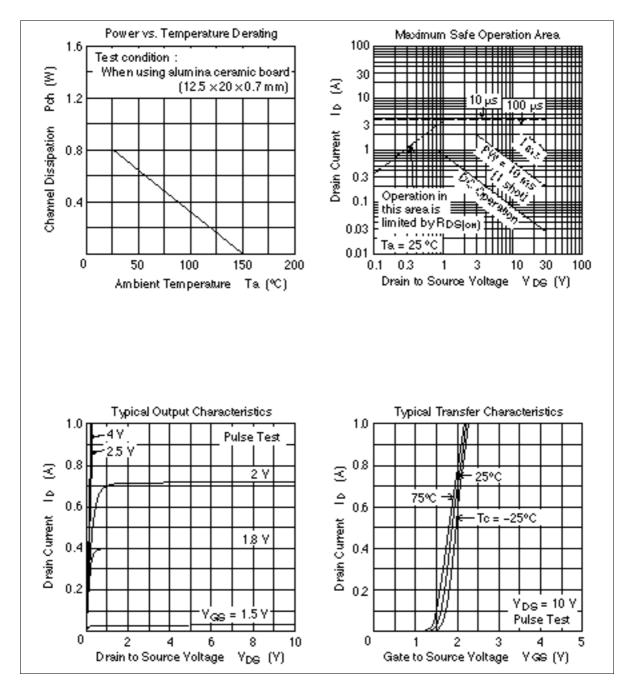
Notes: 1. $PW \le 10\mu s$, duty cycle $\le 1 \%$

2. Value at when using alumina ceramic board (12.5 x 20 x 0.7 mm)

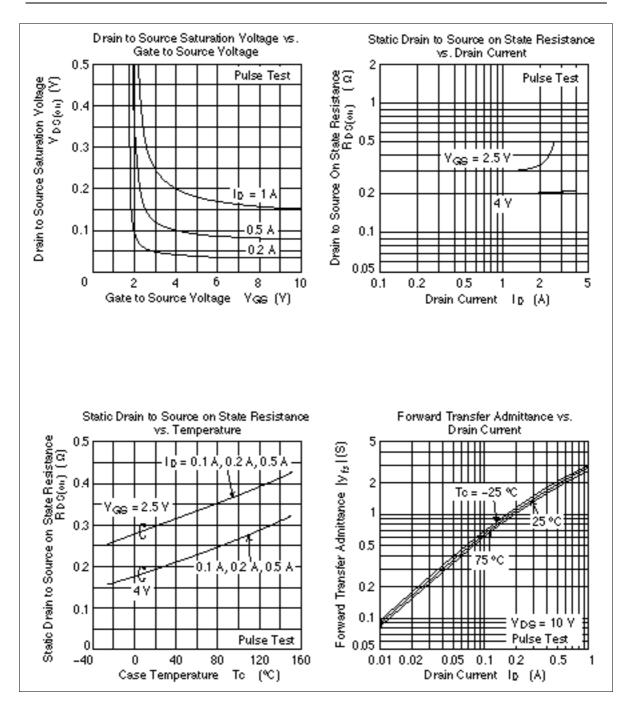
Electrical Characteristics (Ta = 25°C)

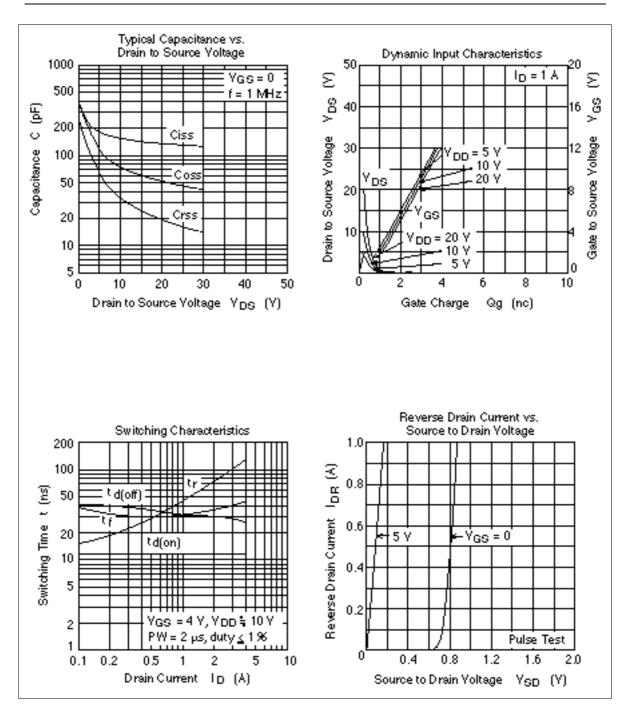
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 100 \mu A, V_{GS} = 0$
Gate to source breakdown	V _{(BR)GSS}	+12		_	V	$I_G = +100 \mu A, V_{DS} = 0$
voltage		-10	_	_	V	$I_G = -100 \mu A, V_{DS} = 0$
Zero gate voltege drain current	I _{DSS}			1.0	μA	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Gate to source leak current	I _{GSS}			±5.0	μA	$V_{GS} = \pm 8V$, $V_{DS} = 0$
Gate to source cutoff voltage	V _{GS(off)}	0.5		1.5	V	$I_D = 10 \mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{\text{DS(on)}}$	_	0.2	0.28	Ω	$I_{D} = 500 \text{ mA}$ $V_{GS} = 4 \text{V}^{*1}$
		_	0.3	0.5	Ω	$I_D = 500 \text{ mA}$ $V_{GS} = 2.5 \text{V}^{*1}$
Forward transfer admittance	y _{fs}	1.2	2.0	—	S	I _D = 500 mA V _{DS} = 10V * ¹
Input capacitance	Ciss		155	_	pF	$V_{DS} = 10V$
Output capacitance	Coss		75	_	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss		35	_	pF	f = 1MHz
Turn-on delay time	t _{d(on)}		12	_	μs	$V_{GS} = 4V, I_D = 500 \text{ mA}$
Rise time	t _r		30		μs	$R_L = 20\Omega$
Turn-off delay time	t _{d(off)}		35		μs	
Fall time	t _f		30		μs	
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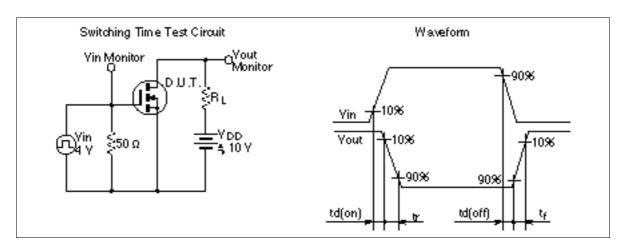
Note: 1. Pulse test



Main Characteristics

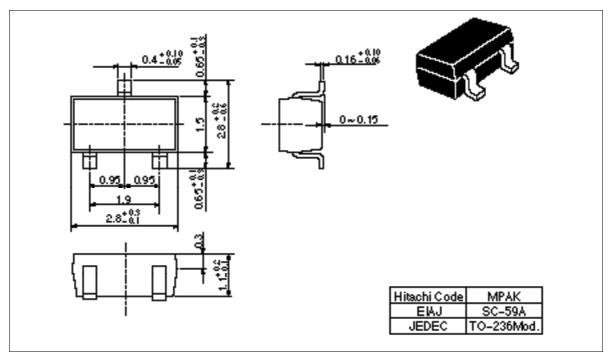






Package Dimensions

Unit: mm



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