# 2SK2912(L), 2SK2912(S)

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

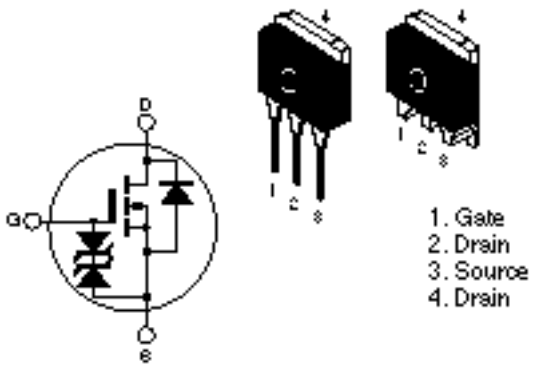
ADE-208-495
1st. Edition

## Features

- Low on-resistance
  $R_{DS}$ = 15 mΩ typ.
- High speed switching
- 4V gate drive device can be driven from 5V source

## Outline

LDPAK




Hitachi semiconductor

## Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 60 | V |
| Gate to source voltage | $V_{GSS}$ | ±20 | V |
| Drain current | $I_D$ | 40 | A |
| Drain peak current | $I_{D(pulse)}$*[1] | 160 | A |
| Body to drain diode reverse drain current | $I_{DR}$ | 40 | A |
| Avalanche current | $I_{AP}$*[3] | 40 | A |
| Avalanche Energy | $E_{AR}$*[3] | 137 | mJ |
| Channel dissipation | Pch*[2] | 50 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |

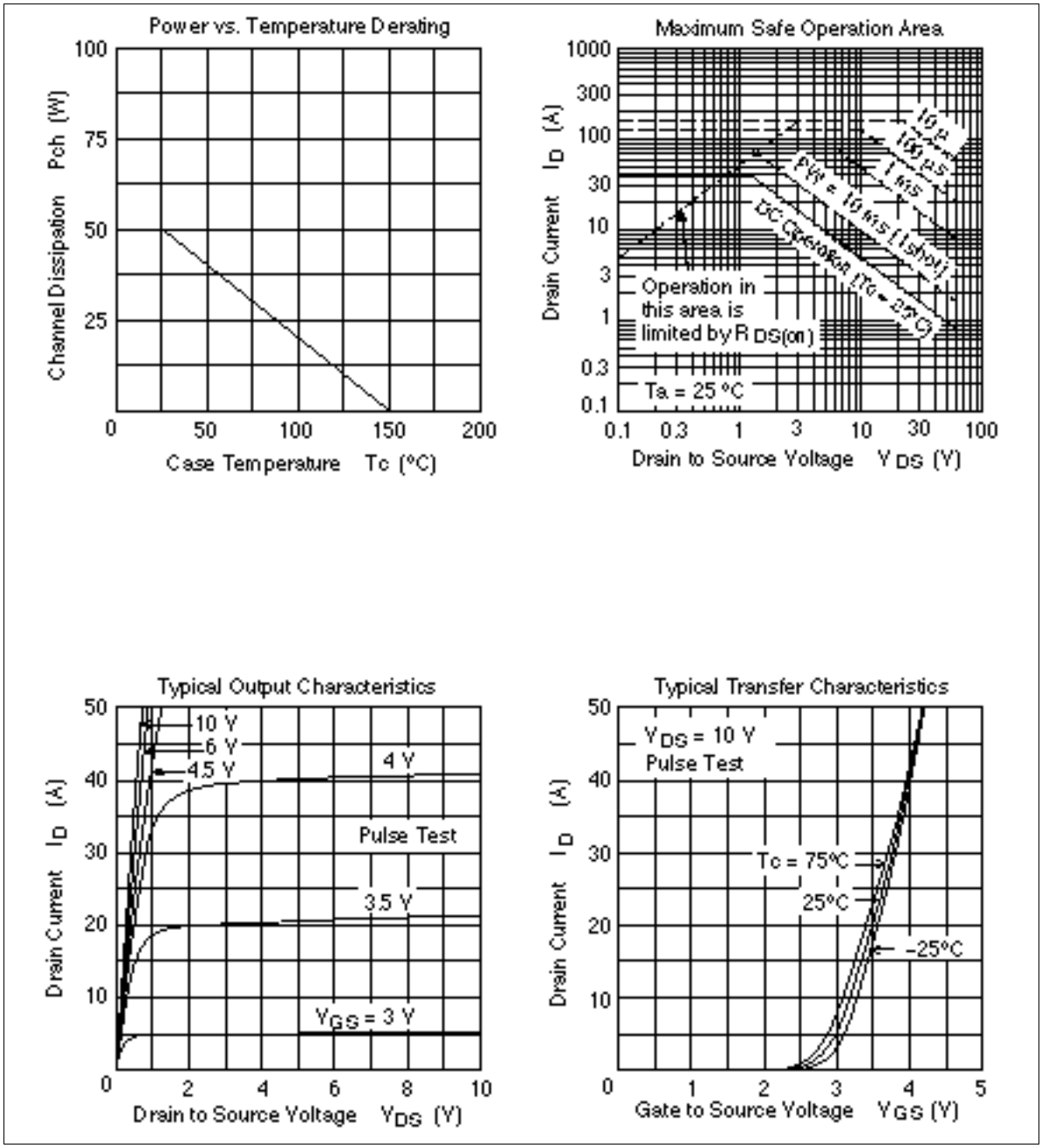
Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg 50 Ω

## Electrical Characteristics (Ta = 25°C)

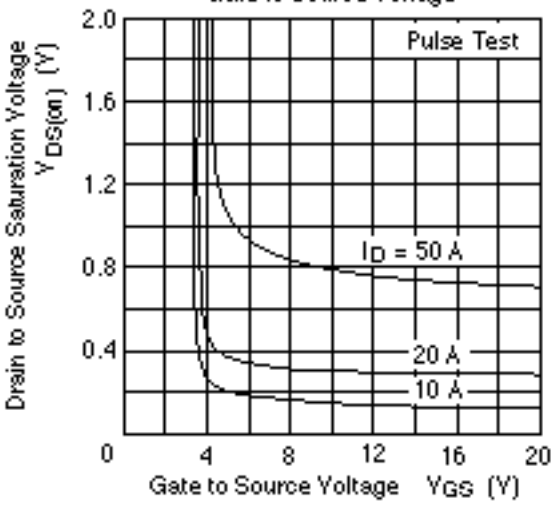
| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 60 | — | — | V | $I_D$ = 10mA, $V_{GS}$ = 0 |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ±20 | — | — | V | $I_G$ = ±100µA, $V_{DS}$ = 0 |
| Gate to source leak current | $I_{GSS}$ | — | — | ±10 | µA | $V_{GS}$ = ±16V, $V_{DS}$ = 0 |
| Zero gate voltege drain current | $I_{DSS}$ | — | — | 10 | µA | $V_{DS}$ = 60 V, $V_{GS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 1.5 | — | 2.5 | V | $I_D$ = 1mA, $V_{DS}$ = 10V |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 15 | 20 | mΩ | $I_D$ = 20A, $V_{GS}$ = 10V*[1] |
| | $R_{DS(on)}$ | — | 25 | 40 | mΩ | $I_D$ = 20A, $V_{GS}$ = 4V*[1] |
| Forward transfer admittance | $\|y_{fs}\|$ | 20 | 35 | — | S | $I_D$ = 20A, $V_{DS}$ = 10V*[1] |
| Input capacitance | Ciss | — | 1500 | — | pF | $V_{DS}$ = 10V |
| Output capacitance | Coss | — | 720 | — | pF | $V_{GS}$ = 0 |
| Reverse transfer capacitance | Crss | — | 200 | — | pF | f = 1MHz |
| Turn-on delay time | $t_{d(on)}$ | — | 20 | — | ns | $I_D$ = 20A, $V_{GS}$ = 10V |
| Rise time | $t_r$ | — | 180 | — | ns | $R_L$ = 1.5Ω |
| Turn-off delay time | $t_{d(off)}$ | — | 200 | — | ns | |
| Fall time | $t_f$ | — | 200 | — | ns | |
| Body to drain diode forward voltage | $V_{DF}$ | — | 0.95 | — | V | $I_F$ = 40A, $V_{GS}$ = 0<br>diF/ dt = 50A/µs |
| Body to drain diode reverse recovery time | $t_{rr}$ | — | 70 | — | V | $I_F$ = 40A, $V_{GS}$ = 0<br>diF/ dt = 50A/µs |

Note: 1. Pulse test

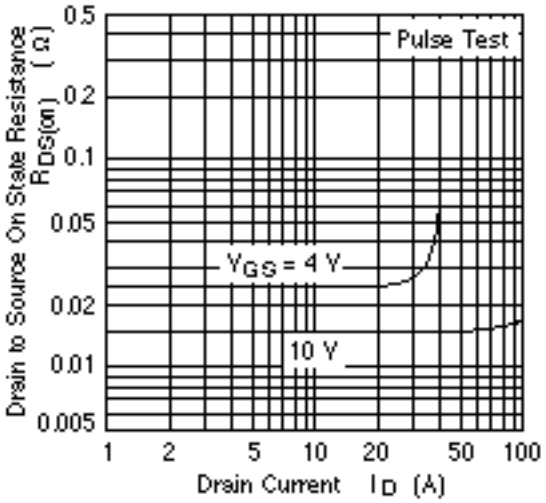
## Main Characteristics



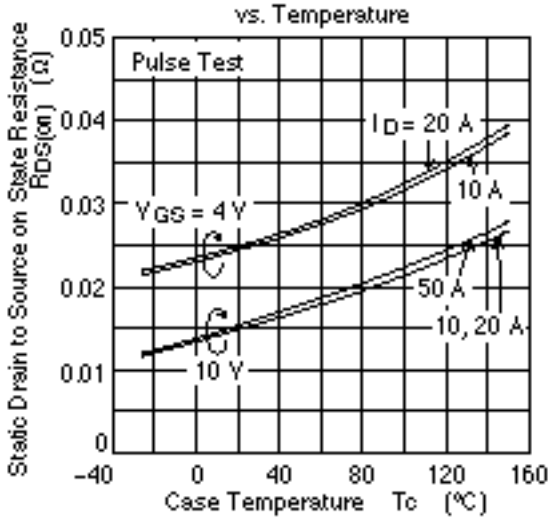
Drain to Source Saturation Voltage vs. Gate to Source Voltage



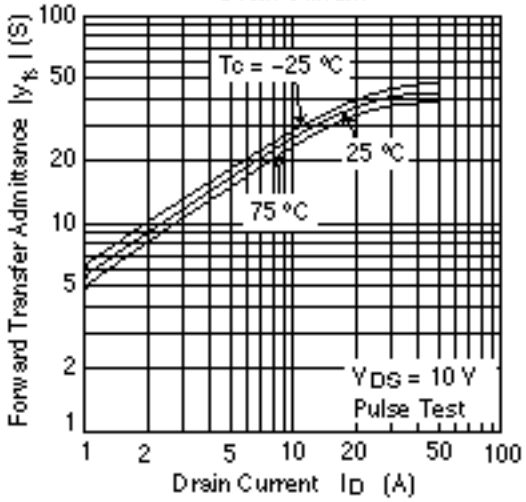

Static Drain to Source on State Resistance vs. Drain Current

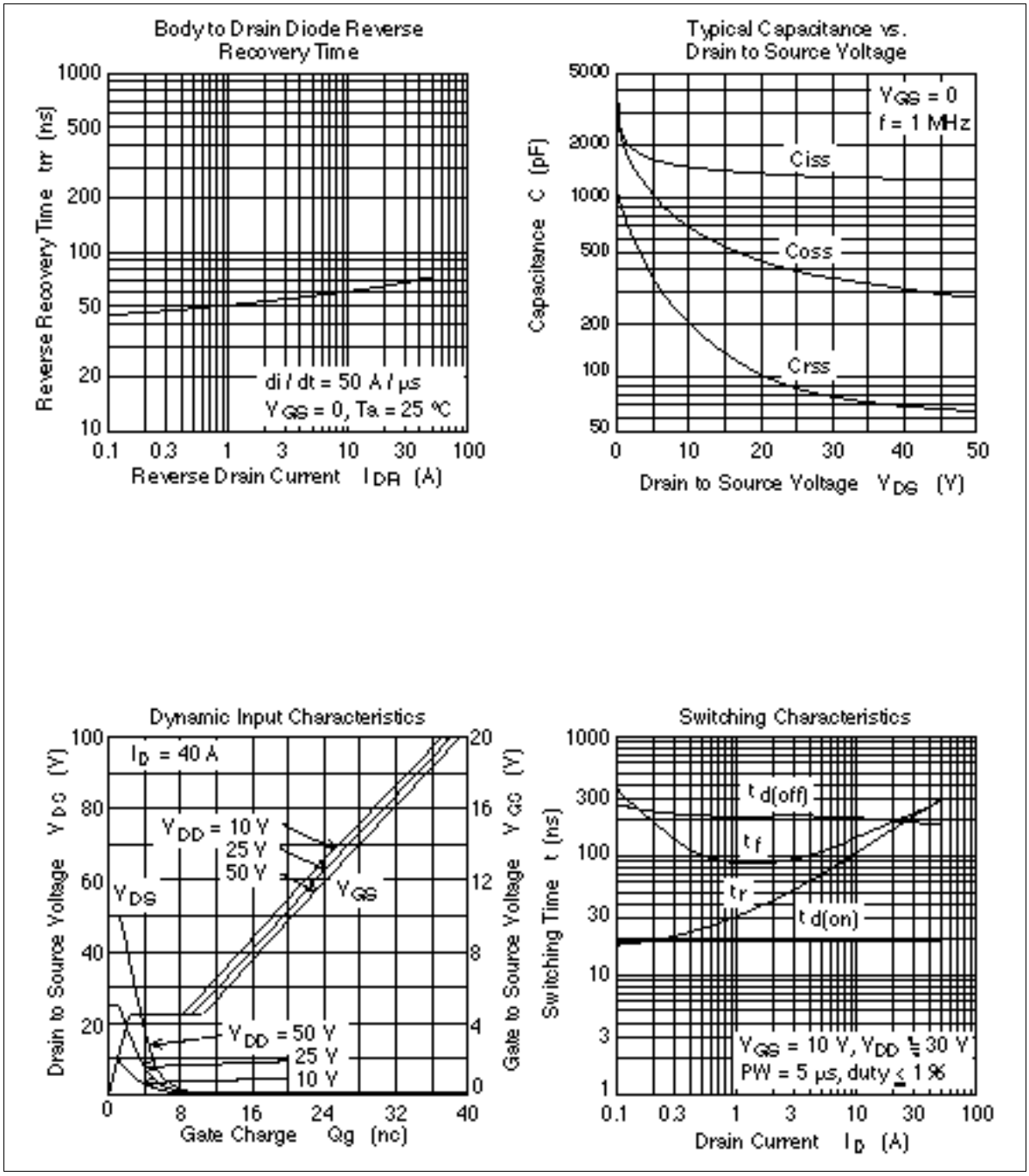



Static Drain to Source on State Resistance vs. Temperature

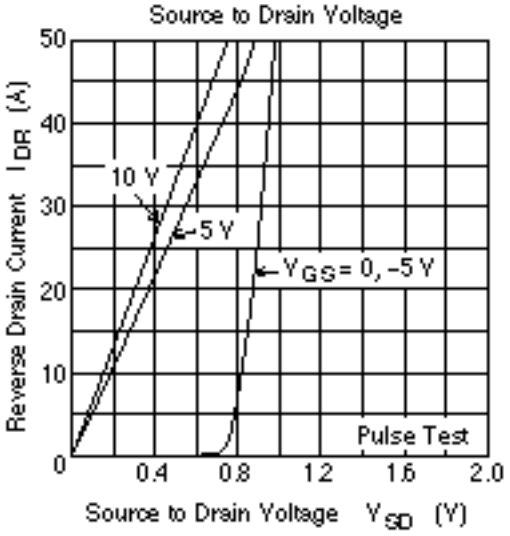



Forward Transfer Admittance vs. Drain Current

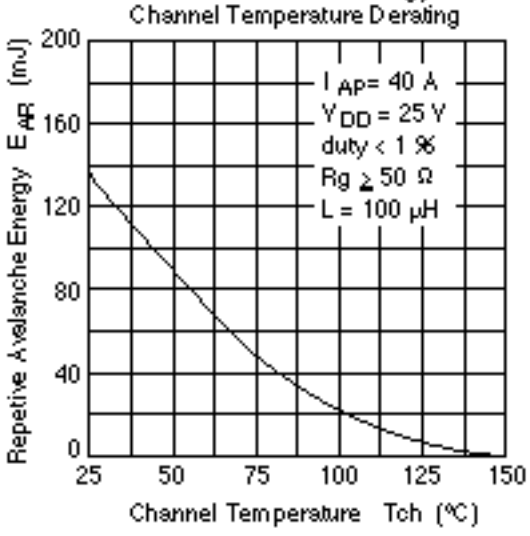



Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
0.1 0.3 1 3 10 30 100
Reverse Drain Current IDR (A)
Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
2000
1000
500
200
100
50
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0 10 20 30 40 50
Drain to Source Voltage VDS (V)
Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
ID = 40 A
VDD = 10 V
25 V
50 V
VDS
VGS
VDD = 50 V
25 V
10 V
0 8 16 24 32 40
Gate Charge Qg (nc)
Switching Characteristics
Switching Time t (ns)
1000
300
100
30
10
3
1
td(off)
tf
tr
td(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
0.1 0.3 1 3 10 30 100
Drain Current ID (A)

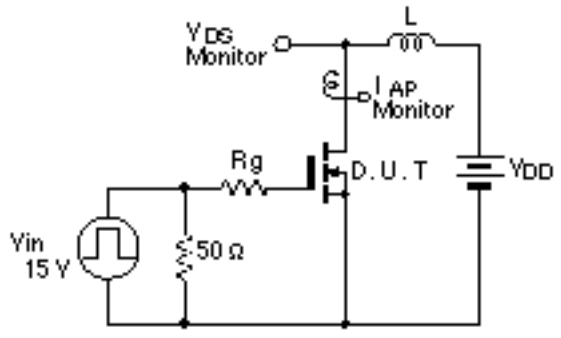
Reverse Drain Current vs. Source to Drain Voltage




Maximum Avalanche Energy vs. Channel Temperature Derating

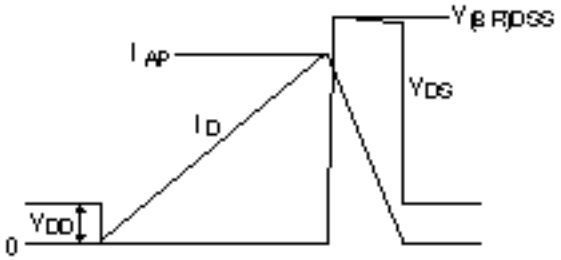



Avalanche Test Circuit

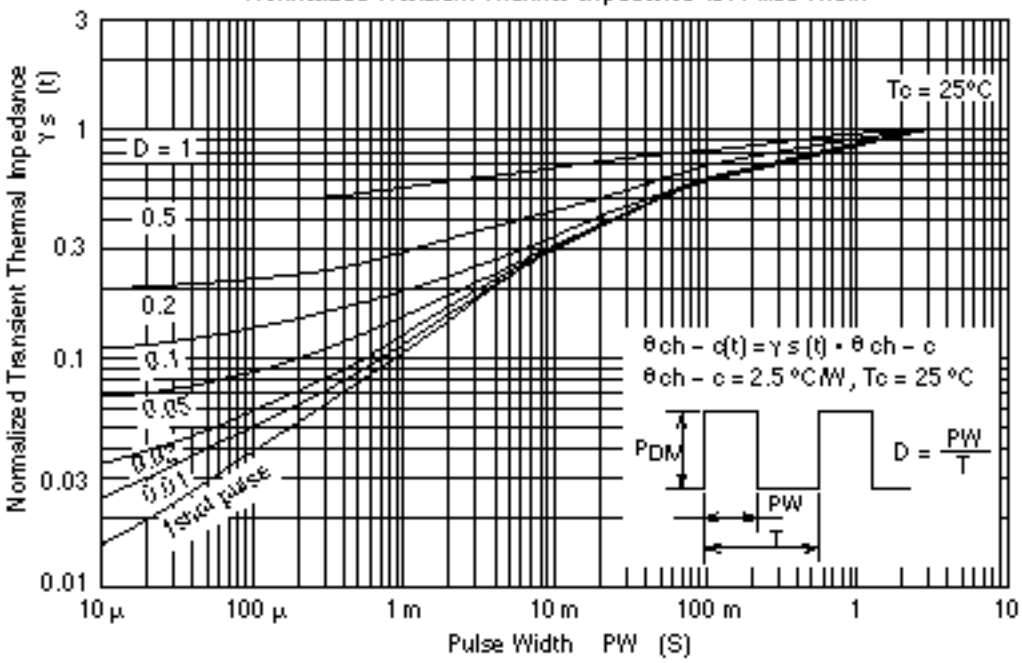



Avalanche Waveform

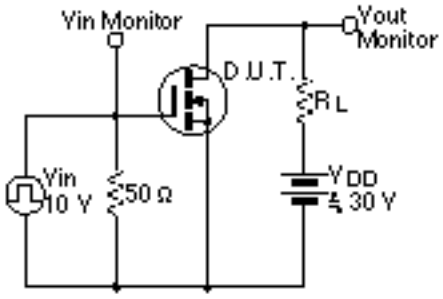
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



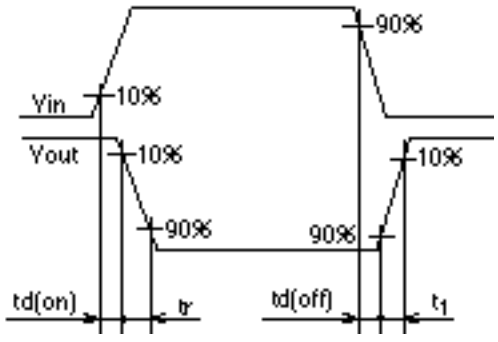
Normalized Transient Thermal Impedance vs. Pulse Width




Switching Time Test Circuit

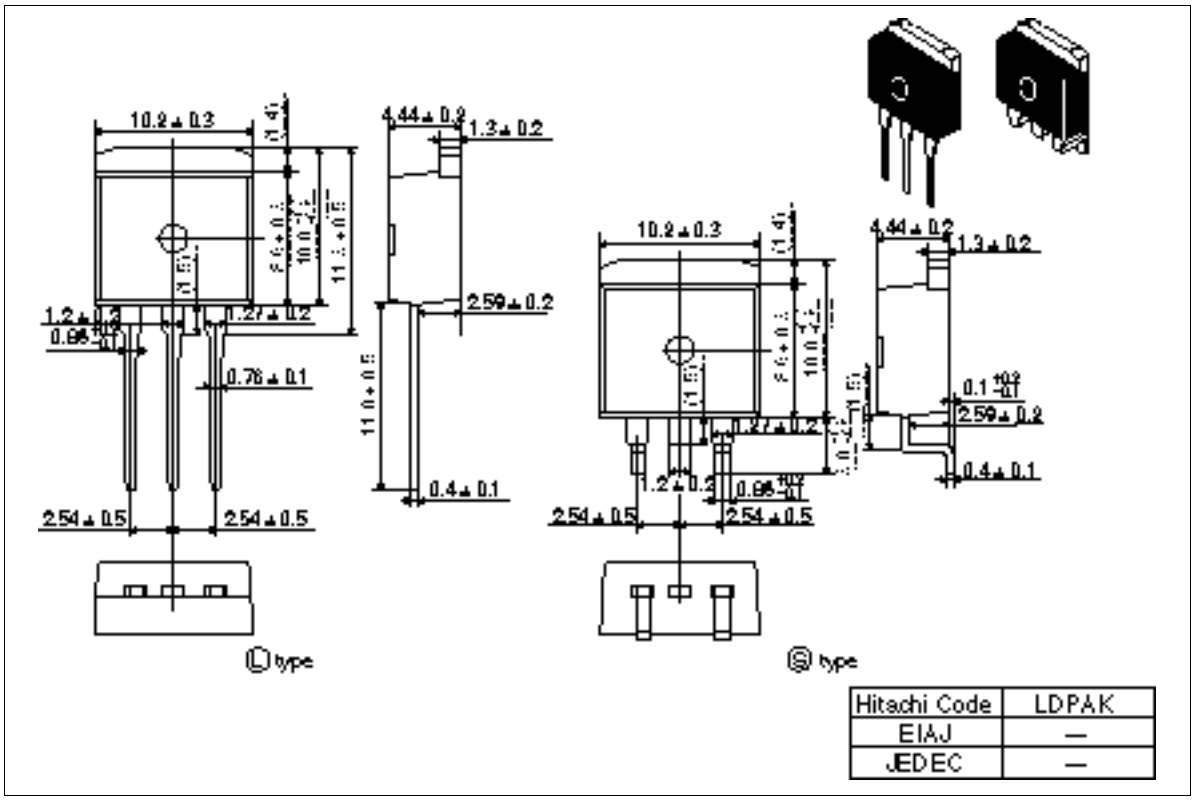



Switching Time Waveforms



## Package Dimensions

**Unit: mm**




| Hitachi Code | LDPAK |
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