Silicon N-Channel MOS FET Low Frequency Power Switching

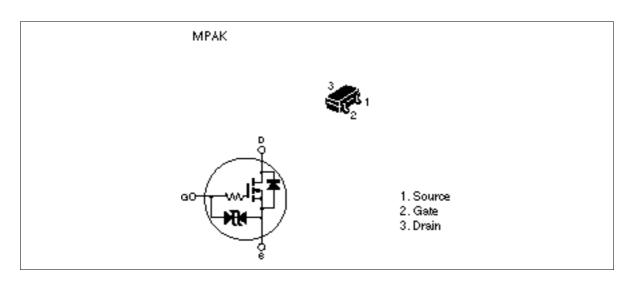
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ADE-208-574 1st. Edition

Features

- Low on-resistance $R_{DS(on)} = 0. \ 8\Omega \ typ. \ (V_{GS} = 4 \ V, \ I_D = 100 \ mA)$
- 2.5V gate drive devices.
- Small package (MPAK)

Outline





Absolute Maximum Ratings ($Ta = 25^{\circ}C$)

Item	Symbol	Ratings	Unit	
Drain to source voltage	V _{DSS}	20	V	
Gate to source voltage	V_{GSS}	±10	V	
Drain current	I _D	0.2	Α	
Drain peak current	I _{D(pulse)} *1	0.4	Α	
Channel dissipation	Pch	150	mW	
Channel temperature	Tch	150	°C	
Storage temperature	Tstg	-55 to +150	°C	

Note: 1. PW \leq 10 μ s, duty cycle \leq 1 %

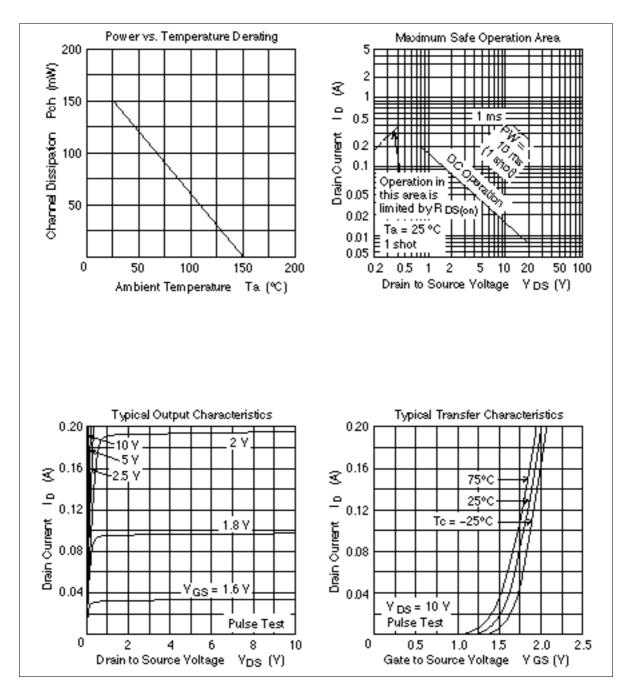
Electrical Characteristics ($Ta = 25^{\circ}C$)

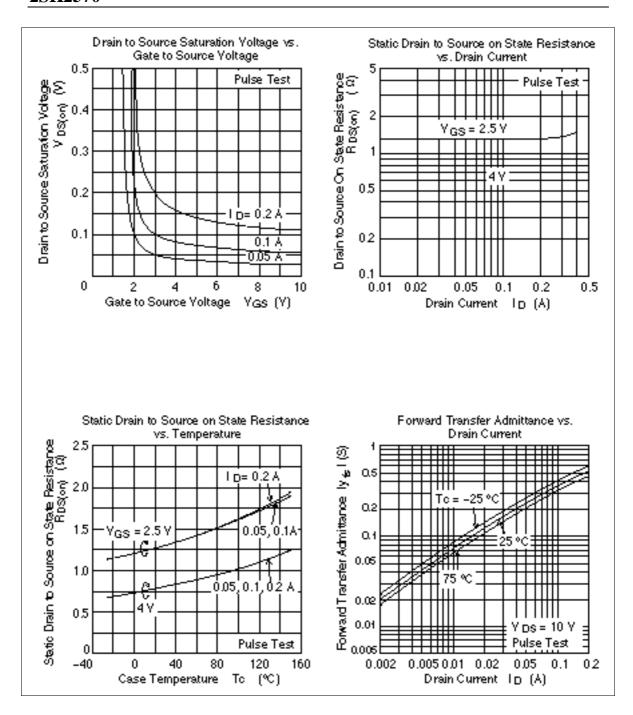
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	_	_	V	$I_D = 10 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	_	_	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Zero gate voltege drain current	I _{DSS}	_	_	1.0	μΑ	V _{DS} = 20 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	_	_	±5.0	μΑ	$V_{GS} = \pm 6.5V, V_{DS} = 0$
Gate to source cutoff voltage	V _{GS(off)}	0.5	_	1.5	V	$I_D = 10 \mu A, \ V_{DS} = 5 V$
Static drain to source on state resistance	R _{DS(on)}	_	8.0	1.1	Ω	I _D = 100 mA
						$V_{GS} = 4V^{*1}$
		_	1.3	2.2	Ω	I _D = 40 mA
						$V_{GS} = 2.5V^{*1}$
Forward transfer admittance	y _{fs}	0.22	0.35	_	S	I _D = 100 mA
						$V_{DS} = 10V^{*1}$
Input capacitance	Ciss	_	45	_	pF	V _{DS} = 10V
Output capacitance	Coss	_	33	_	pF	V _{GS} = 0
Reverse transfer capacitance	Crss	_	9.6	_	pF	f = 1MHz
Turn-on delay time	t _{d(on)}	_	20	_	ns	$V_{GS} = 5V, I_D = 100 \text{ mA}$
Rise time	t _r	_	60	_	ns	$R_L = 100\Omega$
Turn-off delay time	t _{d(off)}	_	240	_	ns	
Fall time	t _f		140		ns	

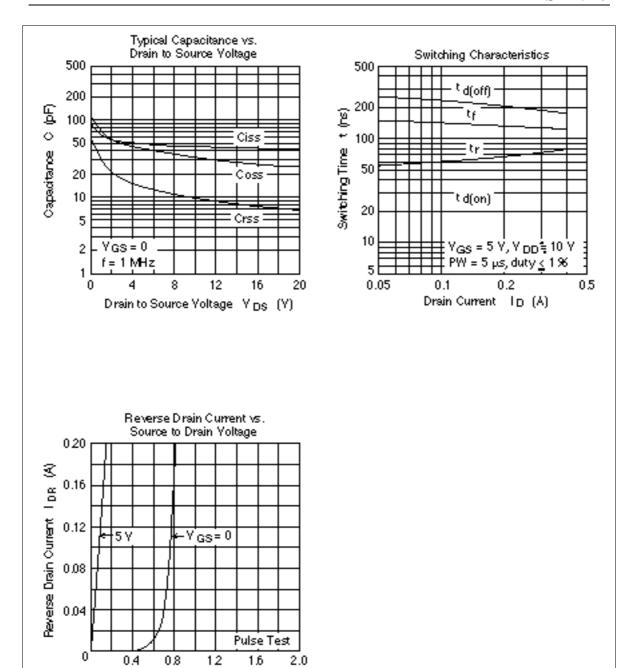
Notes: 1. Pulse test

2. Marking is "ZL-"

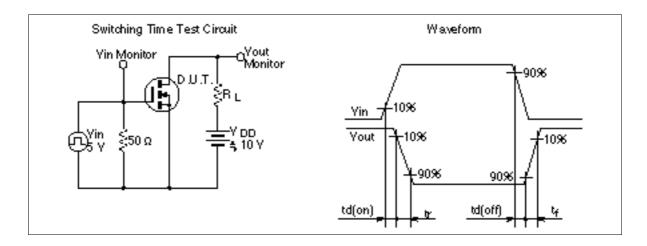
Main Characteristics





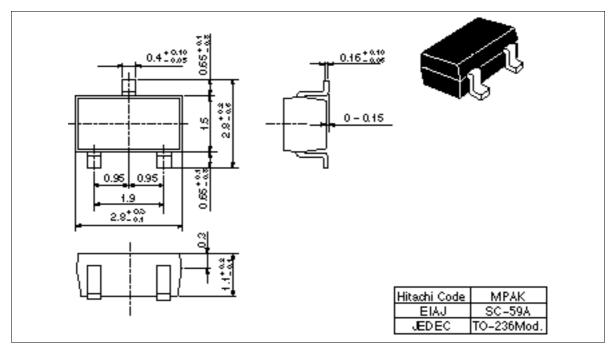


Source to Drain Voltage VSD (V)



Package Dimensions

Unit: mm



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