

# 2SD1251A

## Silicon NPN triple diffusion junction type

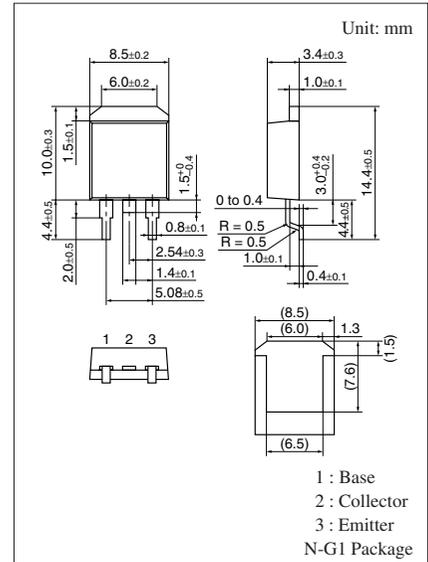
For power amplification

### ■ Features

- Wide safe operation area
- N type package enabling direct soldering of the radiating fin to the printed circuit board, etc. of small electronic equipment.

### ■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	80	V
Collector-emitter voltage (Base open)	$V_{CEO}$	80	V
Emitter-base voltage (Collector open)	$V_{EBO}$	8	V
Collector current	$I_C$	4	A
Peak collector current	$I_{CP}$	6	A
Base current	$I_B$	1	A
Collector power dissipation	$P_C$	30	W
	$T_a = 25^\circ\text{C}$	1.3	
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$



Note) Self-supported type package is also prepared.

### ■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

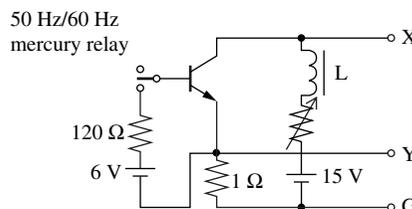
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 20\text{ V}, I_E = 0$			30	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 8\text{ V}, I_C = 0$			1	mA
Collector-emitter sustaining voltage *2	$V_{CEO(SUS)}$	$I_C = 0.2\text{ A}, L = 25\text{ mH}$	80			V
Forward current transfer ratio	$h_{FE1}$	$V_{CE} = 3\text{ V}, I_C = 0.1\text{ A}$	40			—
	$h_{FE2}^{*1}$	$V_{CE} = 3\text{ V}, I_C = 1\text{ A}$	30		160	
Base-emitter voltage	$V_{BE}$	$V_{CE} = 3\text{ V}, I_C = 1\text{ A}$			1.2	V
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 2\text{ A}, I_B = 0.4\text{ A}$			1.0	V
Transition frequency	$f_T$	$V_{CE} = 10\text{ V}, I_C = 0.2\text{ A}, f = 0.5\text{ MHz}$		1		MHz

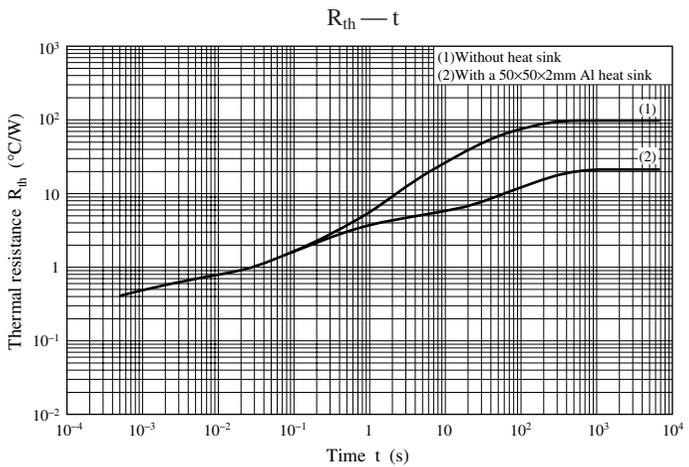
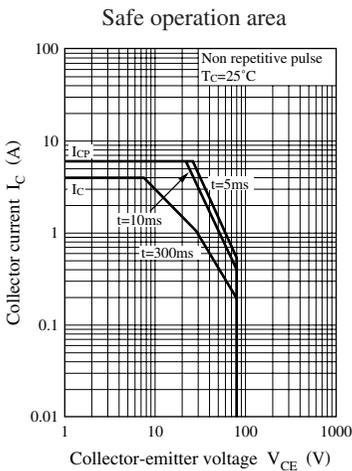
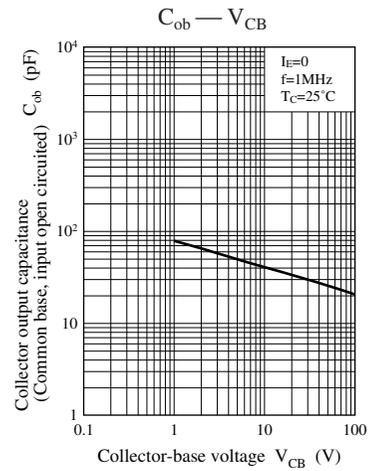
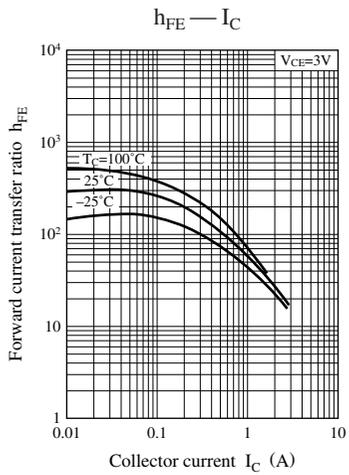
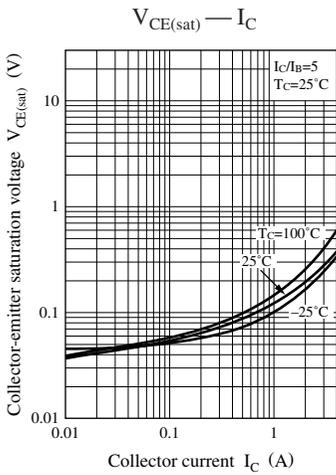
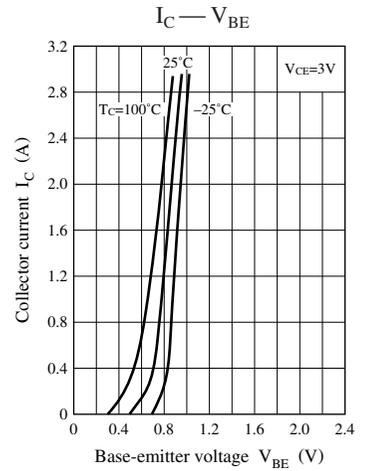
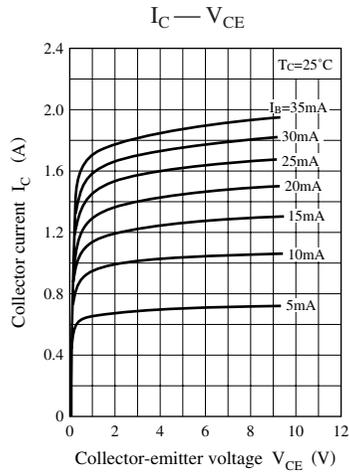
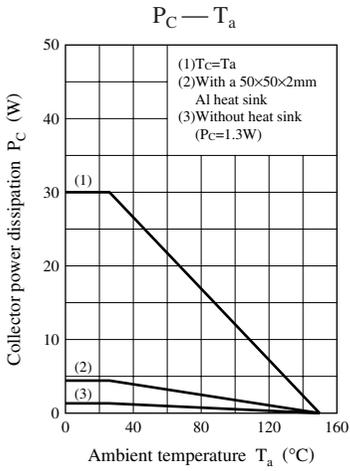
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*1: Rank classification

Rank	Q	P	O
$h_{FE2}$	30 to 60	50 to 100	80 to 160

\*2:  $V_{CEO(SUS)}$  test circuit





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