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Standard tolerances are 5%
20%, 10%, 2% and 1% are available

400 mW low voltage avalanche low noise silicon zener diodes

FEATURES

- Controlled avalanche
- Voltages fropm 4.3 to 10 V
- Low reverse leakage
- Low noise
- Hermetically sealed glass package
- APD can select any voltage in tolerances 1%, 2%, 5% and 10% at your application's test current.

MAXIMUM RATINGS

- Junction Temperature -65°C to + 175°C
- Storage Temperature -65°C to + 200°C
- DC Power Dissipation: 400mW @ T_L = 50°C
- Derate above 50°C: 2.67mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C

Type (1)	Nominal Zener Voltage @ I_{ZT}	Maximum Impedance (2)		Maximum Reverse Leakage		Maximum Noise Density @ 250 µA (3)	Maximum Regulation	
	V_Z	Z_Z	I_Z	I_R @ V_R			ΔV_Z	I_R
	Vdc	Ω	mA	µA	Vdc	µV/√Hz	Vdc	mA
1N6082B	4.3	18	20	2.0	1.5	1	0.75	2.0
1N6083B	4.7	10	10	2.0	2.0	1	0.50	1.0
1N6084B	5.1	10	5	2.0	3.0	1	0.30	0.25
1N6085B	5.6	40	1	2.0	4.5	1	0.10	0.05
1N6086B	6.2	45	1	0.5	5.6	1	0.10	0.01
1N6087B	6.8	50	1	0.05	6.2	1	0.10	0.01
1N6088B	7.5	50	1	0.01	6.8	1	0.10	0.01
1N6089B	8.2	60	1	0.01	7.5	1	0.10	0.01
1N6090B	9.1	60	1	0.01	8.2	2	0.10	0.01
1N6091B	10.0	60	1	0.01	9.1	2	0.10	0.01

Note 1 The JEDEC type numbers shown with a B suffix have a ±5% tolerance. No suffix indicates a ±20% tolerance. Suffix A denotes a ±10% tolerance, suffix C denotes a ±2% tolerance and suffix D denotes ±1% tolerance.

Note 2 The zener impedance is derived from the 60 Hz ac voltage, which results when an ac current having an rms value equal to 10% of the DC zener current (I_{ZT}) is superimposed on I_{ZT}.

Note 3 Measured from 1 KHz to 3 KHz in noise density measurement circuit shown on the following page.

MECHANICAL CHARACTERISTICS

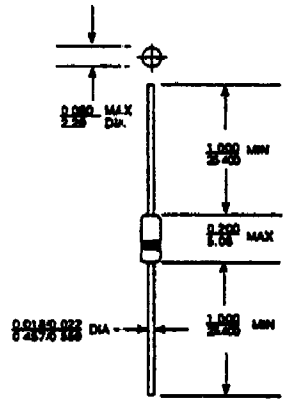

FIGURE 1 all dimensions in INCH mm

CASE: Hermetically sealed glass package (DO-35)
FINISH: Corrosion resistant. Leads are tin plated.
THERMAL RESISTANCE: 200°C/W junction to lead at 0.375-inches from body.
POLARITY: Cathode banded.
WEIGHT: 0.2 grams (typ).

This series also available in DO-7 package. Consult factory for availability.

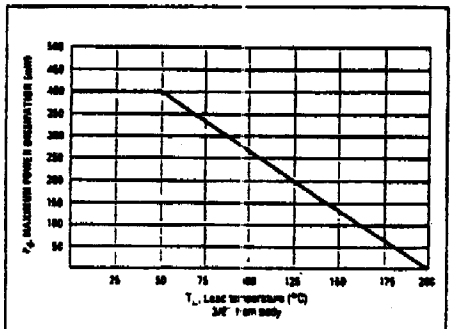

Figure 2 POWER DERATING

Quality Semi-Conductors