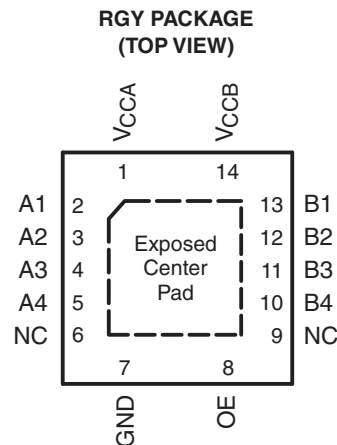
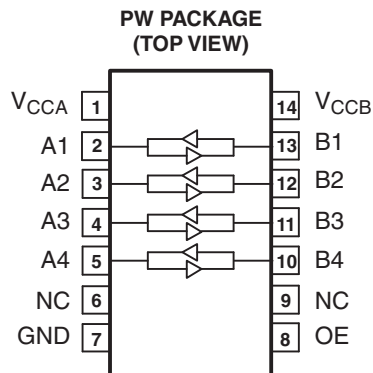


4-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTOMATIC DIRECTION SENSING AND ± 15 -kV ESD PROTECTION

FEATURES

- Qualified for Automotive Applications
- 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - A Port
 - 2500-V Human-Body Model (A114-B)
 - 200-V Machine Model (A115-A)
 - 1500-V Charged-Device Model (C101)
 - B Port
 - ± 15 -kV Human-Body Model (A114-B)
 - 200-V Machine Model (A115-A)
 - 1500-V Charged-Device Model (C101)



NC – No internal connection

For RGY, if the exposed center pad is used, it must be connected only to as a secondary ground or left electrically open.

DESCRIPTION/ORDERING INFORMATION

This 4-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB} .

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The TXB0104 is designed so that the OE input circuit is supplied by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	QFN – RGY	Reel of 1000	TXB0104QRGYRQ1	YE04Q1
	TSSOP – PW	Reel of 2000	TXB0104QPWRQ1	YE04Q1

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TERMINAL FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1	V _{CCA}	A-port supply voltage 1.2 V ≤ V _{CCA} ≤ 3.6 V and V _{CCA} ≤ V _{CCB} .
2	A1	Input/output 1. Referenced to V _{CCA} .
3	A2	Input/output 2. Referenced to V _{CCA} .
4	A3	Input/output 3. Referenced to V _{CCA} .
5	A4	Input/output 4. Referenced to V _{CCA} .
6	NC	No connection. Not internally connected.
7	GND	Ground
8	OE	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .
9	NC	No connection. Not internally connected.
10	B4	Input/output 4. Referenced to V _{CCB} .
11	B3	Input/output 3. Referenced to V _{CCB} .
12	B2	Input/output 2. Referenced to V _{CCB} .
13	B1	Input/output 1. Referenced to V _{CCB} .
14	V _{CCB}	B-port supply voltage 1.65 V ≤ V _{CCB} ≤ 5.5 V.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CCA}	Supply voltage range		–0.5	4.6	V
V _{CCB}			–0.5	6.5	
V _I	Input voltage range	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V _O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V _O	Voltage range applied to any output in the high or low state ⁽²⁾	A port	–0.5	V _{CCA} + 0.5	V
		B port	–0.5	V _{CCB} + 0.5	
I _{IK}	Input clamp current	V _I < 0		–50	mA
I _{OK}	Output clamp current	V _O < 0		–50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CCA} , V _{CCB} , or GND			±100	mA
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

THERMAL IMPEDANCE RATINGS

		TYP	UNIT
θ_{JA}	Package thermal impedance	PW package ⁽¹⁾	113
		RGY package ⁽²⁾	47

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

(2) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾⁽²⁾

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
V _{CCB}					1.65	5.5	
V _{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V _{CCI} × 0.65 ⁽³⁾	V _{CCI}	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	V _{CCA} × 0.65	5.5	
V _{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V _{CCI} × 0.35 ⁽³⁾	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	0	V _{CCA} × 0.35	
V _O	Voltage range applied to any output in the high-impedance or power-off state	A-port	1.2 V to 3.6 V	1.65 V to 5.5 V	0	3.6	V
		B-port			0	5.5	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
						4.5 V to 5.5 V	
T _A	Operating free-air temperature				−40	125	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.

(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.

(3) V_{CCI} is the supply voltage associated with the input port.

ELECTRICAL CHARACTERISTICS⁽¹⁾⁽²⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C		–40°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	
V _{OHA}		I _{OH} = –20 μA	1.2 V		1.1		V _{CCA} – 0.4		V
			1.4 V to 3.6 V						
V _{OLA}		I _{OL} = 20 μA	1.2 V		0.9		0.4		V
			1.4 V to 3.6 V						
V _{OHB}		I _{OH} = –20 μA		1.65 V to 5.5 V			V _{CCB} – 0.4		V
V _{OLB}		I _{OL} = 20 μA		1.65 V to 5.5 V			0.4		V
I _I	OE	V _I = V _{CC1} or GND	1.2 V to 3.6 V	1.65 V to 5.5 V	±1		±5		μA
I _{off}	A port	V _I or V _O = 0 to 3.6 V	0 V	0 V to 5.5 V	±1		±10		μA
	B port	V _I or V _O = 0 to 5.5 V	0 V to 3.6 V	0 V	±1		±10		
I _{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V	±1		±10		μA
I _{CCA}		V _I = V _{CC1} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	0.06		20 15 –15		μA
			1.4 V to 3.6 V	1.65 V to 5.5 V					
			3.6 V	0 V					
			0 V	5.5 V					
I _{CCB}		V _I = V _{CC1} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	3.4		20 –15 15		μA
			1.4 V to 3.6 V	1.65 V to 5.5 V					
			3.6 V	0 V					
			0 V	5.5 V					
I _{CCA} + I _{CCB}		V _I = V _{CC1} or GND, I _O = 0	1.2 V	1.65 V to 5.5 V	3.5		40		μA
			1.4 V to 3.6 V	1.65 V to 5.5 V					
I _{CCZA}		V _I = V _{CC1} or GND, I _O = 0, OE = GND	1.2 V	1.65 V to 5.5 V	0.05		15		μA
			1.4 V to 3.6 V	1.65 V to 5.5 V					
I _{CCZB}		V _I = V _{CC1} or GND, I _O = 0, OE = GND	1.2 V	1.65 V to 5.5 V	3.3		15		μA
			1.4 V to 3.6 V	1.65 V to 5.5 V					
C _i	OE		1.2 V to 3.6 V	1.65 V to 5.5 V	3				pF
C _{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V	5				pF
	B port	11							

(1) V_{CCI} is the supply voltage associated with the input port.(2) V_{CCO} is the supply voltage associated with the output port.

TIMING REQUIREMENTS

 $T_A = 25^{\circ}\text{C}$, $V_{CCA} = 1.2\text{ V}$

			$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
Data rate			20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	50	ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ (unless otherwise noted)

			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			40		40		40		40		Mbps
t_w	Pulse duration	Data inputs	25		25		25		25		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted)

			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			55		55		55		55		Mbps
t_w	Pulse duration	Data inputs	18		18		18		18		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			75		80		100		Mbps
t_w	Pulse duration	Data inputs	13		12		10		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
Data rate			100		100		Mbps
t_w	Pulse duration	Data inputs	10		10		ns

SWITCHING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	6.9	5.7	5.3	5.5	ns
	B	A	7.4	6.4	6	5.8	
t_{en}	OE	A	1	1	1	1	μs
		B	1	1	1	1	
t_{dis}	OE	A	320	320	320	330	ns
		B	150	110	150	110	
t_{rA} , t_{fA}	A-port rise and fall times		4.2	4.2	4.2	4.2	ns
t_{rB} , t_{fB}	B-port rise and fall times		2.1	1.5	1.2	1.1	ns

SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		V _{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	15.9		13.1		13		12.9		ns
	B	A	17.2		15		14.7		16.7		
t _{en}	OE	A	1		1		1		1		μs
		B	1		1		1		1		
t _{dis}	OE	A	340		280		280		300		ns
		B	220		220		220		220		
t _{rA} , t _{fA}	A-port rise and fall times		7.1		7.1		7.1		7.1		ns
t _{rB} , t _{fB}	B-port rise and fall times		6.5		5.2		4.8		4.7		ns

SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		V _{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	14		10.7		9.8		9.5		ns
	B	A	15		11.4		10.6		10.1		
t _{en}	OE	A	1		1		1		1		μs
		B	1		1		1		1		
t _{dis}	OE	A	280		250		250		250		ns
		B	220		220		220		220		
t _{rA} , t _{fA}	A-port rise and fall times		6.2		6.1		6.1		6.1		ns
t _{rB} , t _{fB}	B-port rise and fall times		5.8		5.2		4.8		4.7		ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		V _{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	9.3		8.2		7.7		ns
	B	A	9.6		8.1		7.4		
t _{en}	OE	A	1		1		1		μs
		B	1		1		1		
t _{dis}	OE	A	220		220		220		ns
		B	220		220		220		
t _{rA} , t _{fA}	A-port rise and fall times		5		5		5		ns
t _{rB} , t _{fB}	B-port rise and fall times		4.6		4.8		4.7		ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 3.3 V ± 0.3 V		V _{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A	B	7.7		7		ns
	B	A	7.9		6.8		
t _{en}	OE	A	1		1		μs
		B	1		1		
t _{dis}	OE	A	280		280		ns
		B	220		220		
t _{rA} , t _{fA}	A-port rise and fall times		4.5		4.5		ns
t _{rB} , t _{fB}	B-port rise and fall times		4.1		4.7		ns

OPERATING CHARACTERISTICS $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V _{CCA}							UNIT
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			V _{CCB}							
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C _{pdA}	A-port input, B-port output	C _L = 0, f = 10 MHz, t _r = t _f = 1 ns, OE = V _{CCA} (outputs enabled)	7.8	10	9	8	8	8	9	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C _{pdB}	A-port input, B-port output		38.1	28	28	28	29	29	29	
	B-port input, A-port output		25.4	19	18	18	19	21	22	
C _{pdA}	A-port input, B-port output	C _L = 0, f = 10 MHz, t _r = t _f = 1 ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C _{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.04	

PRINCIPLES OF OPERATION

Applications

The TXB0104 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

Architecture

The TXB0104 architecture (see [Figure 1](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0104 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at $V_{CCO} = 1.2\text{ V}$ to 1.8 V, 50 Ω at $V_{CCO} = 1.8\text{ V}$ to 3.3 V, and 40 Ω at $V_{CCO} = 3.3\text{ V}$ to 5 V.

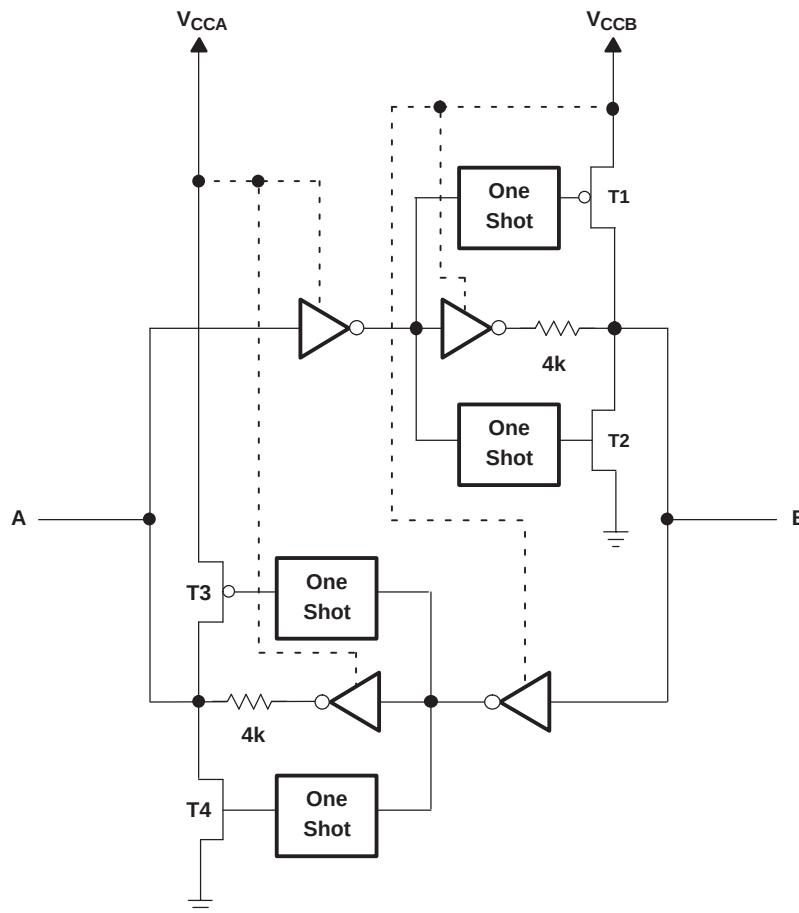
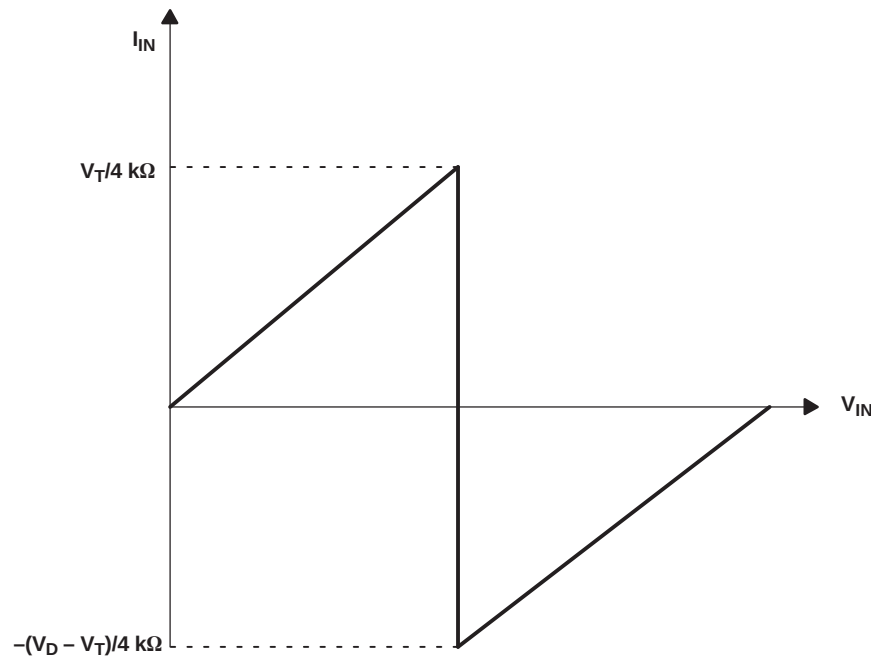


Figure 1. Architecture of TXB0104 I/O Cell

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0104 are shown in Figure 2. For proper operation, the device driving the data I/Os of the TXB0104 must have drive strength of at least ± 2 mA.



- A. V_T is the input threshold voltage of the TXB0104 (typically $V_{CC}/2$).
- B. V_D is the supply voltage of the external driver.

Figure 2. Typical I_{IN} vs V_{IN} Curve

Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0104 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0 \text{ V}$).

Enable and Disable

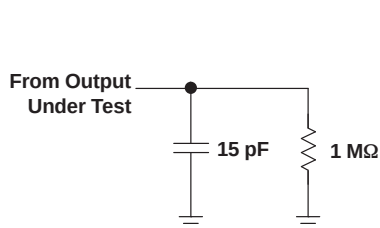
The TXB0104 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistors on I/O Lines

The TXB0104 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0104 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k Ω to ensure that they do not contend with the output drivers of the TXB0104.

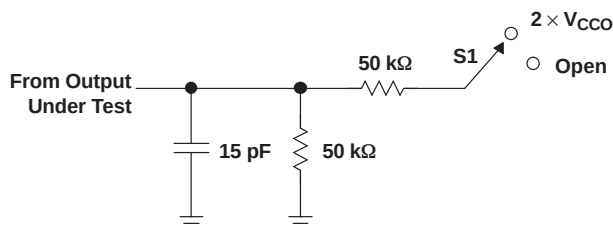
For the same reason, the TXB0104 should not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

PARAMETER MEASUREMENT INFORMATION



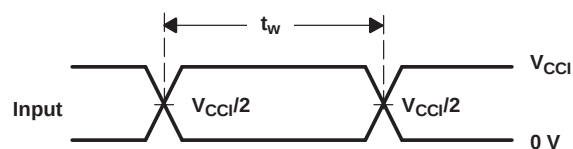
LOAD CIRCUIT FOR MAX DATA RATE,
PULSE DURATION PROPAGATION
DELAY OUTPUT RISE AND FALL TIME
MEASUREMENT

V_{CCO}	V_{TP}
$1.8\text{ V} \pm 0.15\text{ V}$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	0.3 V

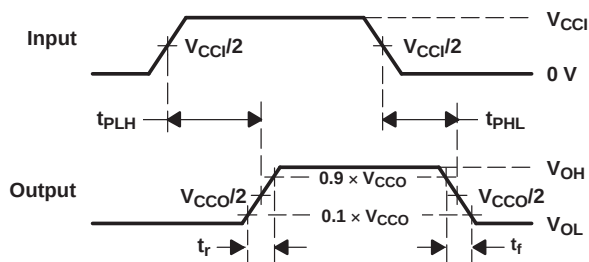


LOAD CIRCUIT FOR
ENABLE/DISABLE
TIME MEASUREMENT

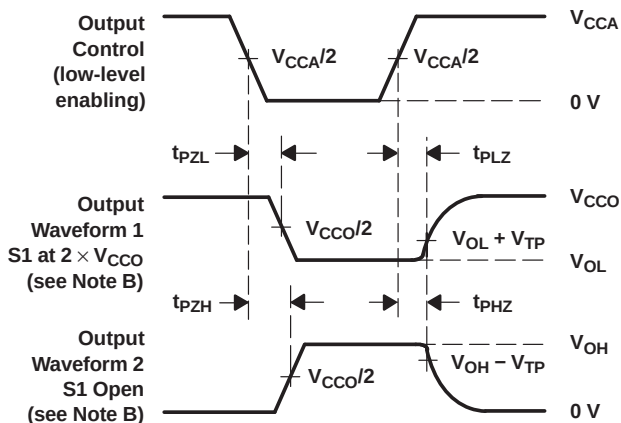
TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $dv/dt \geq 1\text{ V/ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. V_{CCI} is the V_{CC} associated with the input port.
 F. V_{CCO} is the V_{CC} associated with the output port.
 G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TXB0104QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXB0104QRGYRQ1	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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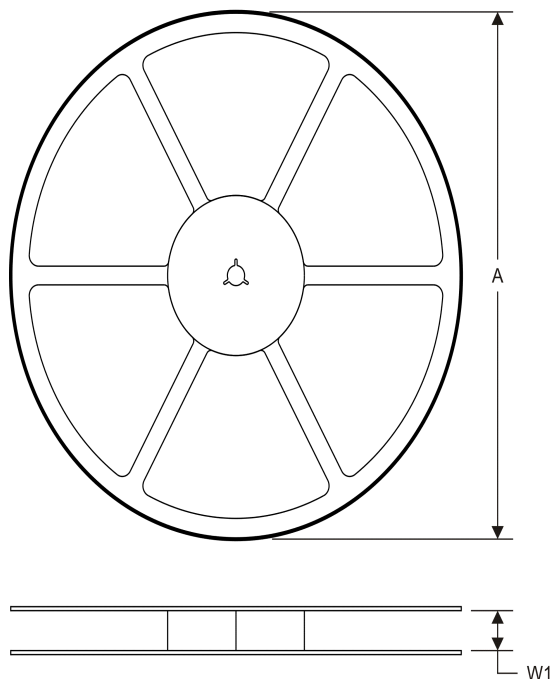
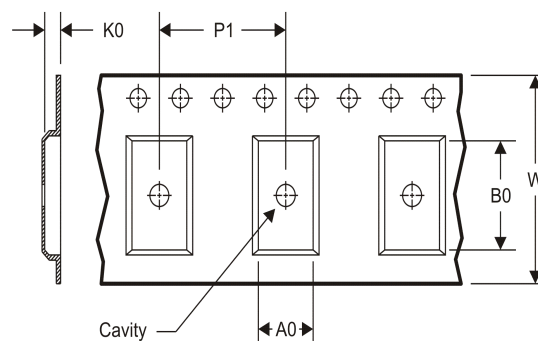
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXB0104-Q1 :

- Catalog: [TXB0104](#)

NOTE: Qualified Version Definitions:

-
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


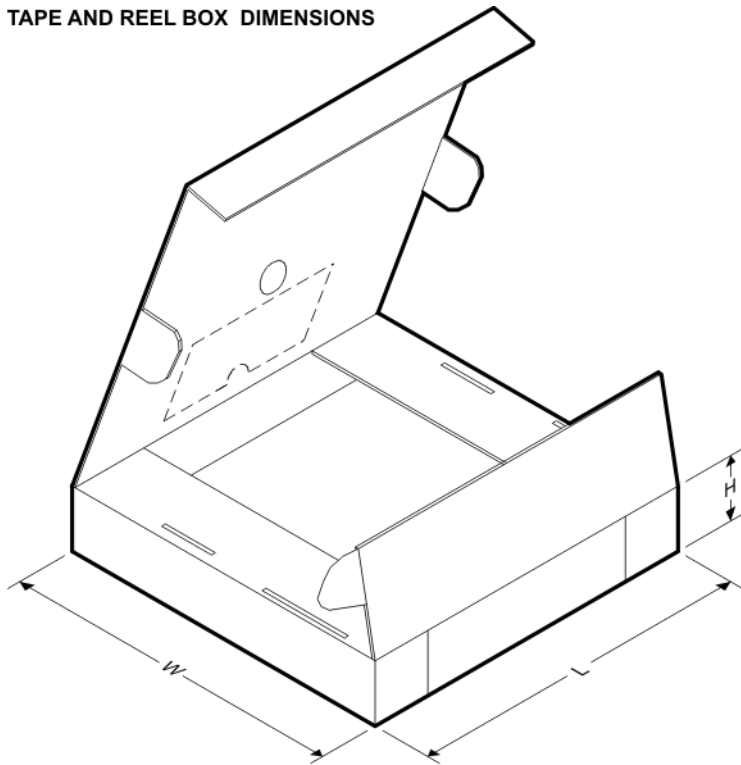
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0104QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXB0104QRGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

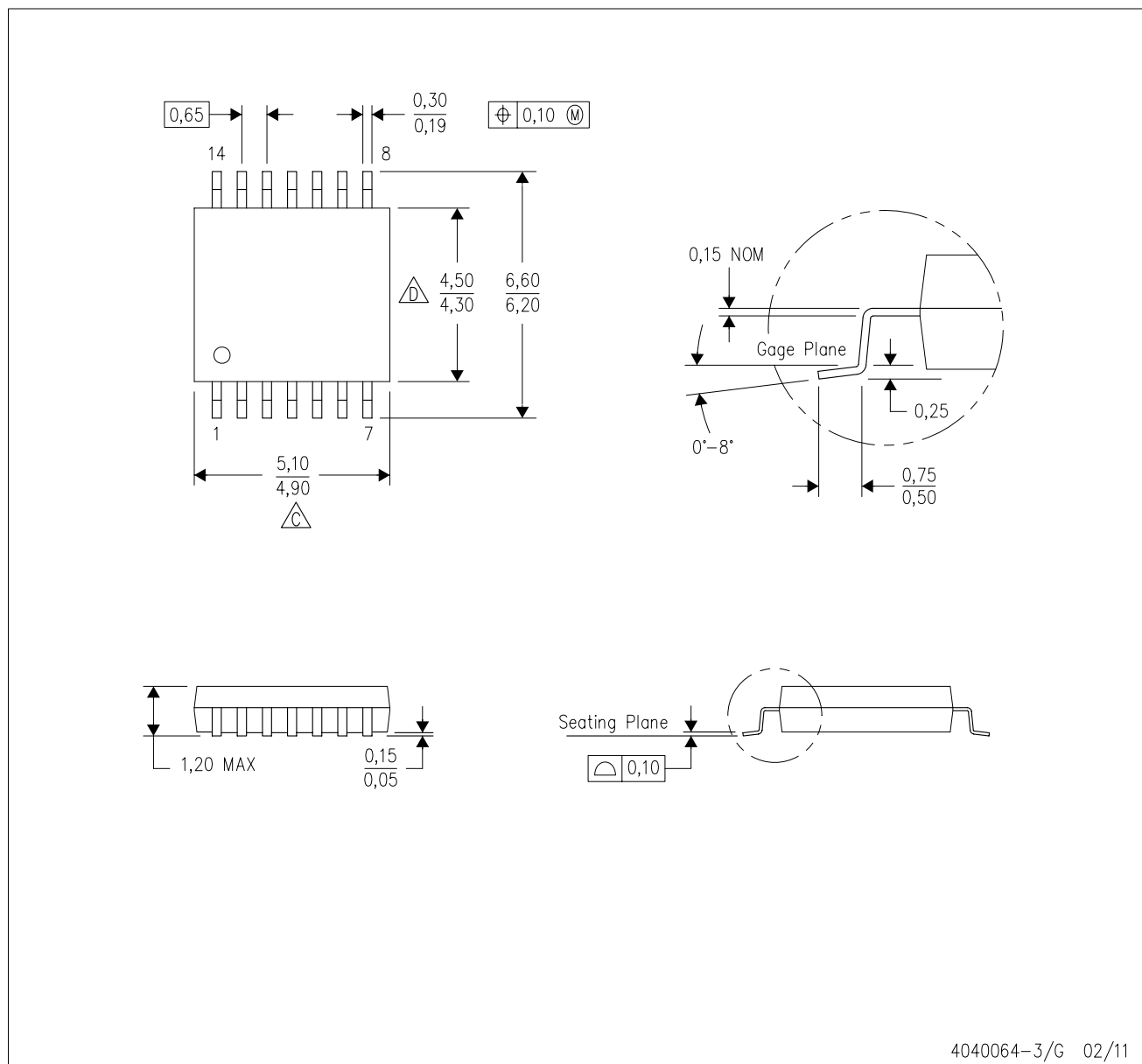


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0104QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
TXB0104QRGYRQ1	VQFN	RGY	14	3000	367.0	367.0	35.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

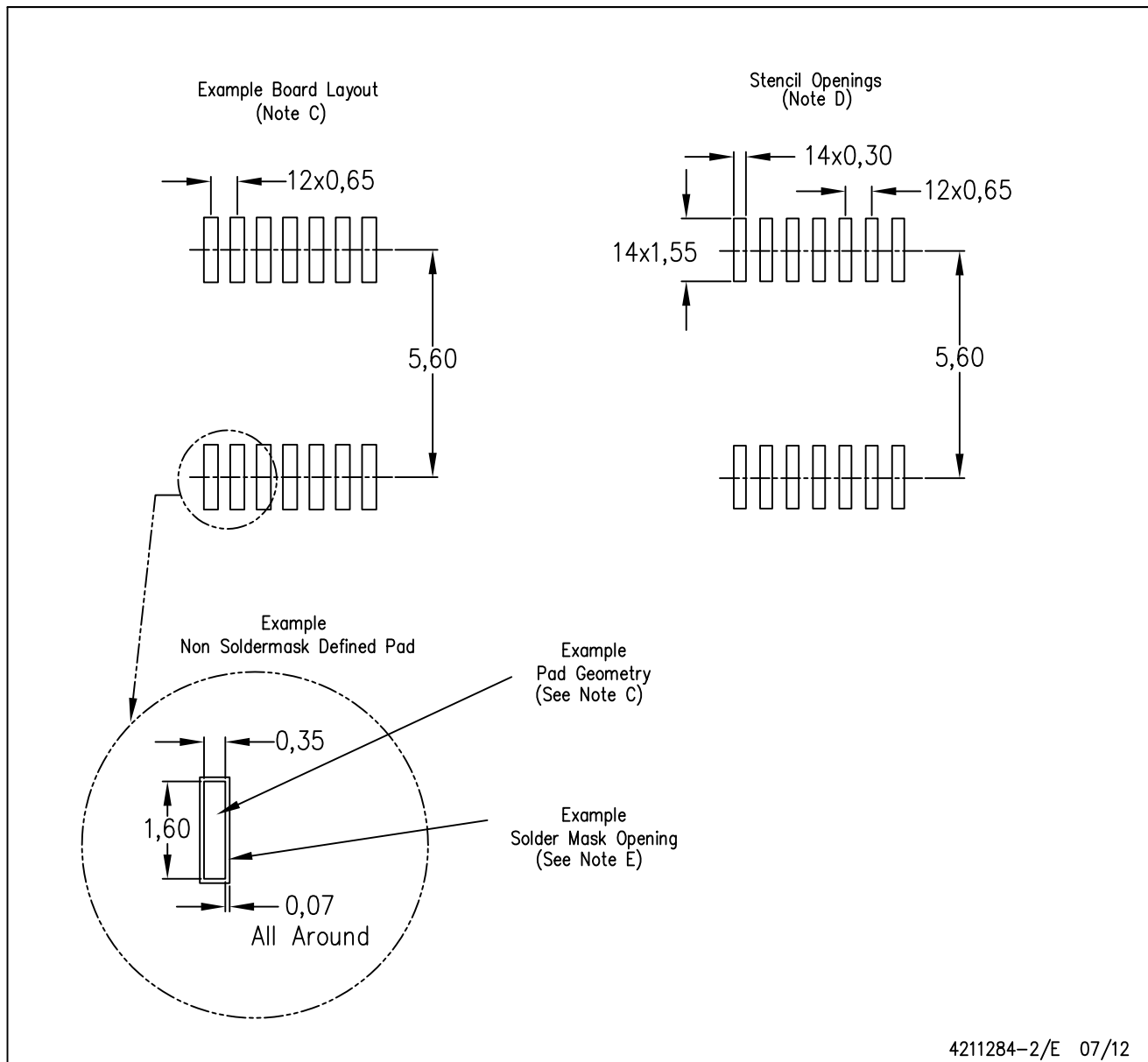


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

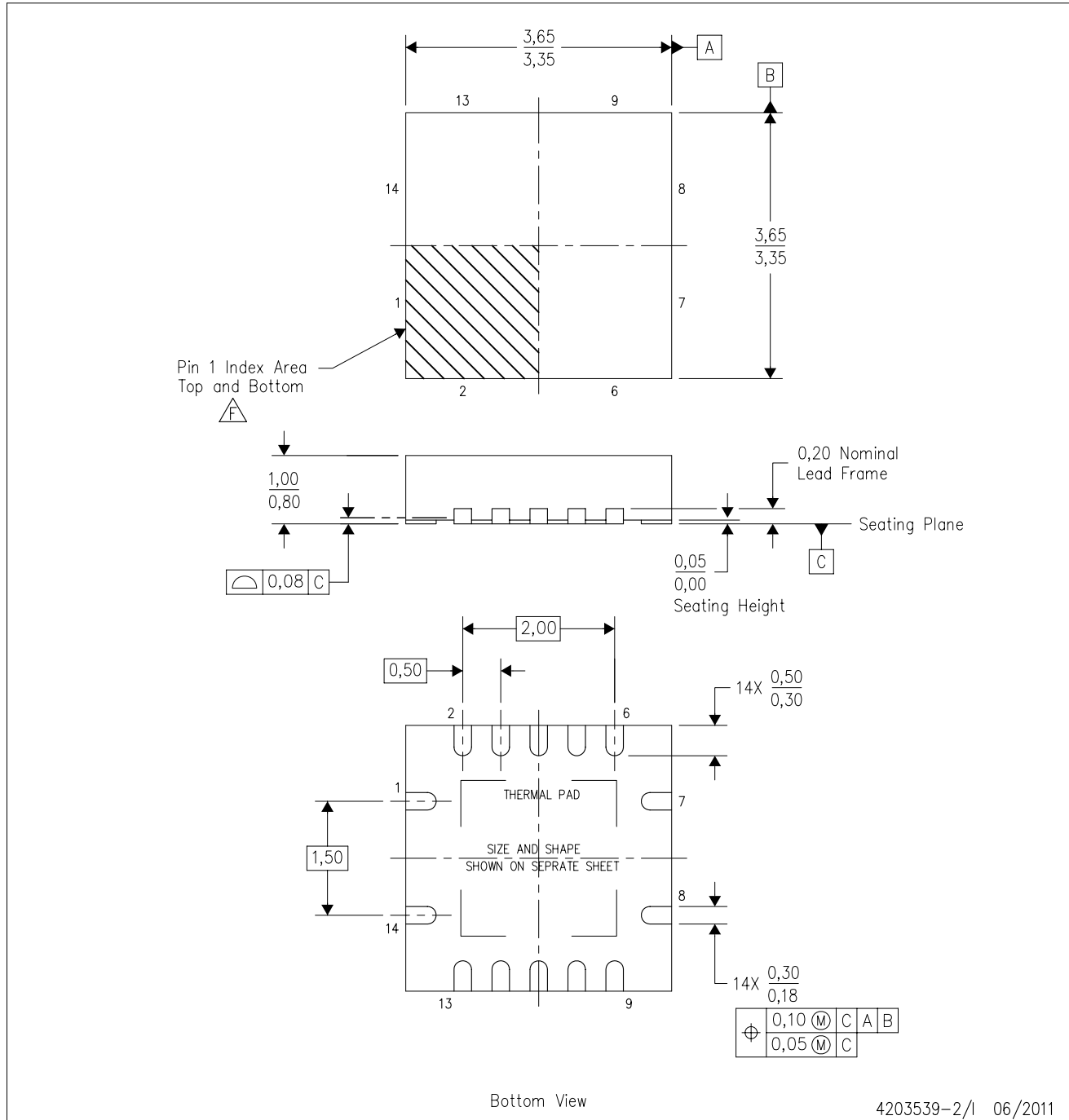


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

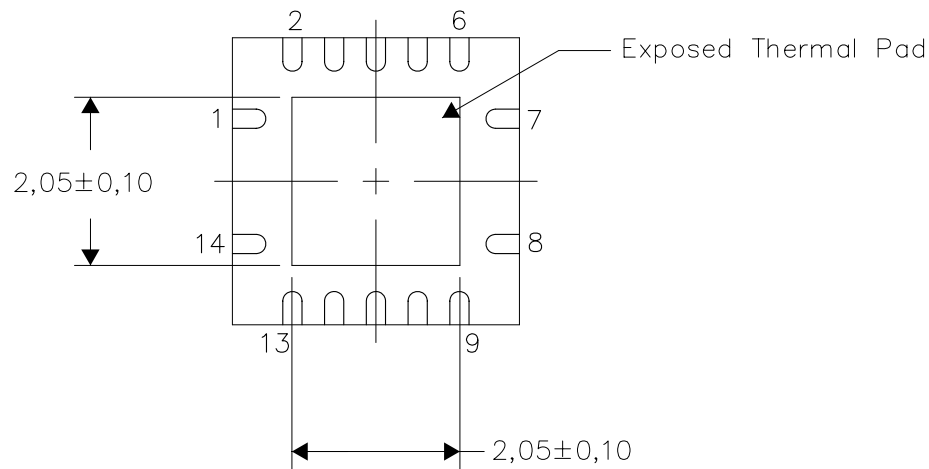
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

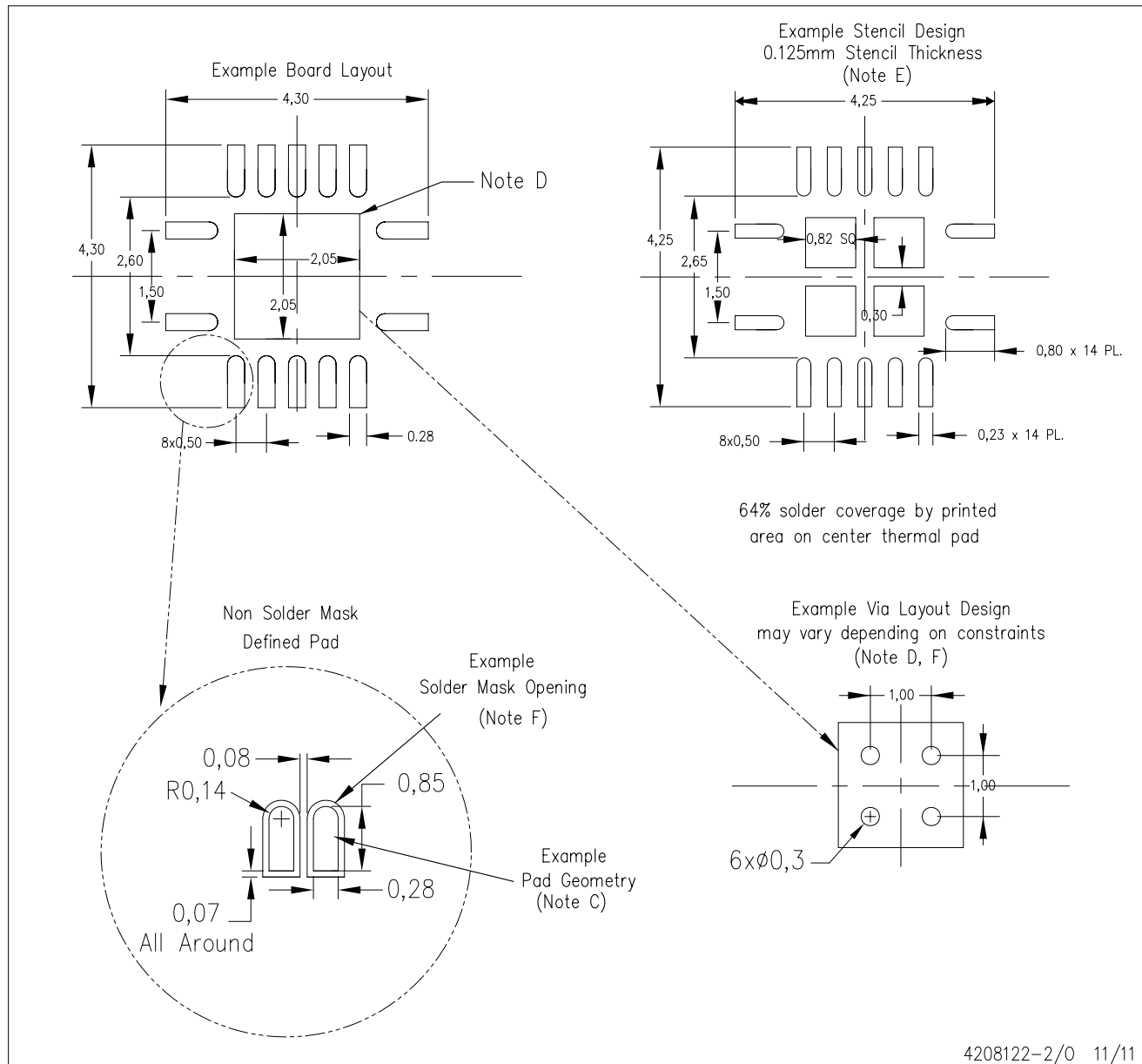
Exposed Thermal Pad Dimensions

4206353-2/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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