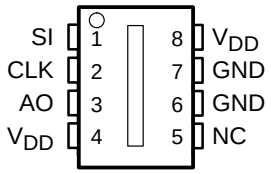
- **Contains 64-Bit Static Shift Register**
- **Contains Analog Buffer With Sample and Hold for Analog Output Over Full Clock Period**
- **Single-Supply Operation**
- **Operates With 500-kHz Shift Clock**
- **8-Pin Clear Plastic DIP Package**
- **Advanced LinCMOS™ Technology**

(TOP VIEW)



NC – No internal connection

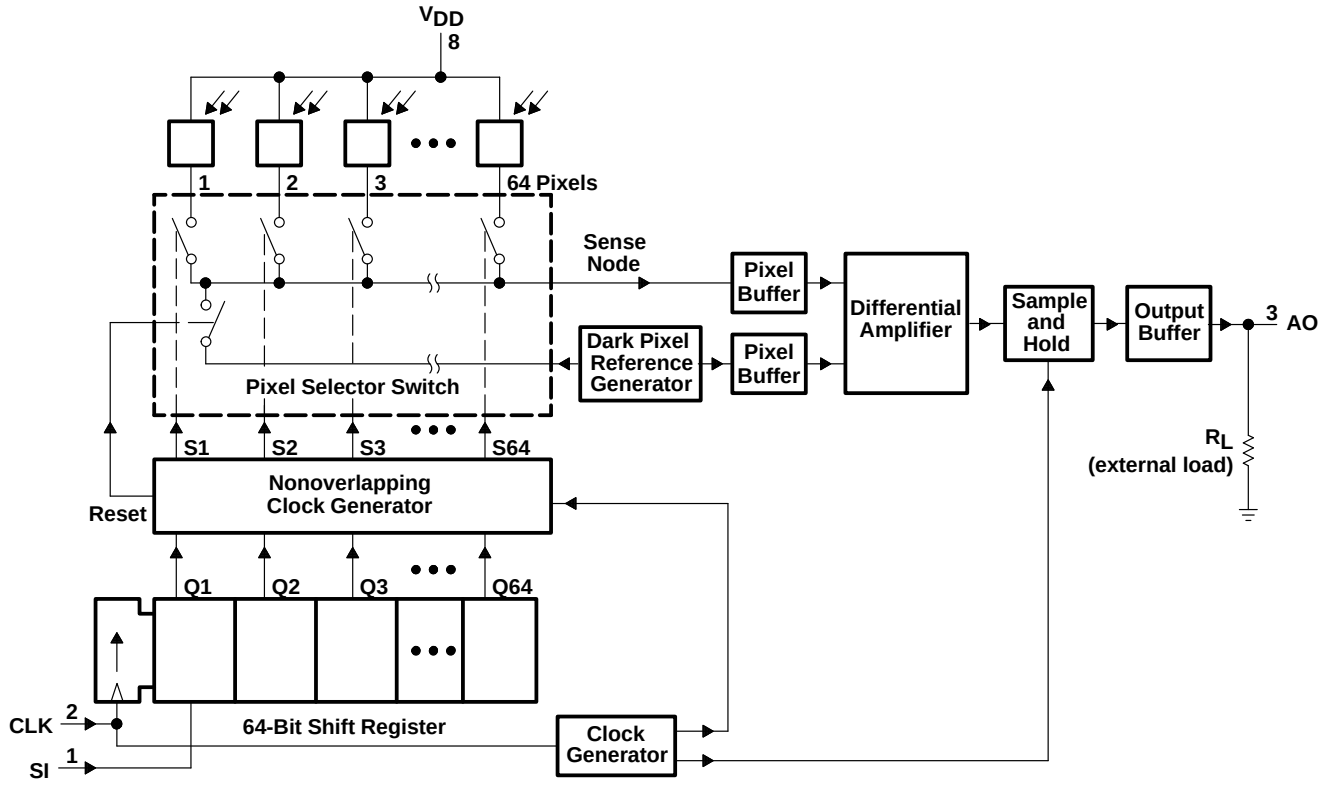
description

The TSL213 integrated opto sensor consists of 64 charge-mode pixels arranged in a 64 × 1 linear array. Each pixel measures 120 µm × 70 µm with 125-µm center-to-center spacing. Operation is simplified by internal logic requiring only clock and start-integration-pulse signals.

The TSL213 is intended for use in a wide variety of applications including linear and rotary encoding, linear positioning, edge and mark detection, and contact imaging.

The TSL213 is supplied in an 8-pin dual-in-line clear plastic package.

functional block diagram



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
AO	3	Analog output
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.
NC	5	No internal connection
SI	1	Serial input. The serial input defines the end of the integration period and initiates the pixel output sequence.
V_{DD}	4, 8	Supply voltages. These supply power to the analog and digital circuits.

detailed description

sensor elements

The line of sensor elements, called pixels, consists of 64 discrete photosensing areas. Light energy striking a pixel generates electron-hole pairs in the region under the pixel. The field generated by the bias on the pixel causes the electrons to collect in the element while the holes are swept into the substrate. The amount of charge accumulated in each element is directly proportional to the amount of incident light and the integration time.

device operation

Operation of the 64 × 1 array sensor consists of two time periods: an integration period during which charge is accumulated in the pixels and an output period during which signals are transferred to the output. The integration period is defined by the interval between serial-input (SI) pulses and includes the output period (see Figure 1). The required length of the integration period depends upon the amount of incident light and the desired output signal level.

sense node

On completion of the integration period, the charge contained in each pixel is transferred in turn to the sense node under the control of the clock (CLK) and SI signals. The signal voltage generated at this node is directly proportional to the amount of charge and inversely proportional to the capacitance of the sense node.

reset

An internal reset signal is generated by the nonoverlapping clock generator (NOCG) and occurs every clock cycle. Reset establishes a known voltage on the sense node in preparation for the next charge transfer. This voltage is used as a reference level for the differential signal amplifier.

shift register

The 64-bit shift register controls the transfer of charge from the pixels to the output stages and provides timing signals for the NOCG. The SI signal provides the input to the shift register and is shifted under direct control of the clock.

The output period is initiated by the presence of the SI input pulse coincident with a rising edge of CLK (see Figures 1 and 2). The analog output voltage corresponds to the level of the first pixel after settling time (t_s) and remains constant for a minimum time, t_v. A voltage corresponding to each succeeding pixel is available at each rising edge of the clock. The output period ends on the rising edge of the 65th clock cycle, at which time the output assumes the high-impedance state. The 65th clock cycle terminates the output of the last pixel and clears the shift register in preparation for the next SI pulse. To achieve minimum integration time, the SI pulse may be present on the 66th rising edge of the clock to immediately reinitiate the output phase. When the output period has been initiated by an SI pulse, the clock must be allowed to complete 65 positive-going transitions in order to reset the internal logic to a known state.

sample and hold

The sample-and-hold signal generated by the NOCG is used to hold the analog output voltage of each pixel constant until the next pixel is clocked out. The signal is sampled while CLK is high and held constant while CLK is low.

nonoverlapping clock generators

The NOCG circuitry provides internal control signals for the sensor, including reset and pixel-charge sensing. The signals are synchronous and are controlled by the outputs of the shift register.

initialization

Initialization of the sensor elements may be necessary on power up or during operation after any period of clock or SI inactivity exceeding the integration time. The initialization phase consists of 12 to 15 consecutively performed output cycles and clears the pixels of any charge that may have accumulated during the inactive period.

output enable

The internally-generated output-enable signal enables the output stage of the sensor during the output period (64 clock cycles). During the remainder of the integration period, the output stage is in the high-impedance state that allows output interconnections of multiple devices without interference.

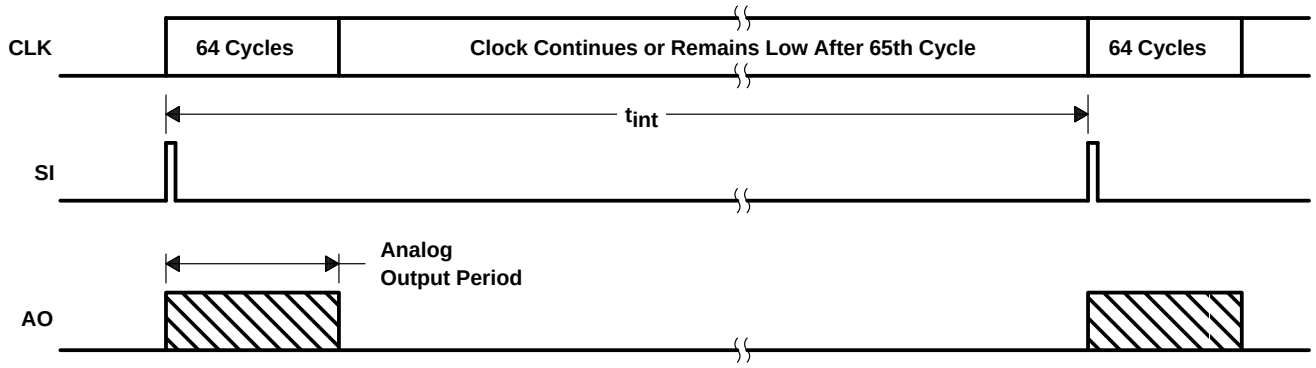


Figure 1. Timing Waveforms

absolute maximum ratings, T_A = 25°C (unless otherwise noted) (see Note 1)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 7 V
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating case temperature range, T_C (see Note 2) . . . . . –10°C to 85°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the network GND.
2. Case temperature is the surface temperature of the plastic package measured directly over the integrated circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5		5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ		750		nm
Clock input frequency, f_{clock}	10		500	kHz
Pulse duration, CLK low, t_w	1			μs
Sensor integration time, t_{int}		5		ms
Setup time, SI before CLK↑, $t_{su(SI)}$	50			ns
Hold time, SI after CLK↑, $t_{h(SI)}$	50			ns
External resistive load, AO, R_L		330		Ω
Total number of TSL213 outputs connected together			10	
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{DD} = 5 V, T_A = 25°C, f_{clock} = 180 kHz, λ_p = 565 nm, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm² (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output voltage saturation level	E_e = 51 μW/cm²	3	3.4		V
Analog output voltage (white, average over 64 pixels)		1.75	2		V
Analog output voltage (dark, each pixel)	E_e = 0		0.25	0.4	V
Output voltage (white) change with change in V_{DD}	V_{DD} = 5 V ±5%		±2%		
Dispersion of analog output voltage	See Note 4			±10%	
Linearity of analog output voltage	See Note 5	0.85		1.15	
Pixel recovery time	See Note 6		25	40	ms
Supply current	I_{DD} Avg		4	9	mA
High-level input current	$V_I = V_{DD}$			0.5	μA
Low-level input current	V_I = 0			0.5	μA
Input capacitance			5		pF

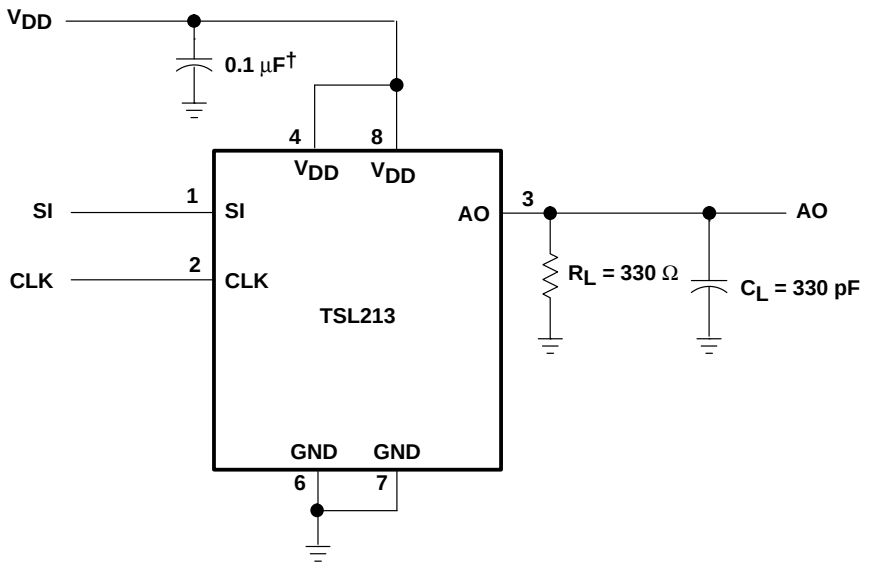
NOTES: 3. The input irradiance (E_e) is supplied by an LED array with λ_p = 565 nm.
4. Dispersion of analog output voltage is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test.
5. Linearity of analog output voltage is calculated by averaging over 64 pixels and measuring the maximum deviation of the voltage at 2 ms and 3.5 ms from a line drawn between the voltage at 2.5 ms and the voltage at 5 ms.
6. Pixel recovery time is the time required for a pixel to go from the analog-output-voltage (white, average over 64 pixels) level to the analog-output-voltage (dark, each pixel) level or vice versa after a step change in light input.

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm², f_{clock} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Settling time	See Figure 2 and Note 7			1	μs
t_v	Valid time				1/2 f_{clock}	μs

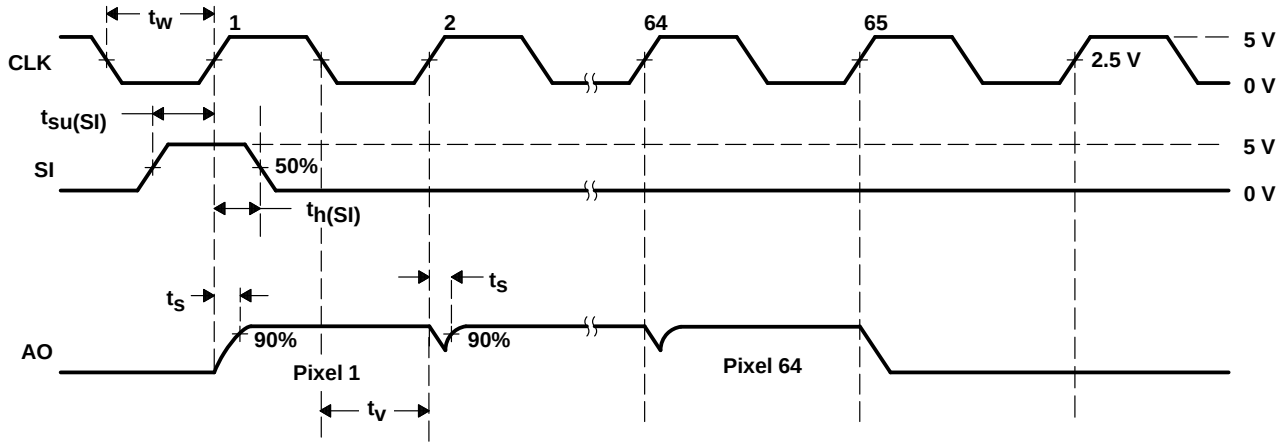
NOTE 7: Clock duty cycle is assumed to be 50%.

PARAMETER MEASUREMENT INFORMATION



† Supply bypass capacitor with short leads should be placed as close to the device as possible.

TEST CIRCUIT



OPERATIONAL WAVEFORMS

Figure 2. Test Circuit and Operational Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED RESPONSIVITY vs WAVELENGTH OF INCIDENT LIGHT

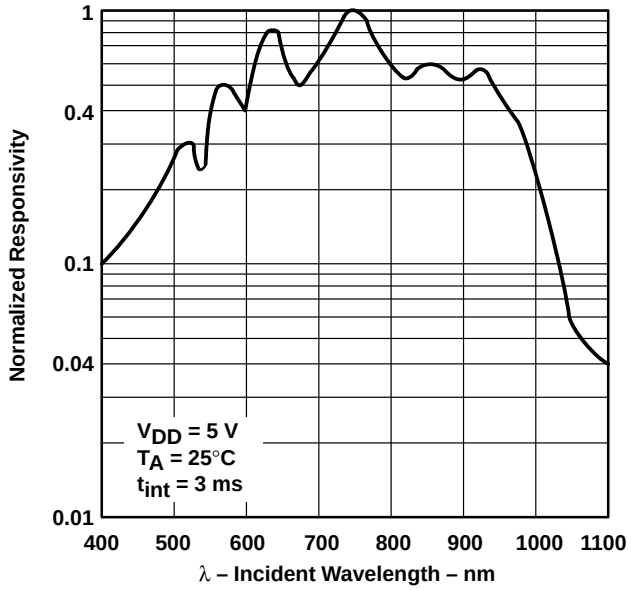


Figure 3

INTEGRATION TIME vs IRRADIANCE FOR CONSTANT AVERAGE ANALOG OUTPUT VOLTAGE

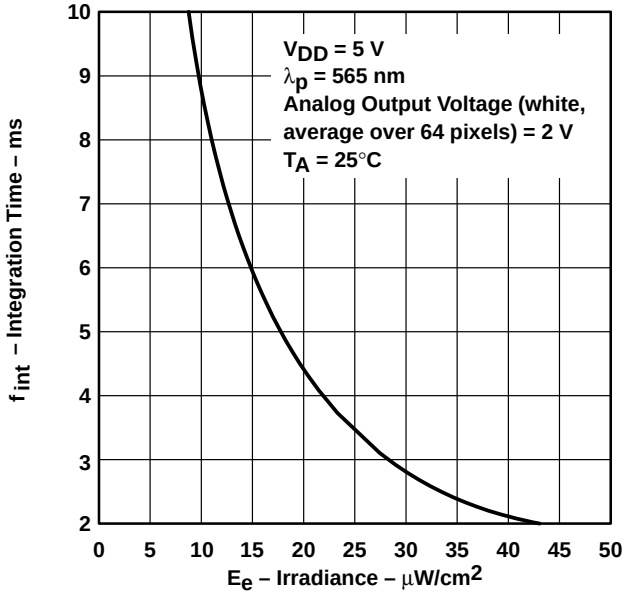


Figure 4

ANALOG OUTPUT VOLTAGE (DARK) vs INTEGRATION TIME

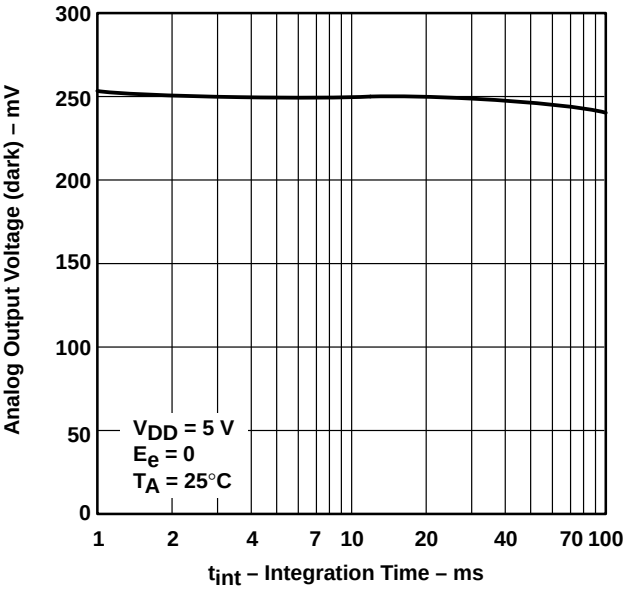


Figure 5

NORMALIZED OUTPUT VOLTAGE vs INTEGRATION TIME

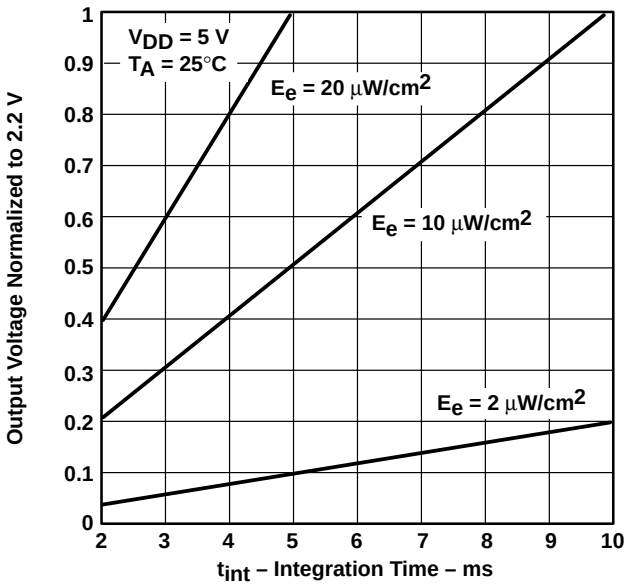
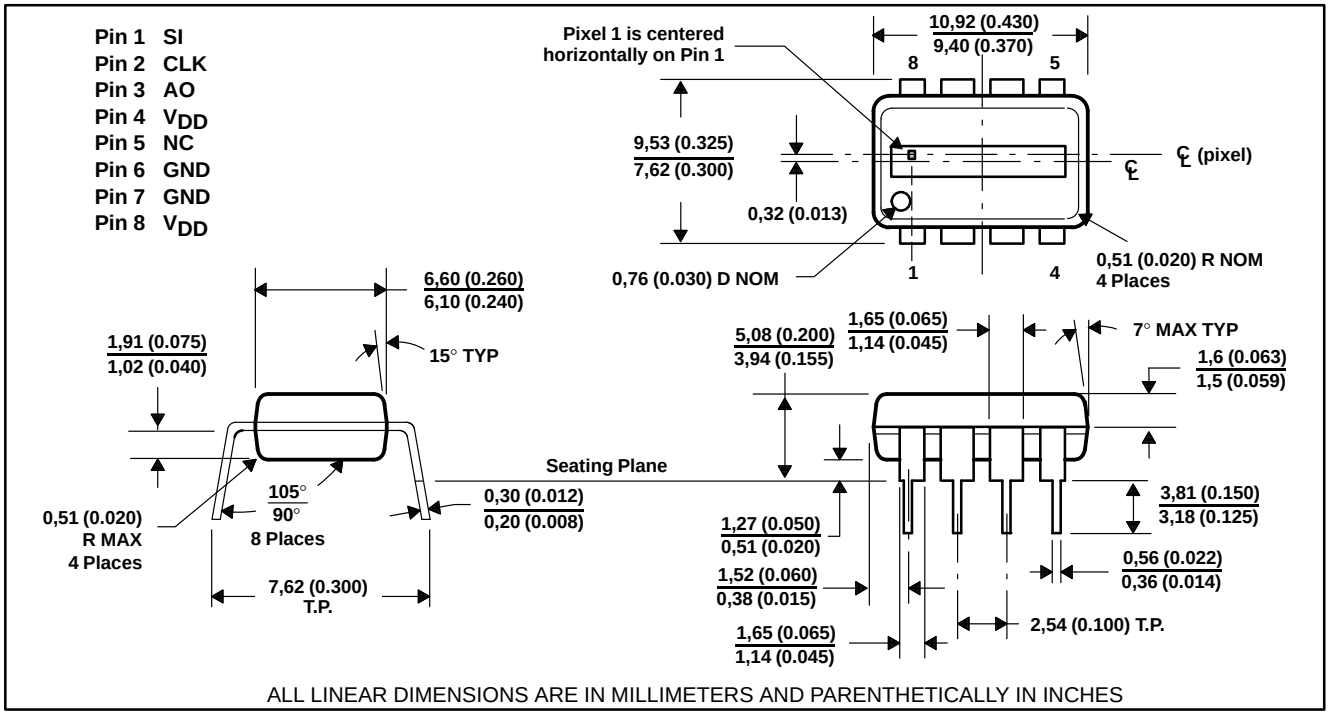


Figure 6

mechanical data

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated with an electrically nonconductive clear plastic compound.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

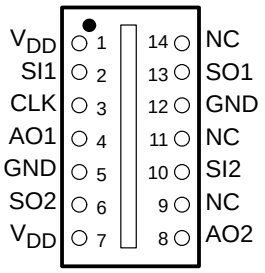
Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

- **Contains Two 64-Bit Static Shift Registers**
- **Offers Extendable Data I/O for Expanding the Number of Sensors**
- **Contains Analog Buffer With Sample-and-Hold for Analog Output Over Full Clock Period**
- **Single-Supply Operation**
- **Operates With 500-kHz Shift Clock**
- **14-Pin Encapsulated Clear Plastic Package**
- **Advanced LinCMOS™ Technology**

(TOP VIEW)



NC – No internal connection

description

The TSL215 integrated opto sensor consists of two sections of 64 charge-mode pixels arranged in a 128 × 1 linear array. Each pixel measures 120 µm × 70 µm with 125-µm center-to-center spacing. Operation is simplified by internal logic requiring only clock and start-integration-pulse signals.

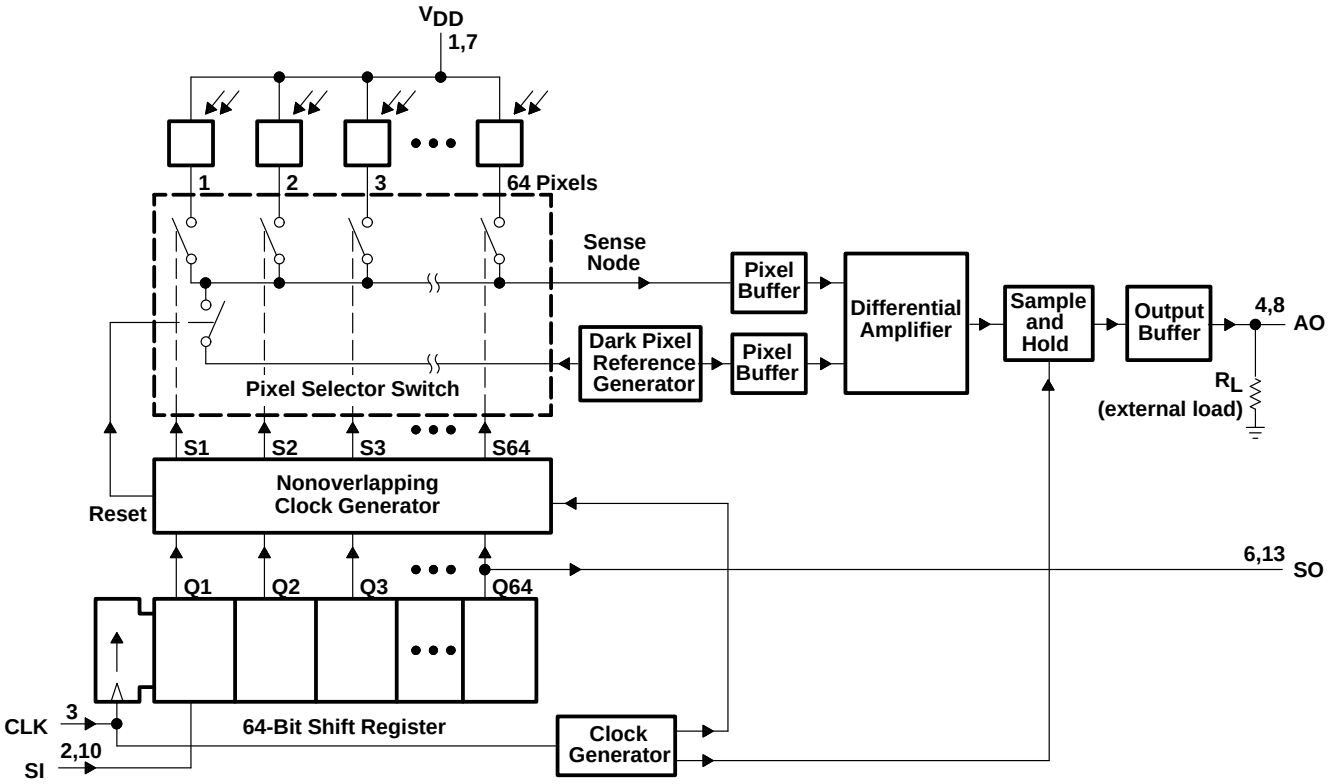
The TSL215 is intended for use in a wide variety of applications including linear and rotary encoding, bar-code reading, edge detection and positioning, and contact imaging.

The TSL215 is supplied in a 14-pin dual-in-line clear plastic package.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram of each section



Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
AO1	4	Analog output of section 1
AO2	8	Analog output of section 2
CLK	3	Clock. The clock controls charge transfer, pixel output, and reset.
GND	5, 12	Ground (substrate). All voltages are referenced to the substrate.
NC	9, 11, 14	No internal connection
SI1	2	Serial input (section 1). The serial input defines the end of the integration period and initiates the pixel output sequence.
SI2	10	Serial input (section 2). The serial input defines the end of the integration period and initiates the pixel output sequence.
SO1	13	Serial output (section 1). The serial output provides a signal to drive the SI2 input.
SO2	6	Serial output (section 2). The serial output provides a signal to drive the SI1 input of another TSL215 sensor for cascading.
V_{DD}	1, 7	Supply voltage. These supply power to the analog and digital circuits.

detailed description

sensor elements

The line of sensor elements, called pixels, consists of 128 discrete photosensing areas. Light energy striking a pixel generates electron-hole pairs in the region under the pixel. The field generated by the bias on the pixel causes the electrons to collect in the element while the holes are swept into the substrate. The amount of charge accumulated in each element is directly proportional to the amount of incident light and the integration time.

device operation

Operation of the 128 × 1 array sensor is a function of two time periods: an integration period during which a charge is accumulated in the pixels and an output period during which signals are transferred to the output. The integration period is defined by the interval between the externally supplied (SI) pulses and includes the output period (see Figure 1). The required length of the integration period depends on the amount of incident light and the desired output signal level. A single TSL215 can be connected in either a serial or parallel configuration.

serial configuration

The serial connection shown in Figure 1 is accomplished by connecting the analog outputs (AO1 and AO2) together and connecting the SO1 output to the SI2 input. As shown in Figure 1, the external SI signal is supplied to only the SI1 input. This causes the first section of 64 pixels to be clocked out in synchronization with CLK. In conjunction with the 64th pixel, the SI pulse is shifted out on the SO1 output. This SO1 pulse is then fed to the SI2 input. The 65th clock cycle terminates the output of the last pixel from the first section and clears the shift register of that section in preparation for the next SI pulse to that section. The rising edge of the 65th cycle also puts AO1 into the high-impedance state. The appearance of the SI2 signal and the 65th clock cycle initiates the output cycle of the second section. The second section of 64 pixels appears at AO2, and the SO2 signal is shifted out on the 128th clock cycle. The rising edge of the 129th clock cycle resets the second section and puts AO2 into the high-impedance state. Both AO1 and AO2 remain in this high-impedance state until a new external SI pulse appears on SI1. When the TSL215 is connected as shown in Figure 1, the analog output appears as a continuous string representing the 128 pixels.

parallel configuration

Parallel operation of the TSL215 (see Figure 2) is accomplished by connecting the serial input lines (SI1 and SI2) together and connecting each AO line (AO1 and AO2) to its own load resistor (R_L). This supplies the external serial input pulse to both SI1 and SI2 simultaneously. Each AO line must be independent of the other line since both sections are active simultaneously. Pixels 1 through 64 appear on AO1, while pixels 65 through 128 appear on AO2. These two sections of 64 pixels begin clocking out concurrently, each on its respective output. On the 64th clock cycle, both SO1 and SO2 are shifted out of each respective register. The rising edge of the 65th cycle terminates the output of the 64th pixel from each section and also resets both section's shift registers. Both AO lines then go to the high-impedance state until the next external SI signal appears.

sense node

On completion of the integration period, the charge contained in each pixel is transferred in turn to the sense node under the control of the clock (CLK) and serial-input (SI) signals. The signal voltage generated at this node is directly proportional to the amount of charge and inversely proportional to the capacitance of the sense node.

reset

An internal reset signal is generated by the nonoverlapping clock generator (NOCG) and occurs every clock cycle. Reset establishes a known voltage on the sense node in preparation for the next charge transfer. This voltage is used as a reference level for the differential signal amplifier.

detailed description (continued)

shift register

Both 64-bit shift registers control the transfer of charge from the pixels to the output stages and provide timing signals for the NOCG. The serial input (SI) signal provides the input to the shift register and is shifted under direct control of CLK out to the serial output (SO) on the 64th clock cycle. This SO pulse can then be used as the SI pulse for the next section or next device.

The output period for each section is initiated by the presence of the SI input pulse coincident with a rising edge of CLK (see Figures 1, 2, and 3). The analog output voltage corresponds to the level of the first pixel after settling time (t_S) and remains constant for a minimum time (t_V). A voltage corresponding to each succeeding pixel is available at each rising edge of CLK. The output period of a section ends when the active section sees the rising edge of the 65th clock cycle, at which time the output assumes the high-impedance state. Once the output period has been initiated by an SI pulse, CLK must be allowed to complete [(n × 64)+1] (where n is the number of sections running in series) positive-going transitions in order to reset the internal logic to a known state. To achieve minimum integration time, the SI pulse may be present on the [(n × 64)+2] rising clock to immediately restart the output phase.

sample-and-hold

The sample-and-hold signal generated by the NOCG is used to hold the analog output voltage of each pixel constant until the next pixel is clocked out. The signal is sampled while CLK is high and held constant while CLK is low.

nonoverlapping clock generators

The NOCG circuitry provides internal control signals for the sensor, including reset and pixel-charge sensing. The signals are synchronous and are controlled by the outputs of the shift register.

initialization

Initialization of the sensor elements may be necessary on power up or during operation after any period of CLK or SI inactivity exceeding the integration time. The initialization phase consists of 12 to 15 consecutively performed output cycles and clears the pixels of any charge that may have accumulated during the inactive period.

multiple-unit operation

Multiple-sensor devices can be connected together in a serial or parallel configuration. The serial connection is accomplished by connecting analog outputs (AO) together and connecting the SO output of each sensor device to the SI input of the next device. The SI signal is applied to only the first device. Each succeeding device receives its SI input from the SO output of the preceding device. For m-cascaded devices, the SI pulse is applied to the first device after every m•128th positive-going CLK transitions. A common clock signal is applied to all the devices simultaneously. Parallel operation of multiple devices is accomplished by supplying CLK and SI signals to all the devices simultaneously. The output of each device is then separately used for processing.

output enable

The internally generated output-enable signal enables the output stage of each section during the output period (64 clock cycles). During the remainder of the integration period, the output stage is in the high-impedance state that allows output interconnections of multiple devices without interference.

absolute maximum ratings, T_A = 25°C (unless otherwise noted) (see Note 1)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.5 V to 7 V
Digital output voltage range, V_O . . . . . –0.5 V to V_{DD} + 0.5 V
Digital output current, I_O . . . . . 3 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating case temperature range, T_C (see Note 2) . . . . . –10°C to 85°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the network GND.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5		5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Analog output external resistive load, R_L		330		Ω
Wavelength of light source, λ		750		nm
Clock input frequency, f_{clock}	10		500	kHz
Pulse duration, CLK low, $t_{w(CLKL)}$	1			µs
Sensor integration time, t_{int} (see Figures 1 and 2)		5		ms
Setup time, SI before CLK↑, $t_{su(SI)}$	50			ns
Hold time, SI after CLK↑, $t_{h(SI)}$	50			ns
Total number of TSL215 outputs connected together			8	
Operating free-air temperature, T_A	0		70	°C

electrical characteristics , V_{DD} = 5 V, T_A = 25°C, f_{clock} = 180 kHz, λ_p = 565 nm, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm² (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Low-level output voltage	I_O = 0			0.1	V
High-level output voltage		4.4			V
Analog output voltage, saturation level	E_e = 60 μW/cm²	3	3.4		V
Analog output voltage (white, average over 64 pixels)		1.75	2.2		V
Analog output voltage (dark, each pixel)	E_e = 0		0.25	0.4	V
Output voltage (white) change with change in V_{DD}	V_{DD} = 5 V ±5%, See Note 4		±2%		
Dispersion of analog output voltage	See Note 5			±10%	
Linearity of analog output voltage	t_{int} = 2 ms to 5 ms, See Note 6	0.85		1.15	
Pixel recovery time	See Note 7		25	40	ms
Supply current	I_{DD} (average), See Note 4		4	12	mA
High-level input current	$V_I = V_{DD}$			0.5	μA
Low-level input current	V_I = 0			0.5	μA
Input capacitance			5		pF

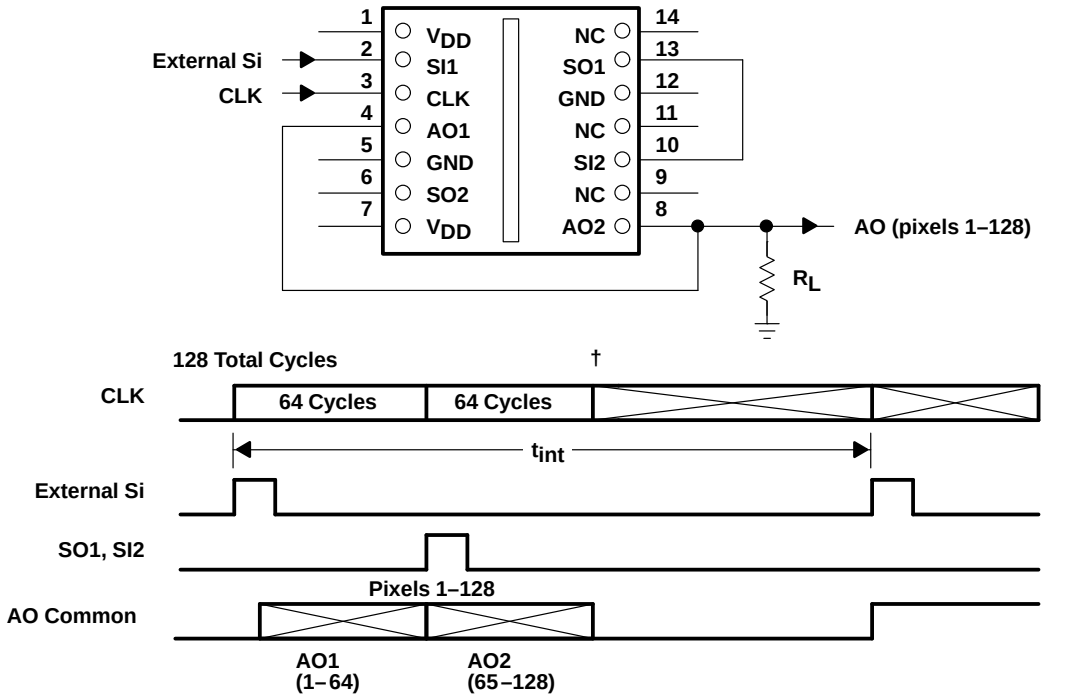
† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 3. The input irradiance (E_e) is supplied by an LED array with λ_p = 565 nm.
4. Device tested in parallel mode with only one section active
5. Dispersion of analog output voltage is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test.
6. Linearity of analog output voltage is calculated by averaging over 64 pixels and measuring the maximum deviation of the voltage at 2 ms and 3.5 ms from a line drawn between the voltage at 2.5 ms and 5 ms.
7. Pixel recovery time is the time required for a pixel to go from the analog-output-voltage (white, average over 64 pixels) level to analog-output-voltage (dark, each pixel) level or vice versa after a step change in light input.

operating characteristics, R_L = 330 Ω, C_L = 330 pF, V_{DD} = 5 V, T_A = 25°C, t_{int} = 5 ms, E_e = 20 μW/cm², f_{clock} = 500 kHz (unless otherwise noted)

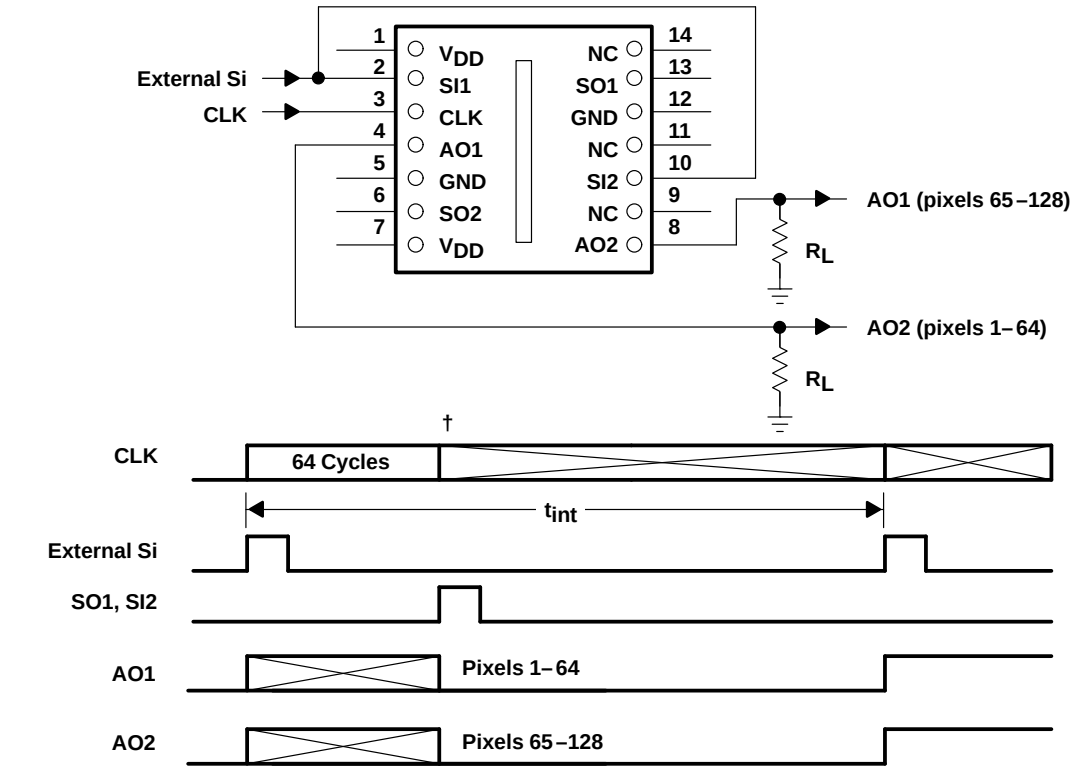
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(SO)}$	Rise time, SO	See Figure 3 and Note 8		25		ns
$t_{f(SO)}$	Fall time, SO			25		ns
$t_{pd(SO)}$	Propagation delay time, SO			70		ns
t_s	Settling time				1	μs
t_v	Valid time				1/2 f_{clock}	μs

NOTE 8: Clock duty cycle is assumed to be 50%.



† CLK continues or goes low after 129 cycles.

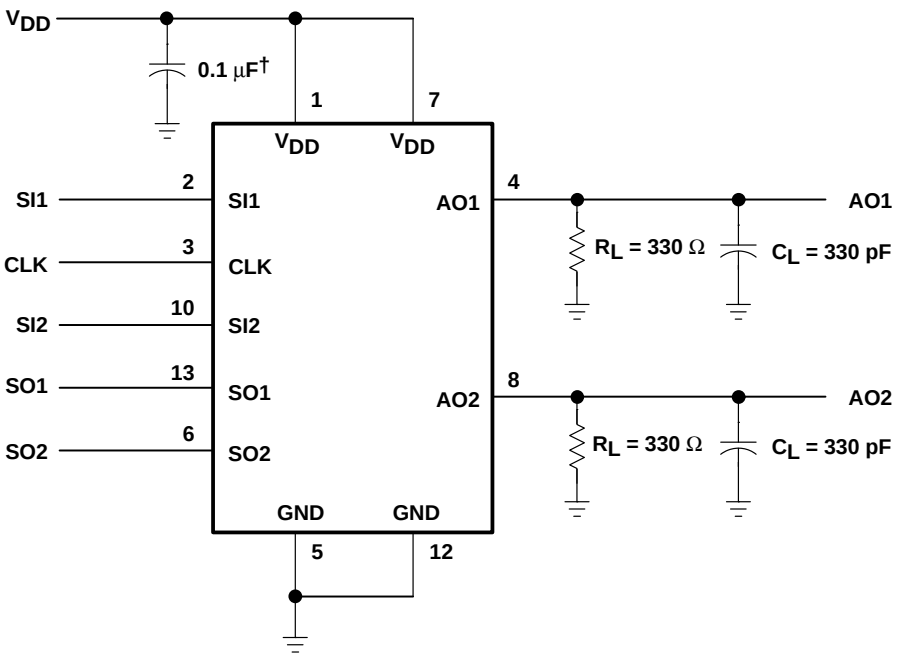
Figure 1. Serial Configuration



† CLK continues or goes low after 65 cycles.

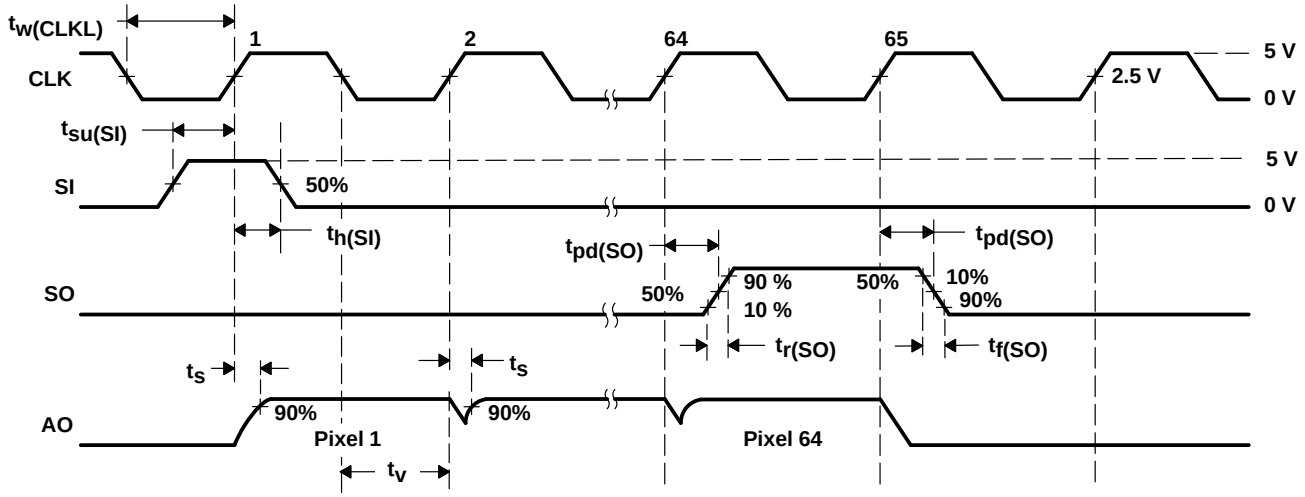
Figure 2. Parallel Configuration

PARAMETER MEASUREMENT INFORMATION



† Supply bypass capacitor with short leads should be placed as close to the device as possible.

TEST CIRCUIT



OPERATIONAL WAVEFORMS

Figure 3. Test Circuit and Operational Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED RESPONSIVITY vs WAVELENGTH OF INCIDENT LIGHT

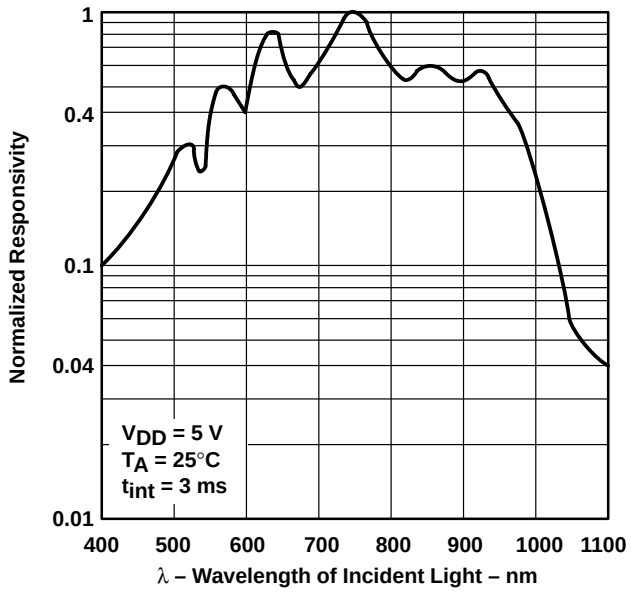


Figure 4

INTEGRATION TIME vs IRRADIANCE FOR CONSTANT AVERAGE ANALOG OUTPUT VOLTAGE

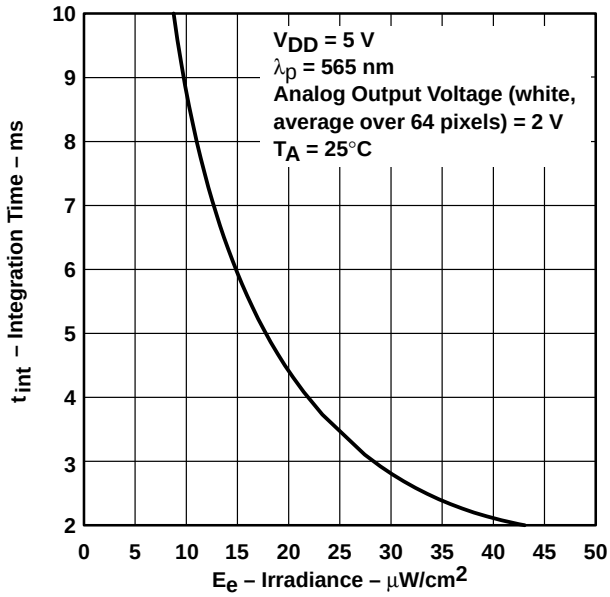


Figure 5

ANALOG OUTPUT VOLTAGE (DARK) vs INTEGRATION TIME

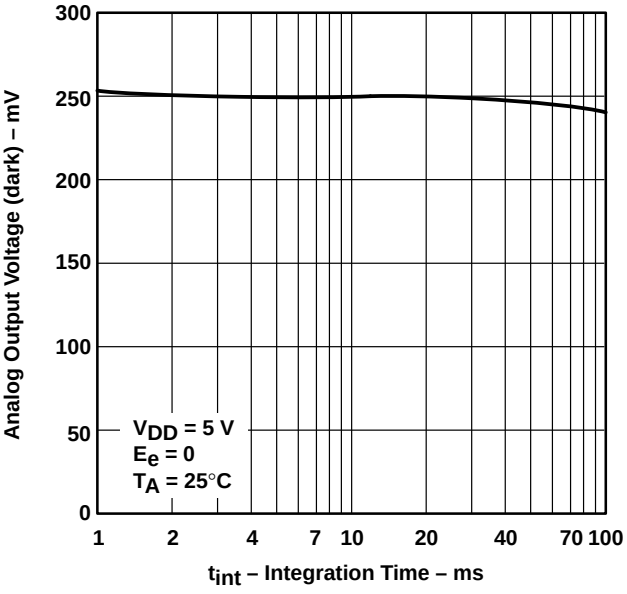


Figure 6

NORMALIZED OUTPUT VOLTAGE vs INTEGRATION TIME

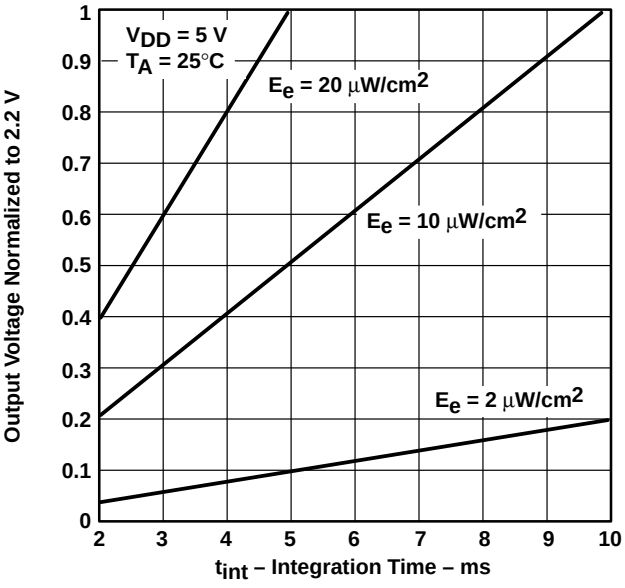
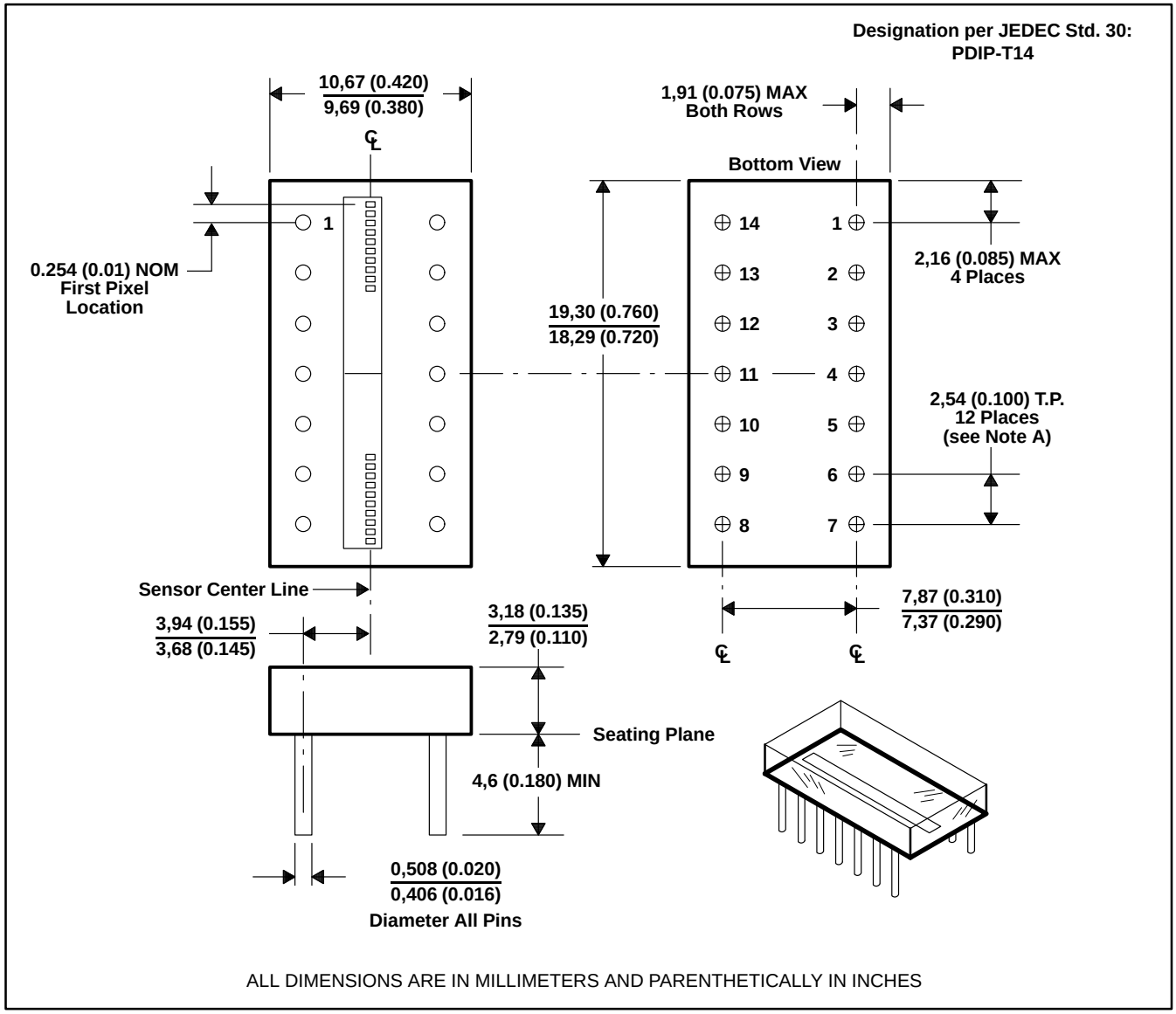


Figure 7

MECHANICAL DATA

This assembly consists of a sensor chip mounted on a printed-circuit board in a clear molded plastic package. The distance between the top surface of the package and the surface of the sensor is nominally 1 mm (0.040 inch).



NOTE A: The true-position spacing is 2,54 mm (0.100 inch) between lead centerlines. Each pin centerline is located within 0,25 mm (0.010 inch) of its true longitudinal positions.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

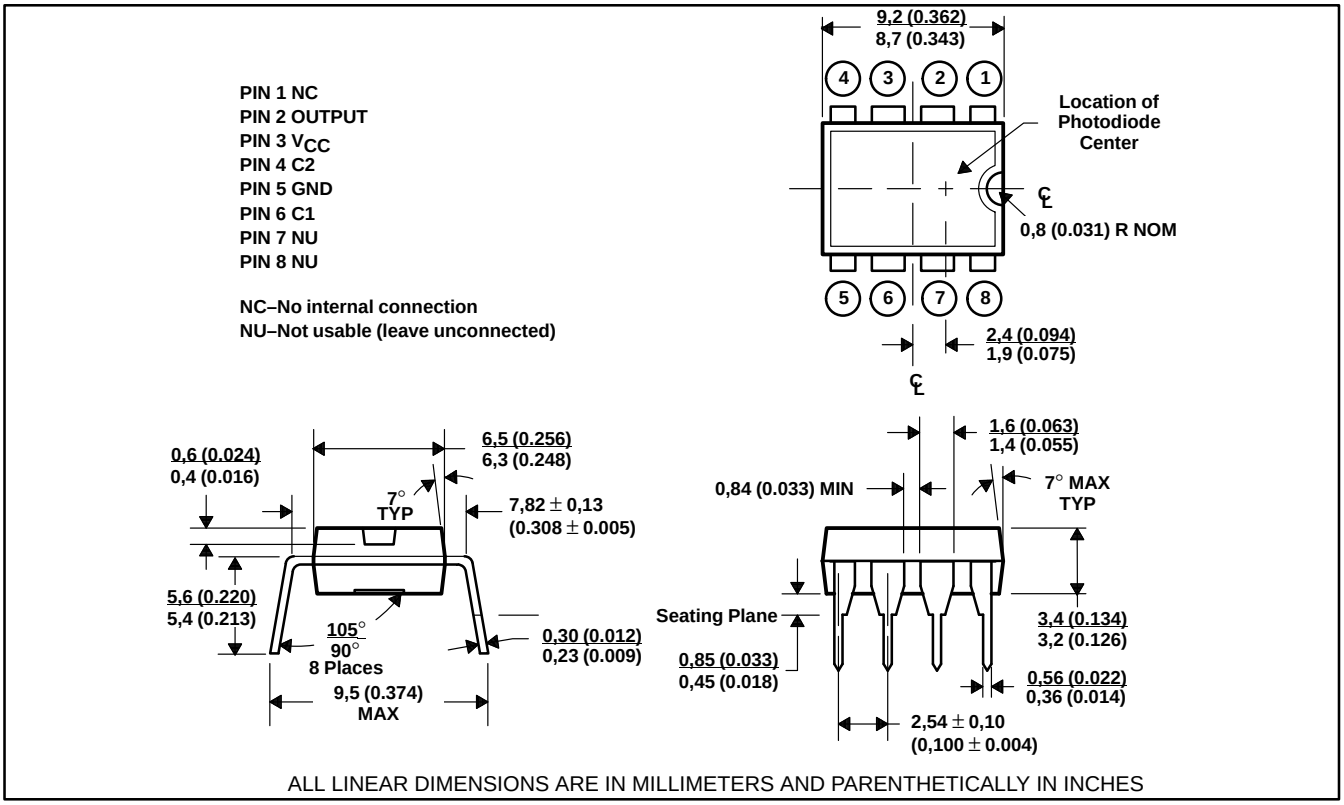
- **High-Resolution Conversion of Light Intensity to Frequency**
- **Wide Dynamic Range . . . 118 dB**
- **Variable (and Single) Supply Range . . . 5 V to 10 V**
- **High Linearity . . . Typically Within 2% of FSR (C = 100 pF)**
- **High Sensitivity . . . Can Detect Change of 0.01% of FSR**
- **CMOS Compatible Output for Digital Processing**
- **Minimum External Components**
- **Microprocessor Compatible**

description

The TSL220 consists of a large-area photodiode and a current-to-frequency converter. The output voltage is a pulse train and its frequency is directly proportional to the light intensity (irradiance) on the photodiode. The output is CMOS† compatible and its frequency may be measured using pulse counting, period timing, or integration techniques. The TSL220 is ideal for light-sensing applications requiring wide dynamic range, high sensitivity, and high noise immunity. The output frequency range is determined by an external capacitor; hence, the desired output frequency is adjustable for a given light intensity at the input. The TSL220 is characterized for operation over the temperature range of –25°C to 70°C.

mechanical data

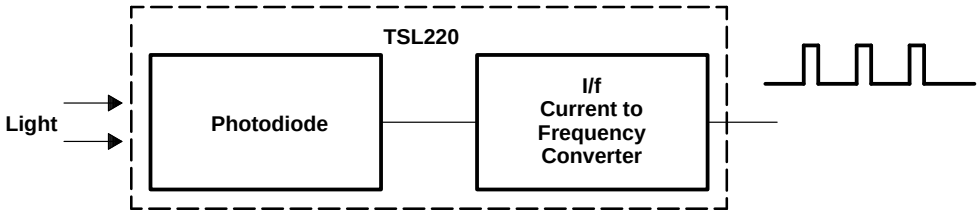
The photodiode and current-to-frequency converter are packaged in a clear plastic 8-pin dual-in-line package. The active chip area is typically 4,13 mm^2 (0.0064 in^2).



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Use of LSTTL logic families may require a 3300-Ω pulldown resistor on the output.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 12 V
Operating free-air temperature, T_A . . . . . –25°C to 70°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to GND (pin 5).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4	5	10	V
Output frequency, f_o ($C \le 100$ pF)			750	kHz
Operating free-air temperature range, T_A	–25		70	°C

electrical characteristics at V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OM}	Peak output voltage	R_L = 50 kΩ	3	4		V
I_{CC}	Supply current	C = 100 pF, E_e = 0		7.5	10	mA

operating characteristics at V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_o	Output frequency	E_e = 125 μW/cm^2, λ = 880 nm, C = 100 pF	50	150	250	kHz
		E_e = 0, C = 100 pF	0	1	50	Hz
t_w	Output pulse duration	C = 470 pF		1		μs
t_r	Output pulse rise time	C = 100 pF		20		ns
t_f	Output pulse fall time	C = 100 pF		120		ns

PARAMETER MEASUREMENT INFORMATION

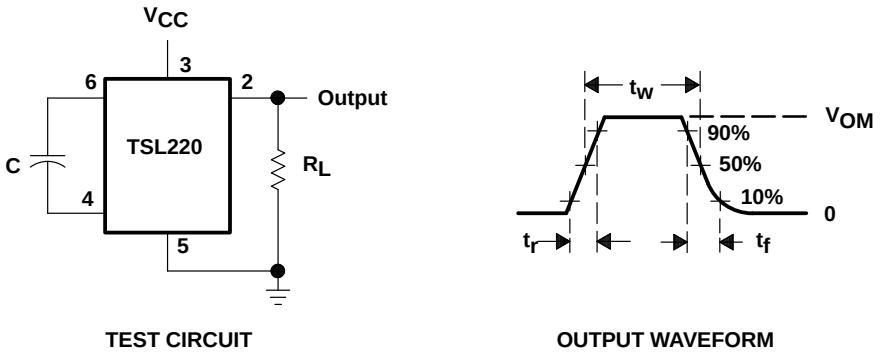


Figure 1. Switching Times

NOTE: Output waveform is monitored on an oscilloscope with the following characteristics: $R_i \geq 1\ M\Omega$, $C_i \leq 6.5\ pF$.

TYPICAL CHARACTERISTICS

OUTPUT PULSE DURATION vs EXTERNAL CAPACITOR VALUE

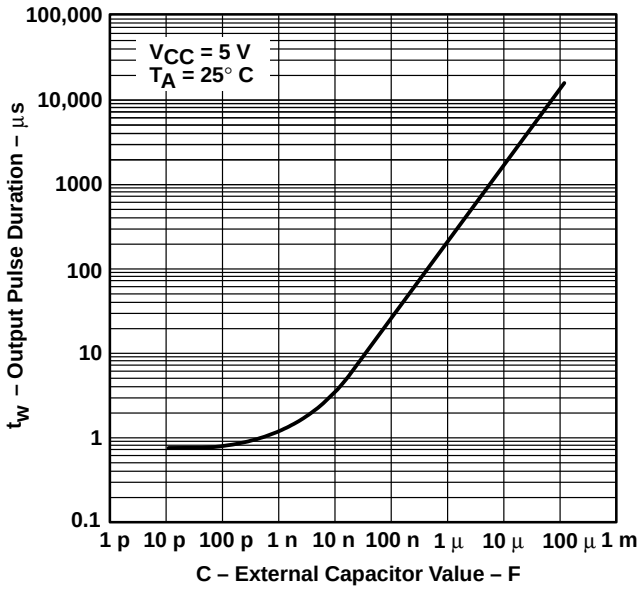


Figure 2

PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

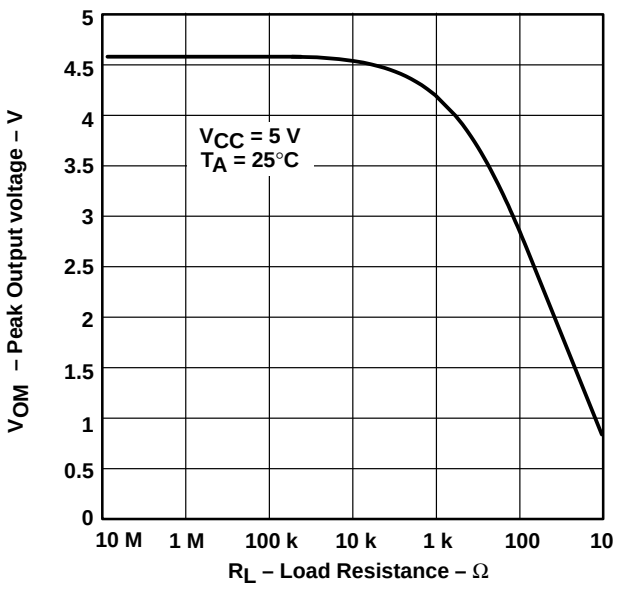


Figure 3

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY vs IRRADIANCE

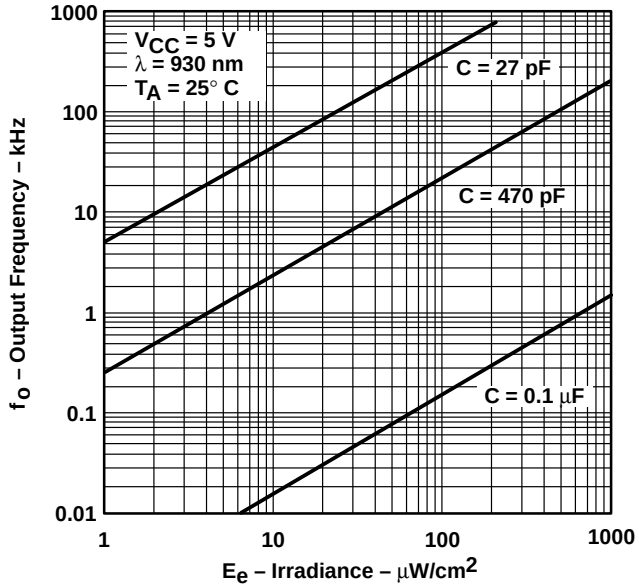


Figure 4

NORMALIZED OUTPUT FREQUENCY vs LOAD RESISTANCE

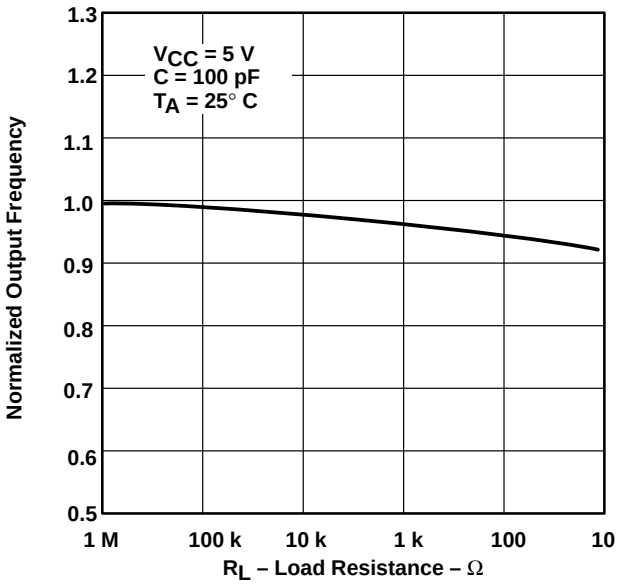


Figure 5

OUTPUT FREQUENCY vs EXTERNAL CAPACITOR VALUE

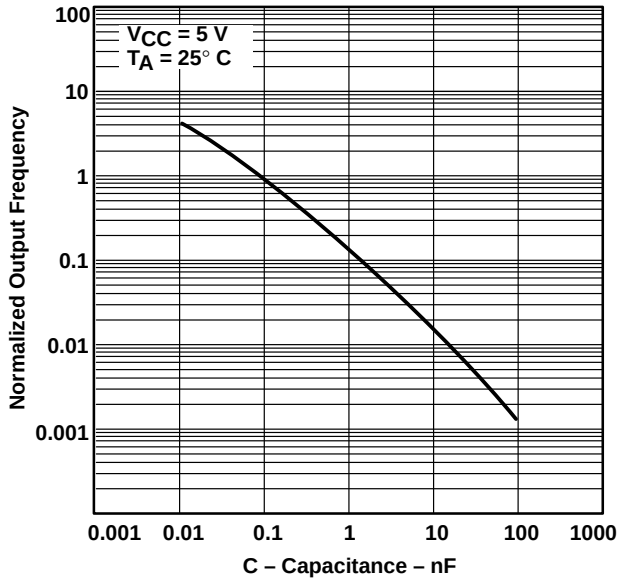


Figure 6

NORMALIZED OUTPUT FREQUENCY vs FREE-AIR TEMPERATURE

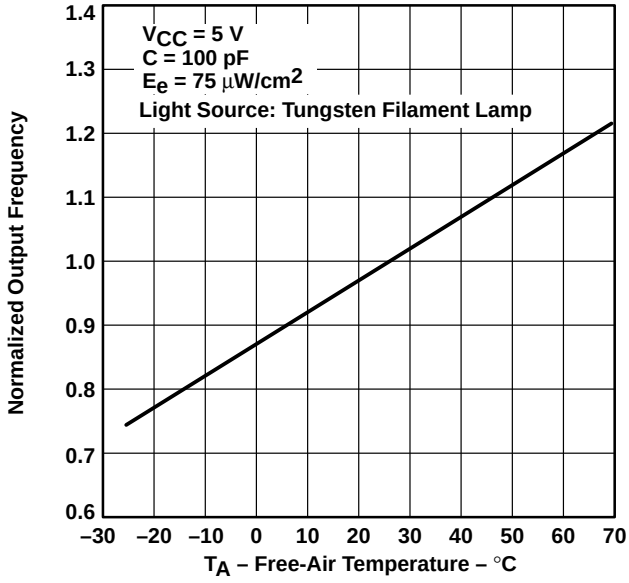


Figure 7

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

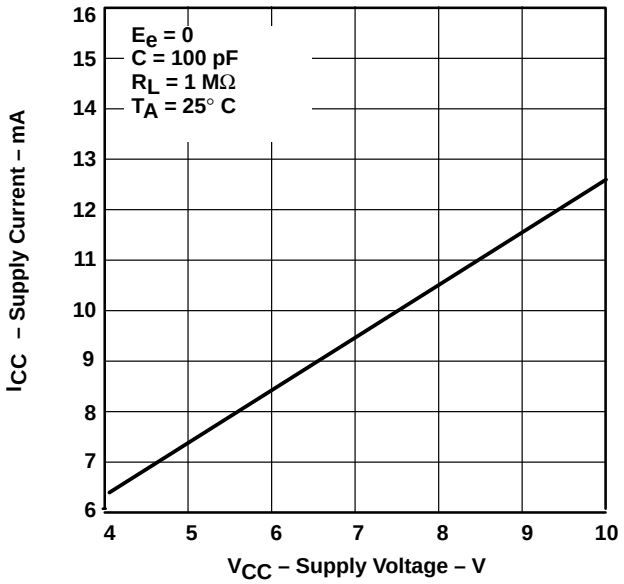


Figure 8

**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

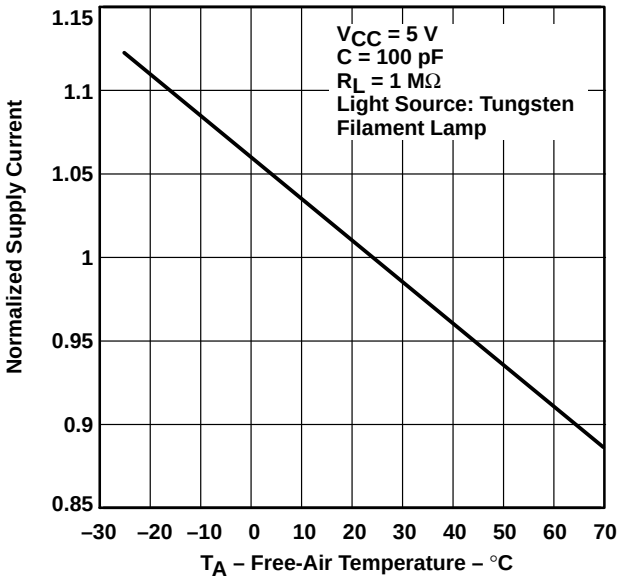


Figure 9

PHOTODIODE SPECTRAL RESPONSE

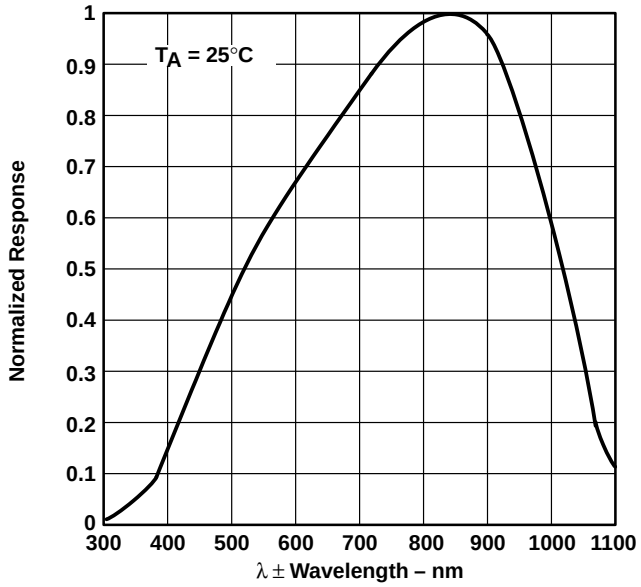


Figure 10

APPLICATION INFORMATION

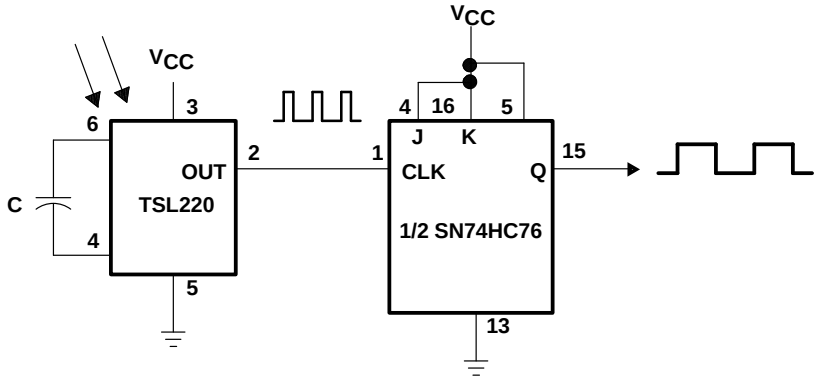
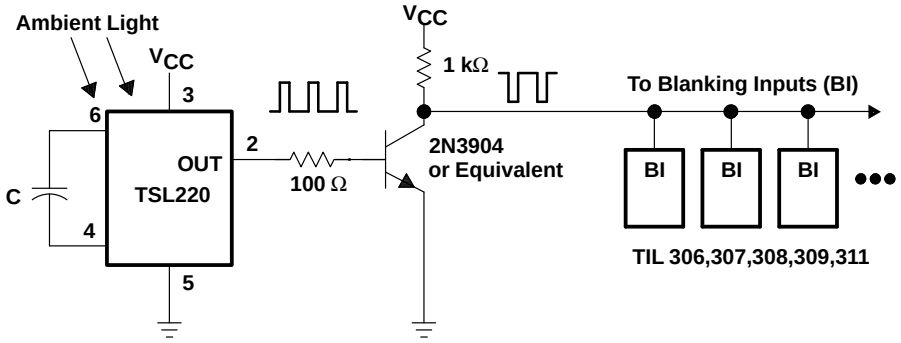


Figure 11. Light-to-Frequency Converter with Square-Wave Output



NOTE: Adjust C to set maximum and minimum brightness levels.

Figure 12. Automatic Display Dimming Circuit

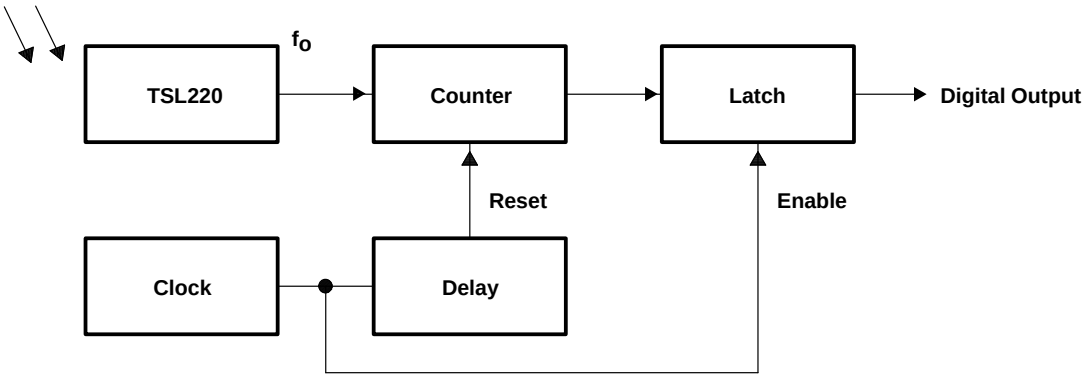


Figure 13. Light-to-Digital Converter

APPLICATION INFORMATION

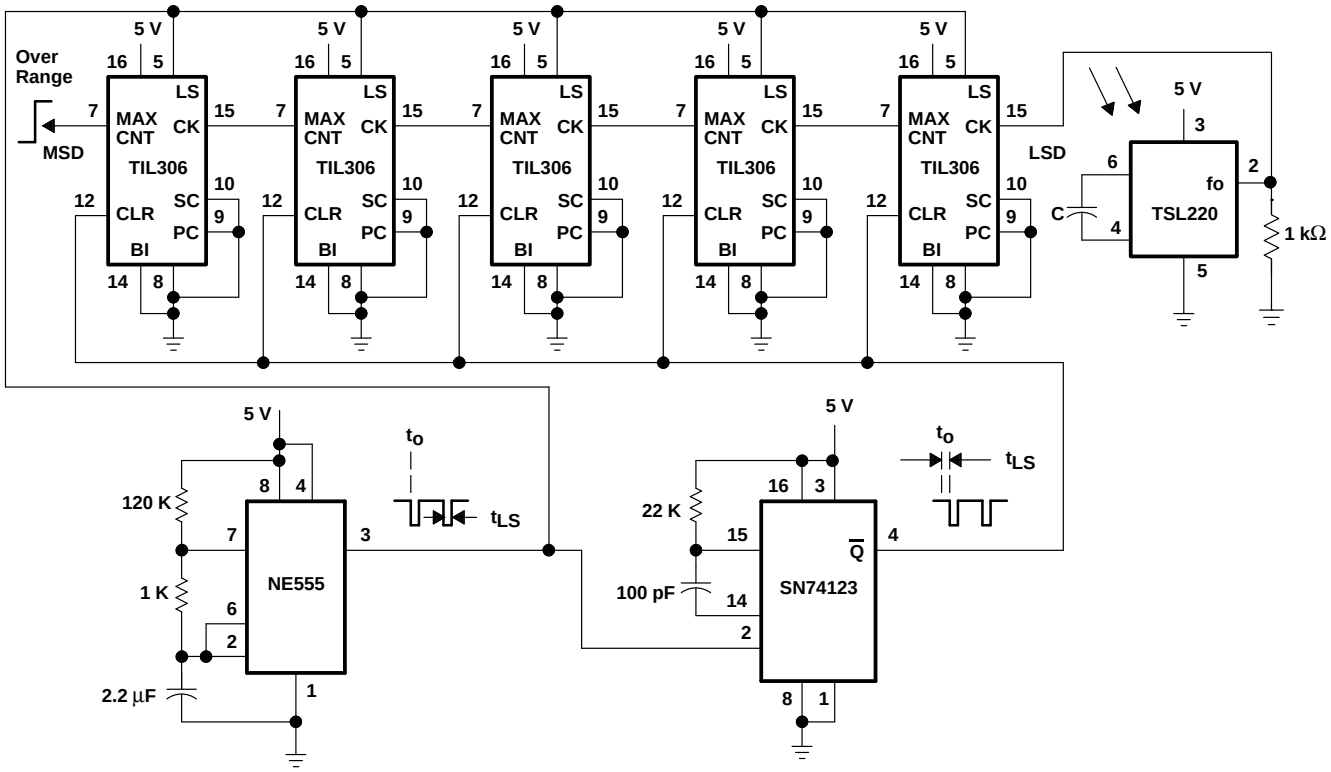


Figure 14. Simple Digital Light Meter

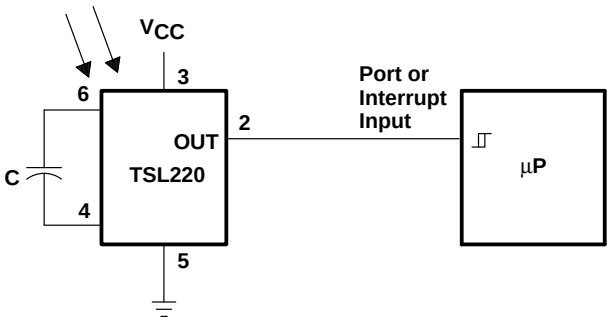
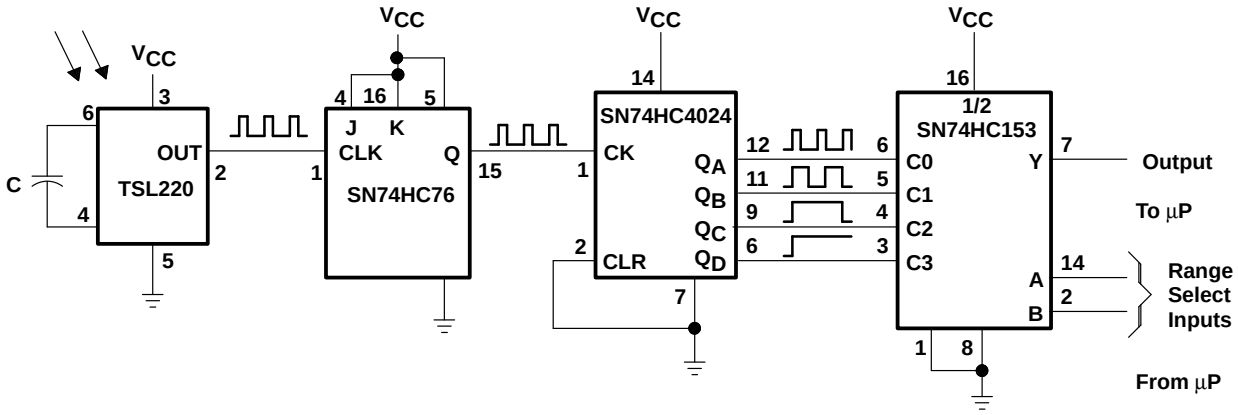


Figure 15. Light Detector with Direct Microprocessor Interface

APPLICATION INFORMATION



NOTE: Adjust C for useful frequency range.

Figure 16. Light Detector with Microprocessor (Microcontroller) and Autoranging Capability

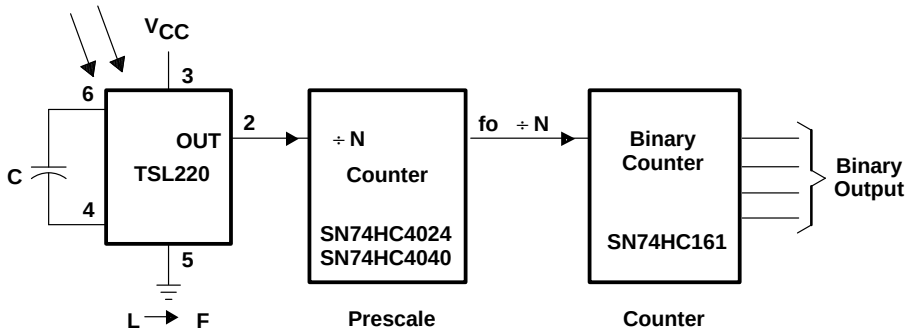
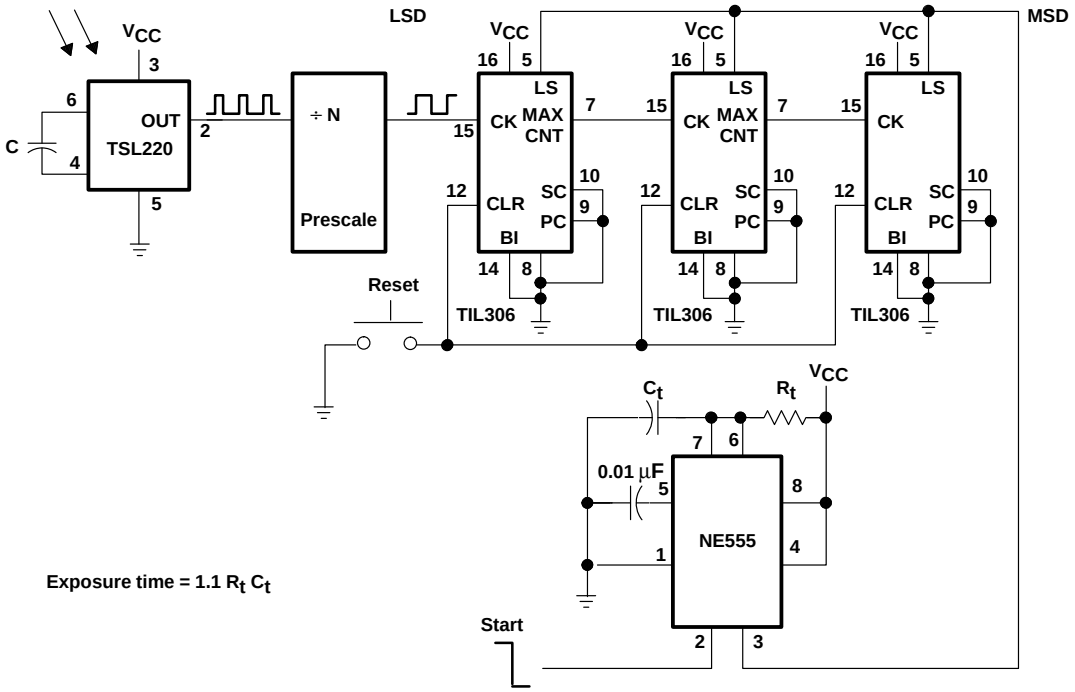


Figure 17. Digital Light Integrator

APPLICATION INFORMATION



Exposure time = 1.1 R_t C_t

Figure 18. Digital Light Exposure Meter

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

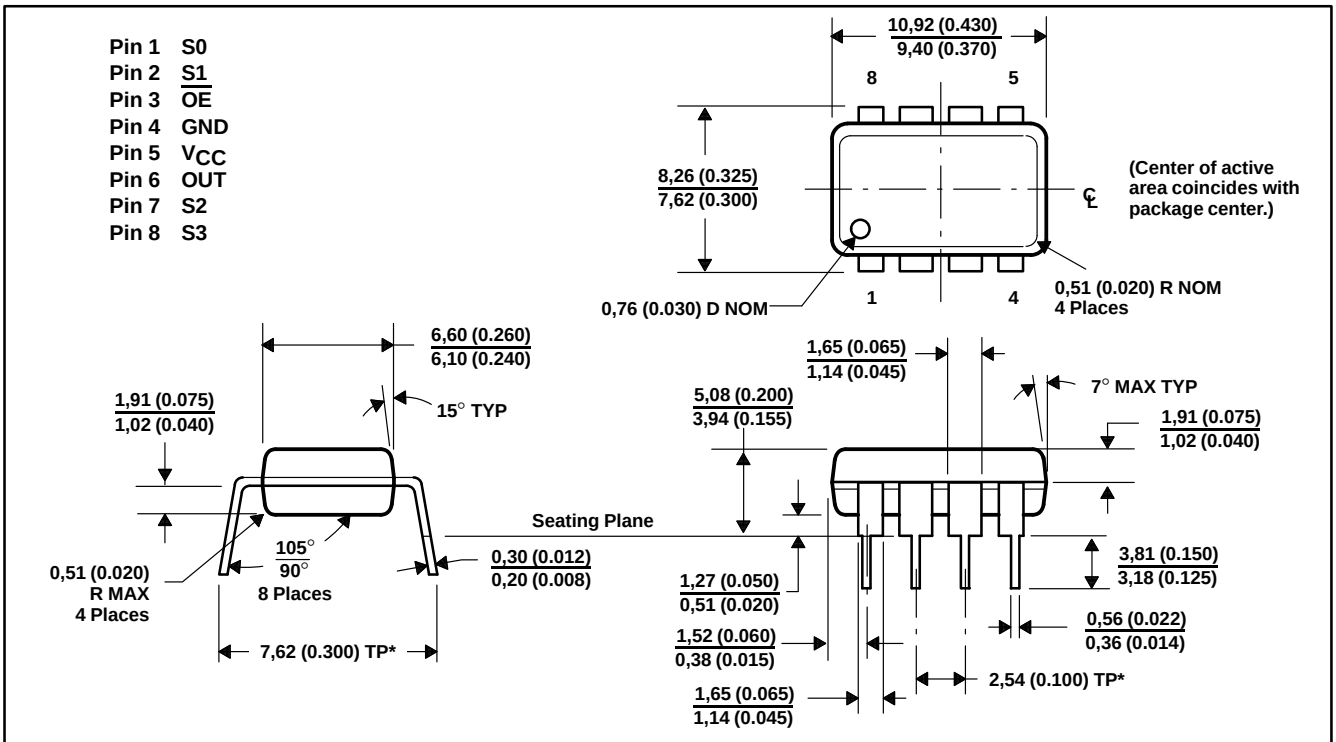
- **High-Resolution Conversion of Light Intensity to Frequency With No External Components**
- **Programmable Sensitivity and Full-Scale Output Frequency**
- **Communicates Directly With a Microcontroller**
- **Single-Supply Operation Down to 2.7 V, With Power-Down Feature**
- **Absolute Output Frequency Tolerance of ±5% (TSL230B)**
- **Nonlinearity Error Typically 0.2% at 100 kHz**
- **Stable 100 ppm/°C Temperature Coefficient**
- **Advanced LinCMOS™ Technology**

description

The TSL230, TSL230A, and TSL230B programmable light-to-frequency converters combine a configurable silicon photodiode and a current-to-frequency converter on single monolithic CMOS integrated circuits. The output can be either a pulse train or a square wave (50% duty cycle) with frequency directly proportional to light intensity. The sensitivity of the devices is selectable in three ranges, providing two decades of adjustment. The full-scale output frequency can be scaled by one of four preset values. All inputs and the output are TTL compatible, allowing direct two-way communication with a microcontroller for programming and output interface. An output enable ($\overline{OE}$) is provided that places the output in the high-impedance state for multiple-unit sharing of a microcontroller input line. The devices are available with absolute-output-frequency tolerances of ±5% (TSL230B), ±10% (TSL230A), or ±20% (TSL230). Each circuit has been temperature compensated for the ultraviolet-to-visible-light range of 300 nm to 700 nm. The devices are characterized for operation over the temperature range of –25°C to 70°C.

mechanical data

The TSL230, TSL230A, and TSL230B are packaged in a clear plastic 8-pin dual-in-line package. The photodiode area is typically 1.36 mm^2 (0.0029 in^2) (S0 = S1 = H).



*True position when unit is installed.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

LinCMOS is a trademark of Texas Instruments Incorporated.

Terminal Functions

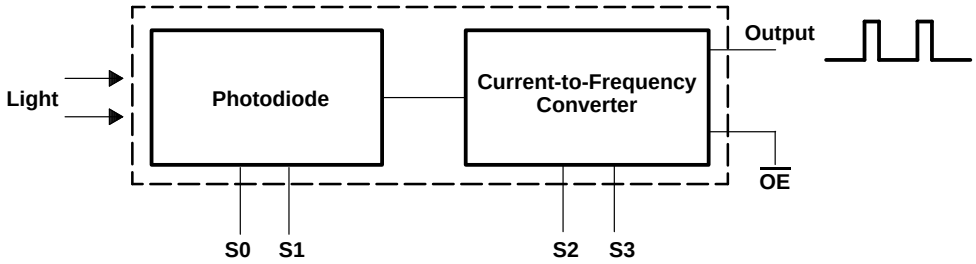
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{OE}$	3	I	Enable for f_O (active low)
OUT	6	O	Scaled-frequency (f_O) output
S0, S1	1, 2	I	Sensitivity-select inputs
S2, S3	7, 8	I	f_O scaling-select inputs
V_{DD}	5		Supply voltage

Selectable Options

S1	S0	SENSITIVITY
L	L	Power Down
L	H	1×
H	L	10×
H	H	100×

S3	S2	f_O SCALING (divide-by)
L	L	1
L	H	2
H	L	10
H	H	100

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 6.5 V
Input voltage range, all inputs, V_I . . . . . –0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . –25°C to 70°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	5	6	V
High-level input voltage, V_{IH}	V_{DD} = 4.5 V to 5.5 V	2		V_{DD}	V
Low-level input voltage, V_{IL}	V_{DD} = 4.5 V to 5.5 V	0		0.8	V
Operating free-air temperature range, T_A		–25		70	°C

electrical characteristics at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	4	4.3		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.17	0.26	V
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				1	µA
I_{DD}	Supply current	Power-on mode		2	3	mA
		Power-down mode			10	µA
	Full-scale frequency†		1.1			MHz
	Temperature coefficient of output frequency	λ ≤ 700 nm, –25°C ≤ T_A ≤ 70°C		±100		ppm/°C
k_{SVS}	Supply voltage sensitivity	V_{DD} = 5 V ±10%		0.5		%/V

† Full-scale frequency is the maximum operating frequency of the device without saturation.

operating characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TSL230			TSL230A			TSL230B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_O	Output frequency	S0 = H, S1 = S2 = S3 = L, E_e = 130 mW/cm², λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0, S0 = H, S1 = S2 = S3 = L		0.1	10		0.1	10		0.1	10	Hz
		S1 = H, S0 = S2 = S3 = L, E_e = 13 mW/cm², λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0 S1 = H, S0 = S2 = S3 = L		0.13	10		0.13	10		0.13	10	Hz
		S0 = S1 = H, S2 = S3 = L, E_e = 1.3 mW/cm², λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0, S0 = S1 = H, S2 = S3 = L		0.5	10		0.5	10		0.5	10	Hz
t_w	Output pulse duration	S2 = S3 = L	125		550	125		550	125		550	ns
		S2 or S3 = H		1/2f_O			1/2f_O			1/2f_O		s
	Nonlinearity‡	f_O = 0 MHz to 10 kHz		±0.1%			±0.1%			±0.1%		%F.S.
		f_O = 0 MHz to 100 kHz		±0.2%			±0.2%			±0.2%		%F.S.
		f_O = 0 MHz to 1 MHz		±0.5%			±0.5%			±0.5%		%F.S.
	Recovery from power down				100			100			100	µs
	Step response to full-scale step input		1 pulse of new frequency plus 1 µs									
	Response time to programming change		2 periods of new principal frequency plus 1 µs§									
	Response time to output enable ($\overline{OE}$)			50	150		50	150		50	150	ns

† Full-scale frequency is the maximum operating frequency of the device without saturation.
‡ Nonlinearity is defined as the deviation of f_O from a straight line between zero and full scale, expressed as a percent of full scale.
§ Principal frequency is the internal oscillator frequency, equivalent to divide-by-1 output selection.

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY vs IRRADIANCE

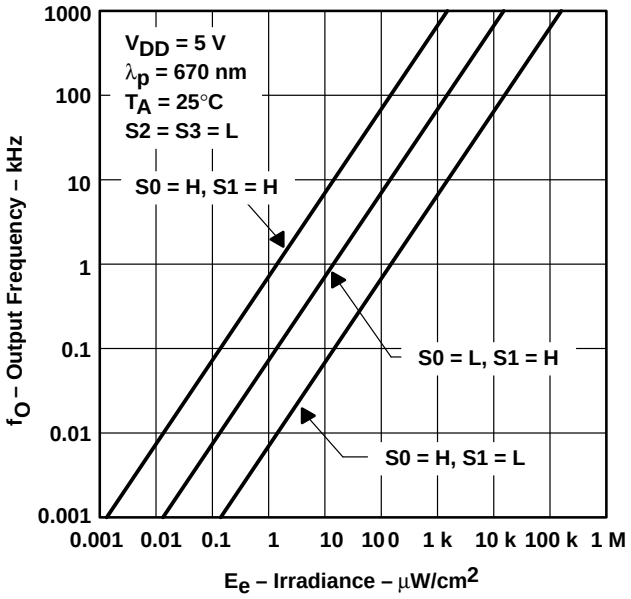


Figure 1

PHOTODIODE SPECTRAL RESPONSIVITY

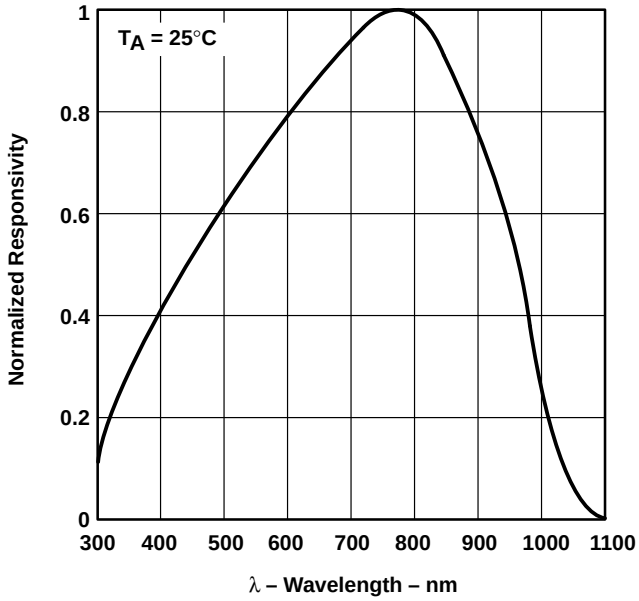


Figure 2

DARK FREQUENCY vs TEMPERATURE

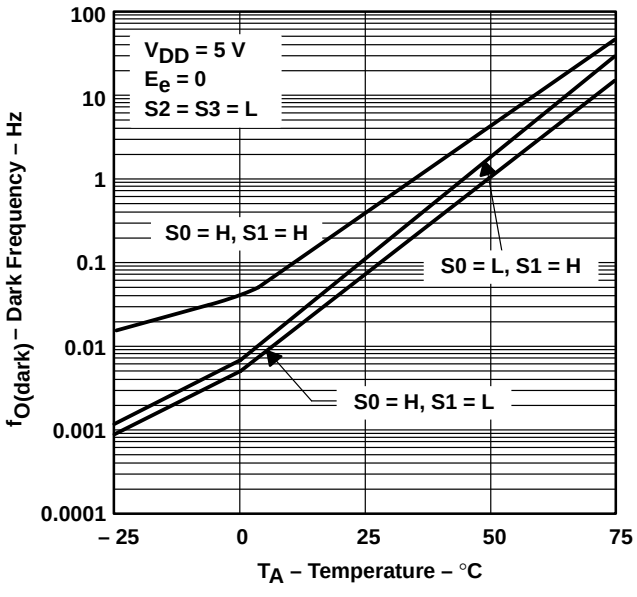


Figure 3

TEMPERATURE COEFFICIENT OF OUTPUT FREQUENCY vs WAVELENGTH OF INCIDENT LIGHT

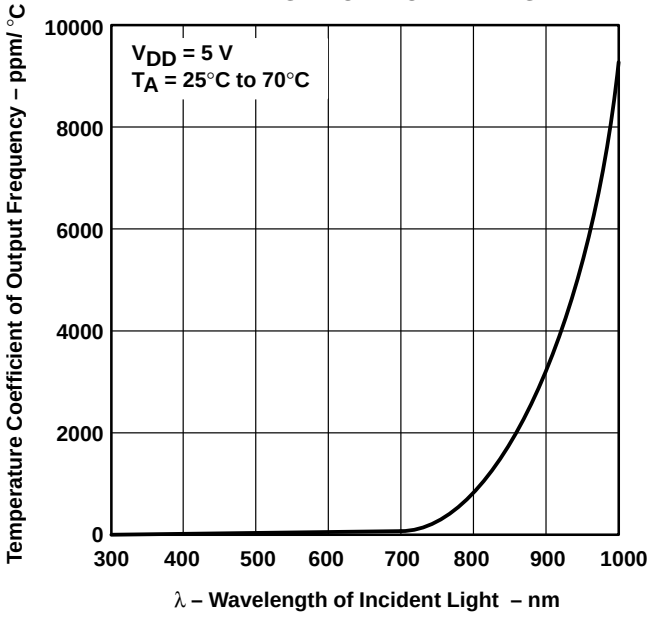


Figure 4

TYPICAL CHARACTERISTICS

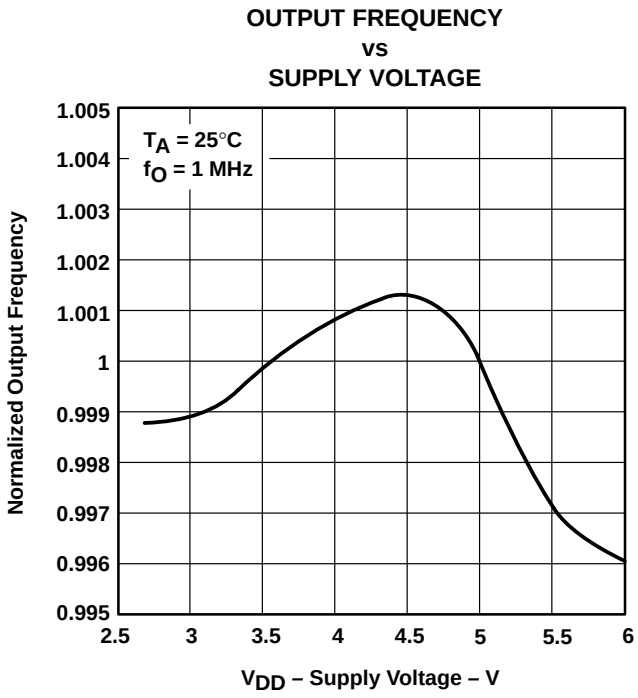


Figure 5

APPLICATION INFORMATION

power-supply considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01-μF to 0.1-μF capacitor with short leads.

output interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

sensitivity adjustment

Sensitivity is controlled by two logic inputs, S0 and S1. Sensitivity is adjusted using an electronic iris technique – effectively an aperture control – to change the response of the device to a given amount of light. The sensitivity can be set to one of three levels: 1x, 10x or 100x, providing two decades of adjustment. This allows the responsivity of the device to be optimized to a given light level while preserving the full-scale output-frequency range. Changing of sensitivity also changes the effective photodiode area by the same factor.

APPLICATION INFORMATION

output-frequency scaling

Output-frequency scaling is controlled by two logic inputs, S2 and S3. Scaling is accomplished on chip by internally connecting the pulse-train output of the converter to a series of frequency dividers. Divided outputs available are divide-by 2, 10, 100, and 1 (no division). Divided outputs are 50 percent-duty-cycle square waves while the direct output (divide-by 1) is a fixed-pulse-width pulse train. Because division of the output frequency is accomplished by counting pulses of the principal (divide-by 1) frequency, the final-output period represents an average of n (where n is 2, 10 or 100) periods of the principal frequency. The output-scaling-counter registers are cleared upon the next pulse of the principal frequency after any transition of the S0, S1, S2, S3, or OE lines. The output goes high upon the next subsequent pulse of the principal frequency, beginning a new valid period. This minimizes the time delay between a change on the input lines and the resulting new output period in the divided output modes. In contrast with the sensitivity adjust, use of the divided outputs lowers both the full-scale frequency and the dark frequency by the selected scale factor.

The frequency-scaling function allows the output range to be optimized for a variety of measurement techniques. The divide-by-1 or straight-through output can be used with a frequency counter, pulse accumulator, or high-speed timer (period measurement). The divided-down outputs may be used where only a slower frequency counter is available, such as a low-cost microcontroller, or where period measurement techniques are used. The divide-by-10 and divide-by-100 outputs provide lower frequency ranges for high resolution-period measurement.

measuring the frequency

The choice of interface and measurement technique depends on the desired resolution and data acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

Using the divide-by-2 output, data can be collected at a rate of twice the output frequency or one data point every microsecond for full-scale output. Period measurement requires the use of a fast reference clock with available resolution directly related to reference-clock rate. Output scaling can be used to increase the resolution for a given clock rate or to maximize resolution as the light input changes. Period measurement is used to measure rapidly varying light levels or to make a very fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random- or high-frequency variations (jitter) resulting from noise in the light signal. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration (the accumulation of pulses over a very long period of time) can be used to measure exposure, the amount of light present in an area over a given time period.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

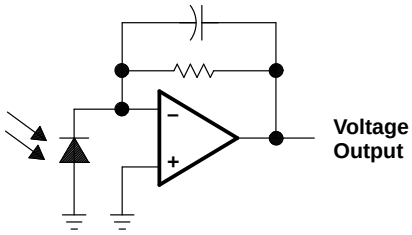
TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

- **Monolithic Silicon IC Containing Photodiode, Operational Amplifier, and Feedback Components**
- **Converts Light Intensity to Output Voltage**
- **High Irradiance Responsivity Typically 80 mV/(μW/cm^2) at λ_p = 880 nm (TSL250)**
- **Compact 3-Leaded Clear Plastic Package**
- **Low Dark (Offset) Voltage . . . 10 mV Max at 25°C, V_{DD} = 5 V**
- **Single-Supply Operation**
- **Wide Supply-Voltage Range . . . 3 V to 9 V**
- **Low Supply Current . . . 800 μA Typical at V_{DD} = 5 V**
- **Advanced LinCMOS™ Technology**

description

The TSL250, TSL251, and TSL252 are light-to-voltage optical sensors, each combining a photodiode and a transimpedance amplifier (feedback resistor = 16 MΩ, 8 MΩ, and 2 MΩ respectively) on a single monolithic IC. The output voltage is directly proportional to the light intensity (irradiance) on the photodiode. These devices utilize Texas Instruments silicon-gate LinCMOS™ technology, which provides improved amplifier offset-voltage stability and low power consumption.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 10 V
Output current, I_O . . . . . ±10 mA
Duration of short-circuit current at (or below) 25°C (see Note 2) . . . . . 5 s
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 240°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.
2. Output may be shorted to supply.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	9	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C, λp = 880 nm, R_L = 10 kΩ (unless otherwise noted) (see Note 3)

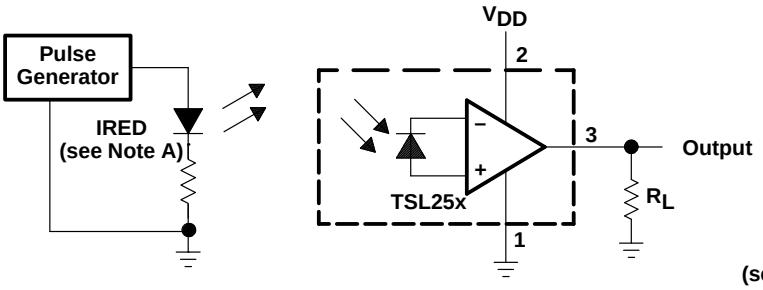
PARAMETER		TEST CONDITIONS	TSL250			TSL251			TSL252			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_D	Dark voltage	E_e = 0		3	10		3	10		3	10	mV
V_{OM}	Maximum output voltage swing	E_e = 2 mW/cm^2	3.1	3.5		3.1	3.5		3.1	3.5		V
V_O	Output voltage	E_e = 25 μW/cm^2	1	2	3							V
		E_e = 45 μW/cm^2				1	2	3				
		E_e = 285 μW/cm^2							1	2	3	
α_{vo}	Temperature coefficient of output voltage (V_O)	E_e = 25 μW/cm^2, T_A = 0°C to 70°C		±1								mV/°C
		E_e = 45 μW/cm^2, T_A = 0°C to 70°C					±1					
		E_e = 285 μW/cm^2, T_A = 0°C to 70°C								±1		
N_e	Irradiance responsivity	See Note 4		80			45			7		mV/(μW/cm^2)
I_{DD}	Supply current	E_e = 25 μW/cm^2		900	1600							μA
		E_e = 45 μW/cm^2					900	1600				
		E_e = 285 μW/cm^2								900	1600	

NOTES: 3. The input irradiance E_e is supplied by a GaAlAs infrared-emitting diode with λ_p = 880 nm.
4. Irradiance responsivity is characterized over the range V_O = 0.05 to 3 V.

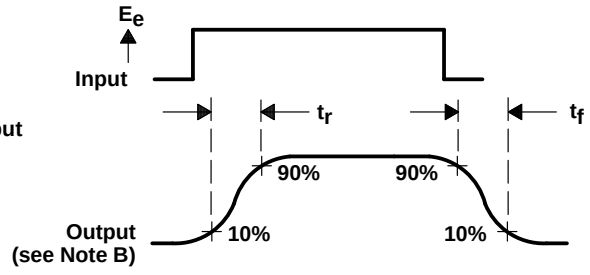
operating characteristics at T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	TSL250			TSL251			TSL252			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Output pulse rise time	V_{DD} = 5 V, λ_p = 880 nm		360			90			7		μs
t_f	Output pulse fall time	V_{DD} = 5 V, λ_p = 880 nm		360			90			7		μs
V_n	Output noise voltage	V_{DD} = 5 V, f = 20 Hz		0.6			0.5			0.4		μV/√Hz

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. The input irradiance is supplied by a pulsed GaAlAs infrared-emitting diode with the following characteristics: λ_p = 880 nm, t_r < 1 μs, t_f < 1 μs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r < 100 ns, Z_i ≥ 1 MHz, C_i ≤ 20 pF.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs IRRADIANCE

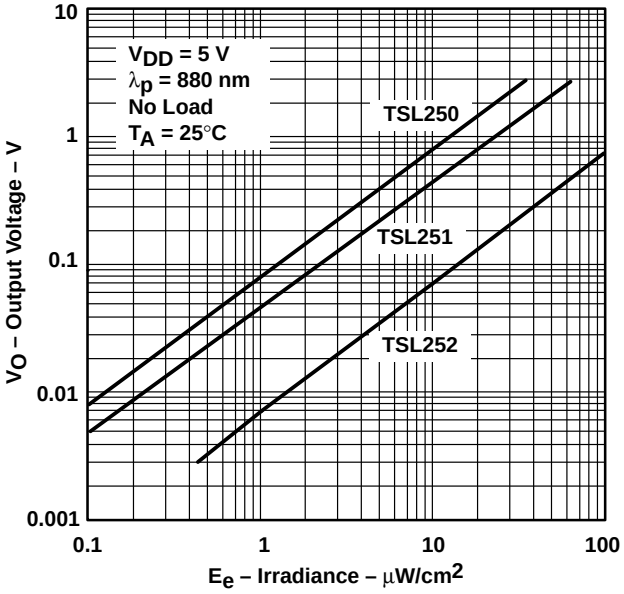


Figure 2

PHOTODIODE SPECTRAL RESPONSIVITY

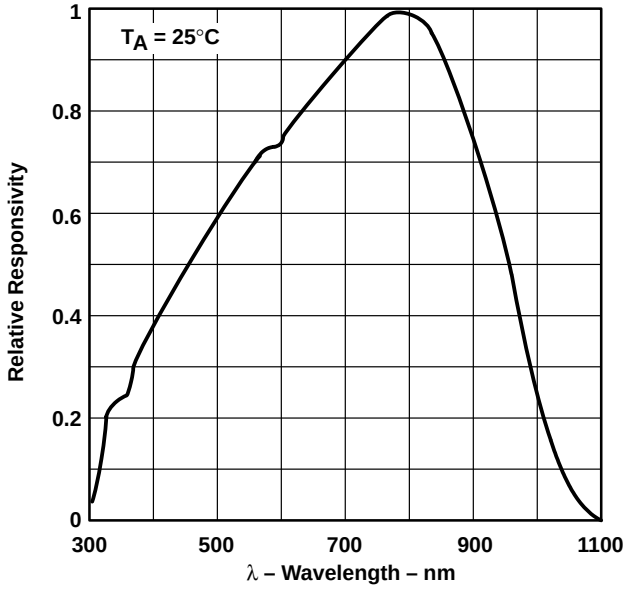


Figure 3

MAXIMUM OUTPUT VOLTAGE vs SUPPLY VOLTAGE

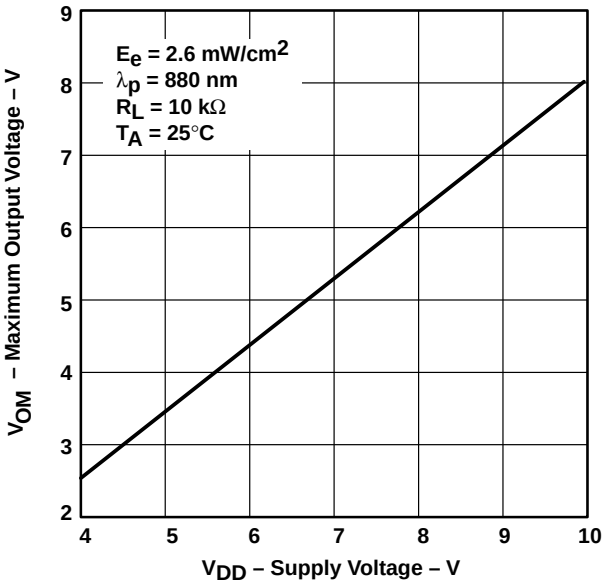


Figure 4

SUPPLY CURRENT vs OUTPUT VOLTAGE

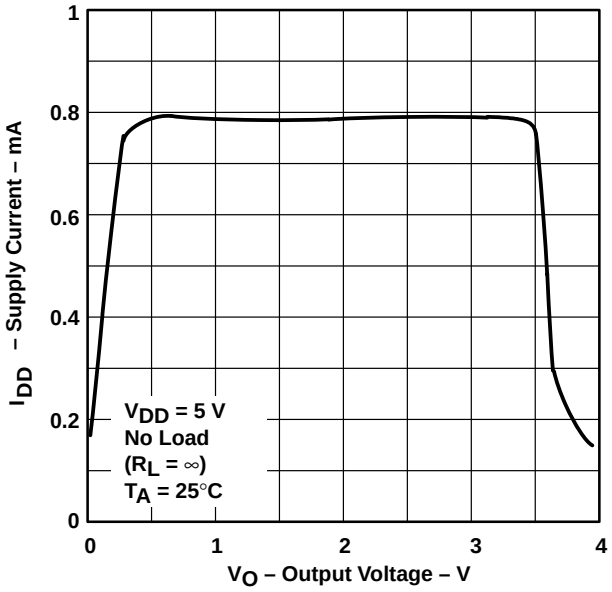


Figure 5

TYPICAL CHARACTERISTICS

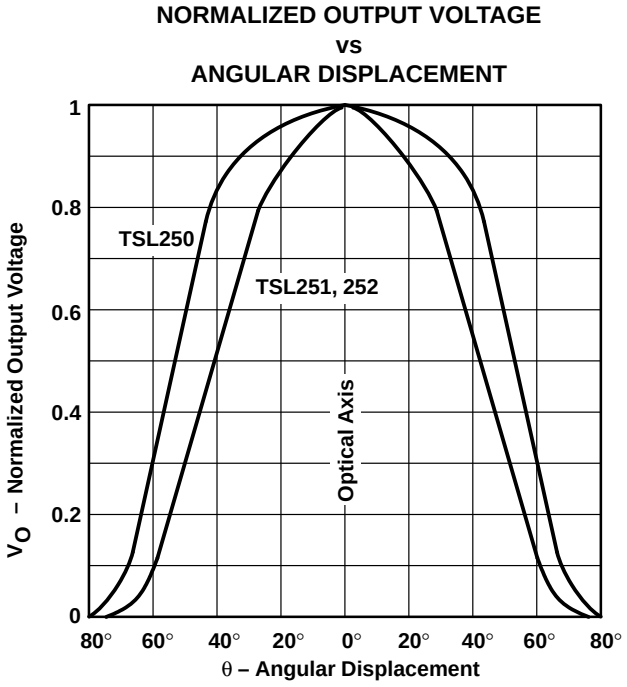
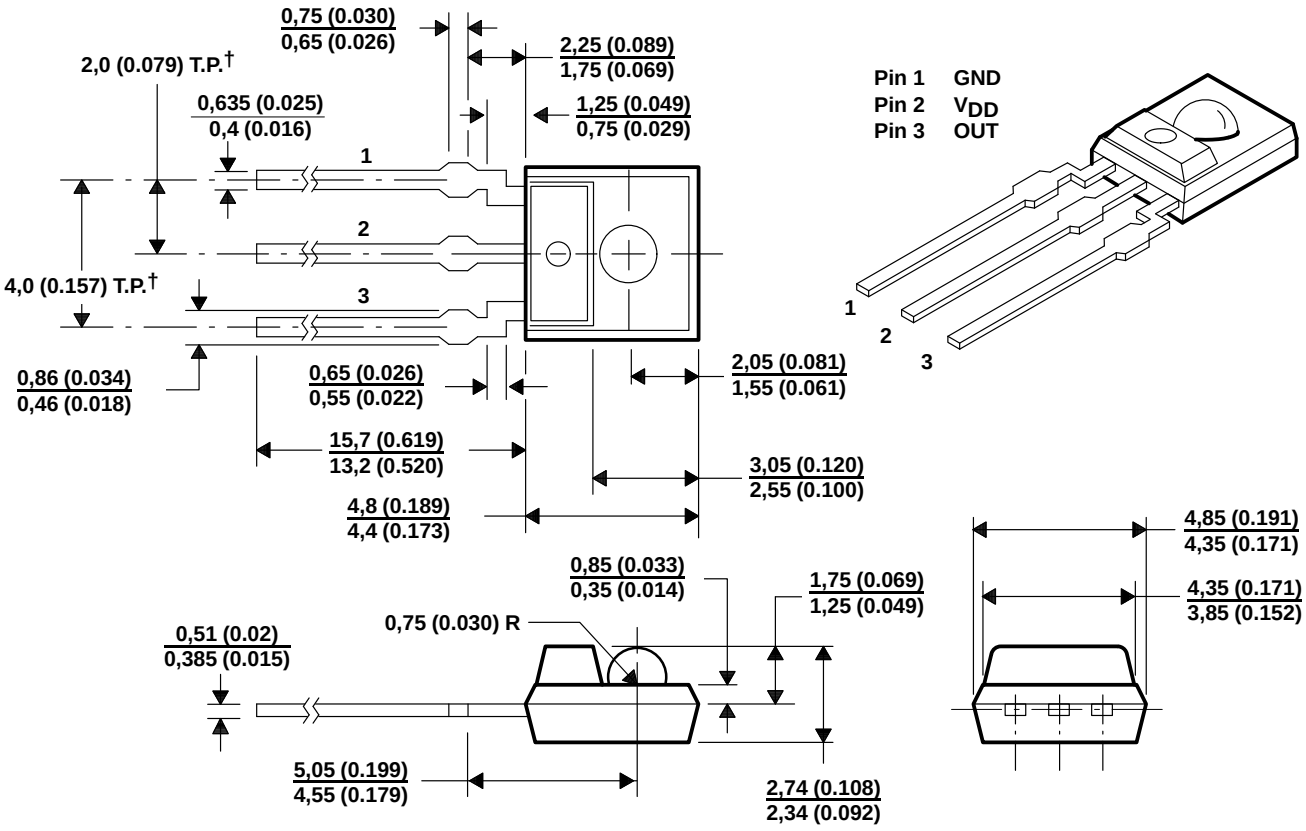


Figure 6

APPLICATION INFORMATION

The photodiode/amplifier chip is packaged in a clear plastic three-leaded package. The integrated photodiode active area is typically 1,0 mm^2 (0.0016 in^2) for TSL250, 0,5 mm^2 (0.00078 in^2) for the TSL251, and 0,26 mm^2 (0.0004 in^2) for the TSL252.



† True position when unit is installed.

NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.

Figure 7. Mechanical Data

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.