

GENERAL PURPOSE LED LIGHTING PWM CONTROLLER

Check for Samples: [TPS92001](#), [TPS92002](#)

FEATURES

- **Ideal for Single Stage Designs**
- **Supports Isolated and Non-Isolated Topologies**
- **Phase-Cut TRIAC Dimmable**
- **Few External Components Mode Operation**
- **Wide Duty Cycle Range for Wide-Input Voltage or Dimming Range**
- **Convenient 5-V Reference Output**
- **Undervoltage Lockout for Safe Operation**
- **Operation to 1-MHz**
- **0.4-A Source/0.8-A Sink FET Driver**
- **Low 100- μ A Startup Current**

APPLICATIONS

- **Residential LED Lighting Drivers for A19 E12/E26/27, GU10, MR16, PAR30/38 Integral Lamps**
- **Drivers for Wall Sconces, Pathway Lighting and Overhead Lighting**
- **Drivers for Wall Washing, Architectural and Display Lighting**

| DEVICE NUMBER | TURN-ON THRESHOLD (V) | TURN-OFF THRESHOLD (V) |
|------------------|--------------------------|---------------------------|
| TPS92001 | 10 | 8 |
| TPS92002 | 15 | |

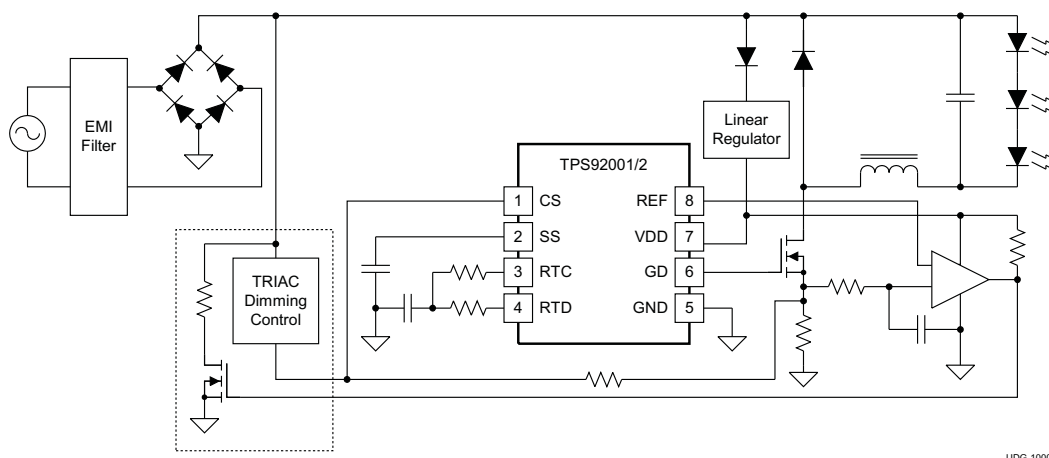
DESCRIPTION

The TPS92001/2 family of general LED lighting PWM controllers contains control and drive circuitry required for off-line isolated or non-isolated LED lighting applications.

The controllers can support Phase Cut TRIAC dimming with minimal external components. The controllers can also be implemented for stage conversion where the power factor (PF) exceeds regulatory requirements for lighting. These controllers also have an accessible 5-V reference that could be used to power a microcontroller or other low power peripheral components. The controllers operate in fixed frequency current mode switching with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100 μ A, logic to ensure latched operation, a PWM comparator, and a totem pole output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state. Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor.

The TPS92001/2 family also features full cycle soft start. The family offers UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems. The TPS92001/2 is offered in the 8-pin MSOP (DGK) and 8-pin SOIC (D) packages. The small MSOP package makes the device ideally suited for applications where board space and height are at a premium.

SIMPLIFIED APPLICATION



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | | RANGE | UNIT |
|--------------------------------|---|-------------------|------|
| Input voltage range | VDD | 19 | V |
| | SS | -0.3 to REF + 0.3 | |
| | RTC, RTD | -0.3 to REF + 0.3 | |
| Continuous input current | I _{REF} | -15 | mA |
| | I _{VDD} | 25 | |
| Output current | I _{GD} (tpw < 1 μs and Duty Cycle < 10%) | -0.4 to 0.8 | A |
| Operating junction temperature | T _J | -55 to +150 | °C |
| Storage temperature | T _{stg} | -65 to +150 | |
| Lead temperature | Soldering, 10 s | +300 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| VDD Input voltage | | 21 | V |
| I _{GD} Output sink current | 0 | | A |
| T _J Operating junction temperature | -40 | 105 | °C |

DISSIPATION RATINGS

| PACKAGE | θ _{JA} , THERMAL IMPEDANCE JUNCTION-TO-AMBIENT, NO AIRFLOW (°C/W) | θ _{JB} , THERMAL IMPEDANCE JUNCTION-TO-BOARD, NO AIRFLOW (°C/W) | T _A = 25°C POWER RATING (mW) | T _A = 85°C POWER RATING (mW) | T _B = 85°C POWER RATING (mW) |
|--------------|--|--|---|---|---|
| SOIC-8 (D) | 165 ⁽¹⁾ | 55 | 606 ⁽²⁾ | 242 ⁽²⁾ | 730 ⁽²⁾⁽³⁾ |
| MSOP-8 (DGK) | 181 ⁽¹⁾ | 62 | 552 ⁽²⁾ | 221 ⁽²⁾ | 664 ⁽³⁾⁽²⁾ |

- (1) Tested per JEDEC EIA/JESD51-1. Thermal resistance is a function of board construction and layout. Air flow will reduce thermal resistance. This number is included only as a general guideline; see TI document [SPRA953 IC Package Thermal Metrics](#).
 (2) Maximum junction temperature T_J, equal to 125°C.
 (3) Thermal resistance to the circuit board is lower. Measured with standard single-sided PCB construction. Board temperature, T_B, measured approximately 1 cm from the lead to board interface. This number is provided only as a general guideline.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

| | MIN | MAX | UNIT |
|------------------|-----|------|------|
| Human body model | | 2000 | V |
| CDM | | 1500 | |

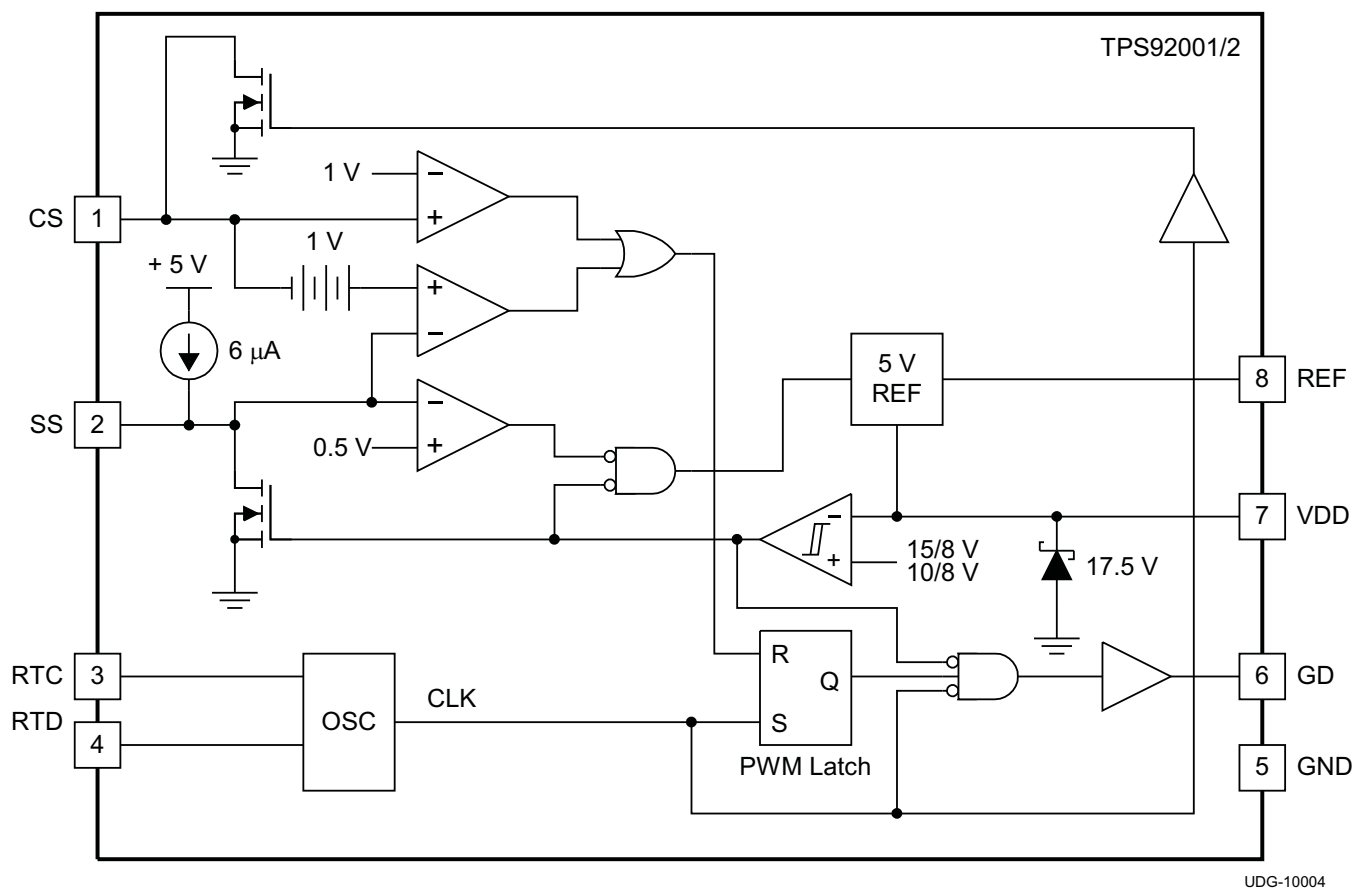
ELECTRICAL CHARACTERISTICS

 $V_{DD} = 12\text{ V}$, $C_{REF} = 0.47\text{-}\mu\text{F}$, $T_A = T_J$ (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------------------|---------------------------------------|----------|---|--|------|------|-------|------|
| SUPPLY SECTION | | | | | | | | |
| VDD | Supply clamp | | I _{VDD} = 10 mA | | 16 | 17.5 | 19 | V |
| I _{VDD} | Supply current | | No Load | | | 600 | 900 | μA |
| I _{VDD} | Supply current startup ⁽¹⁾ | | | | | 110 | | μA |
| Supply current standby | | TPS92001 | V _{VDD} = Start threshold – 300 mv | | | 110 | 125 | μA |
| | | TPS92002 | | | | 130 | 170 | |
| UNDERVOLTAGE LOCKOUT SECTION | | | | | | | | |
| Start threshold | | TPS92001 | | | 9.4 | | 10.4 | V |
| | | TPS92002 | | | 14.0 | | 15.6 | |
| UVLO hysteresis | | TPS92001 | | | 1.65 | | | |
| | | TPS92002 | | | 6.2 | | | |
| VOLTAGE REFERENCE SECTION | | | | | | | | |
| Output voltage | | | I _{REF} = 0 mA | | 4.75 | 5 | 5.25 | V |
| Line regulation | | | 10 V ≤ V _{VDD} ≤ 15 V | | | 2 | | mV |
| Load regulation | | | 0 mA ≤ I _{REF} ≤ 5 mA | | | 2 | | mV |
| COMPARATOR SECTION | | | | | | | | |
| I _{CS} | Current sense | | Output OFF | | | -100 | | nA |
| Comparator threshold | | | | | 0.9 | 0.95 | 1 | V |
| GD _{DLY} | GD propagation delay (No Load) | | 0.8 V ≤ V _{CS} ≤ 1.2 V at T _R = 10 ns | | | 50 | 100 | ns |
| SOFT START SECTION | | | | | | | | |
| I _{SS} | Soft-start current | | V _{VDD} = 16 V, V _{SS} = 0 V, -40°C ≤ T _A ≤ 85°C | | -4.9 | -7.0 | -9.1 | μA |
| | | | V _{VDD} = 16 V, V _{SS} = 0 V, -40°C ≤ T _A ≤ 85° | | -4.9 | -7.0 | -10.0 | μA |
| V _{SS} | Low-level output voltage | | V _{VDD} = 7.5 V, I _{SS} = 200 μA | | | | 0.2 | V |
| Shutdown threshold | | | | | 0.44 | 0.48 | 0.52 | V |
| OSCILLATOR SECTION | | | | | | | | |
| Switching frequency | | | R _{RTC} = 10 kΩ, R _{RTD} = 4.32 kΩ, C _{CT} = 820pF | | 90 | 100 | 110 | kHz |
| Frequency change with voltage | | | 10 V ≤ V _{VDD} ≤ 15 V | | | 0.1 | | %/V |
| V _{CT(peak)} | Timing capacitor peak voltage | | | | | 3.33 | | V |
| V _{CT(valley)} | Timing capacitor valley voltage | | | | | 1.67 | | V |
| V _{CT(p-p)} | Timing capacitor peak-to-peak voltage | | | | 1.54 | 1.67 | 1.80 | V |
| GATE DRIVE SECTION | | | | | | | | |
| Power driver V _{SAT} low | | | I _{GD} = 80 mA (dc) | | | 0.8 | 1.5 | V |
| Power driver V _{SAT} high | | | I _{GD} = -40 mA (dc), (V _{VDD} – V _{GD}) | | | 0.8 | 1.5 | V |
| Power driver low-voltage during UVLO | | | I _{GD} = 20 mA (dc) | | | | 1.5 | V |
| D _{MIN} | Minimum duty cycle | | V _{CS} = 2 V | | | 0% | | |
| D _{MAX} | Maximum duty cycle | | | | | 70% | | |
| t _{RISE} | Rise Time | | C _{GD} = 1nF | | | 35 | | ns |
| t _{FALL} | Fall Time | | C _{GD} = 1nF | | | 18 | | ns |

(1) Specified by design. Not production tested.

FUNCTIONAL BLOCK DIAGRAM

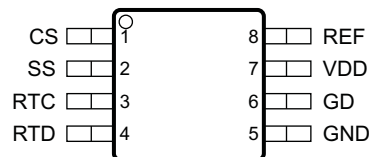
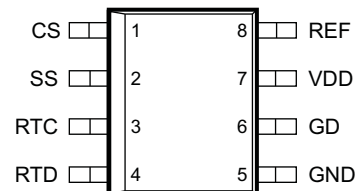


ORDERING INFORMATION

| OPERATING TEMPERATURE RANGE T _A | PACKAGE | THRESHOLD | | ORDERABLE DEVICE NUMBER | PINS | TRANSPORT MEDIA | QUANTITY |
|--|------------------------------|-----------|----------|-------------------------|------|-----------------|----------|
| | | TURN-ON | TURN-OFF | | | | |
| –40°C to 85°C | Plastic Small Outline (MSOP) | 10 | 8 | TPS92001DGK | 8 | Tube | 80 |
| | | | | TPS92001DGKR | | Tape and Reel | 2500 |
| | Plastic Small Outline (SOIC) | | | TPS92001D | | Tube | 75 |
| | | | | TPS92001DR | | Tape and Reel | 2500 |
| | Plastic Small Outline (MSOP) | 15 | | TPS92002DGK | | Tube | 80 |
| | | | | TPS92002DGKR | | Tape and Reel | 2500 |
| | Plastic Small Outline (SOIC) | | | TPS92002D | | Tube | 75 |
| | | | | TPS92002DR | | Tape and Reel | 2500 |

DEVICE INFORMATION

TPS92001/2

**DGK Package
(Top View)**

**D Package
(Top View)**


PIN FUNCTIONS

| PIN NAME | NO. | I/O | DESCRIPTION |
|----------|-----|-----|---|
| CS | 1 | I | This pin is the summing node for current sense feedback, voltage sense feedback (by optocoupler) and slope compensation. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250ohm on resistance NMOS FET during PWM off time. It offers effective leading edge blanking, with the delay set by the RC time constant of the feedback resistance from current sense resistor to CS input and the high frequency filter capacitor at this node to GND. |
| GND | 5 | – | Reference ground and power ground for all functions. |
| GD | 6 | O | This pin is the high current power driver output. A minimum series gate resistor of 3.9 Ω is recommended to limit the gate drive current when operating with high-bias voltages. |
| REF | 8 | O | The internal 5-V reference output. This reference is buffered and is available on the REF pin. The REF pin should be bypassed with a 0.47-μF ceramic capacitor to GND. |
| RTC | 3 | I | This pin connects to timing resistor R _{RTC} , and controls the positive ramp (rise) time of the internal oscillator (see Equation 1). The positive threshold of the internal oscillator is sensed through inactive timing resistor R _{RTD} which connects to pin RTD and timing capacitor, C _{CT} . $t_{RISE} = 0.74 \times (C_{CT} + 27 \text{ pF}) \times R_{RTC} \quad (1)$ |
| RTD | 4 | I | This pin connects to timing resistor RTD and controls the negative ramp (fall) time of the internal oscillator (see Equation 2). The negative threshold of the internal oscillator is sensed through inactive timing resistor R _{RTC} which connects to pin RTC and timing capacitor, C _{CT} . $t_{FALL} = 0.74 \times (C_{CT} + 27 \text{ pF}) \times R_{RTD} \quad (2)$ |
| SS | 2 | I | This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 6-μA current source. Under normal soft-start, the SS pin is discharged to at least 0.4 V and then ramps positive to 1 V during which time the output driver is held low. As the SS pin charges from 1 V to 2 V, the soft-start is implemented by an increasing output duty cycle. If the SS pin is taken below 0.5 V, the output driver is inhibited and held low. The user accessible 5-V voltage reference also goes low and I _{VDD} = 100 μA |
| VDD | 7 | I | The power input connection for this device. This pin is shunt regulated at 17.5 V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1-μF ceramic capacitor. |

APPLICATION INFORMATION

Introduction

The typical application diagrams in [Figure 3](#) and [Figure 4](#) show isolated and non-isolated flyback converters utilizing the TPS92001. Note that the capacitors C_{REF} and C_{VDD} are local decoupling capacitors for the reference and device input voltage, respectively. Both capacitors should be low ESR and ESL ceramic, placed as close as possible to the device pins, and returned directly to the ground pin of the device for best stability. The REF pin provides the internal bias to many of the device functions and C_{REF} should be at least 0.47- μ F to prevent the REF voltage from drooping.

Current Sense (CS) Pin

In the TPS92001/2, the current regulation is obtained through the summation of the primary current sense and any slope compensation at the CS pin compared to a 1-V threshold, as shown in the [FUNCTIONAL BLOCK DIAGRAM](#). Crossing this 1-V threshold resets the PWM latch and modulates the output driver on-time. In the absence of a CS signal, the output obeys the programmed maximum on-time of the oscillator. When adding slope compensation, it is important to use a small capacitor to AC couple the oscillator waveform before summing this signal into the CS pin. By forcing the CS node to exceed the 1-V threshold the TPS92001/2 is forced to zero percent duty cycle.

Oscillator

[Equation 3](#) calculates the oscillator frequency setting.

$$f_{OSC} = (0.74 \times (C_{CT} + 27\text{pF}) \times (R_{RTC} + R_{RTD}))^{-1} \quad (3)$$

$$D_{MAX} = 0.74 \times R_{TC} \times (C_T + 27\text{pF}) \times f_{OSC} \quad (4)$$

Referring to [Figure 1](#) and the waveforms in [Figure 2](#), when Q1 is on, C_{CT} charges via the on-resistance of the Q1 MOSFET and the RTC pin. During this charging process, the voltage of C_{CT} is sensed through the RTD pin. The S input of the oscillator latch, S_{OSC} , is level sensitive, so crossing the upper threshold (set at $2/3 V_{REF}$ or 3.33 V for a typical 5.0 V reference) sets the Q output (CLK signal) of the oscillator latch high. A high CLK signal results in turning off Q1 and turning on Q2. The timing capacitor then discharges through RTD and the $R_{DS(on)}$ of Q2. C_{CT} discharges from 3.33 V to the lower threshold (set at $1/3 V_{REF}$ or 1.67 V for a typical 5.0-V reference) sensed through RTC. The R input to the oscillator latch, R_{OSC} , is also level sensitive and resets the CLK signal low when C_{CT} crosses the 1.67-V threshold, turning off Q2 and turning on Q1, initiating another charging cycle.

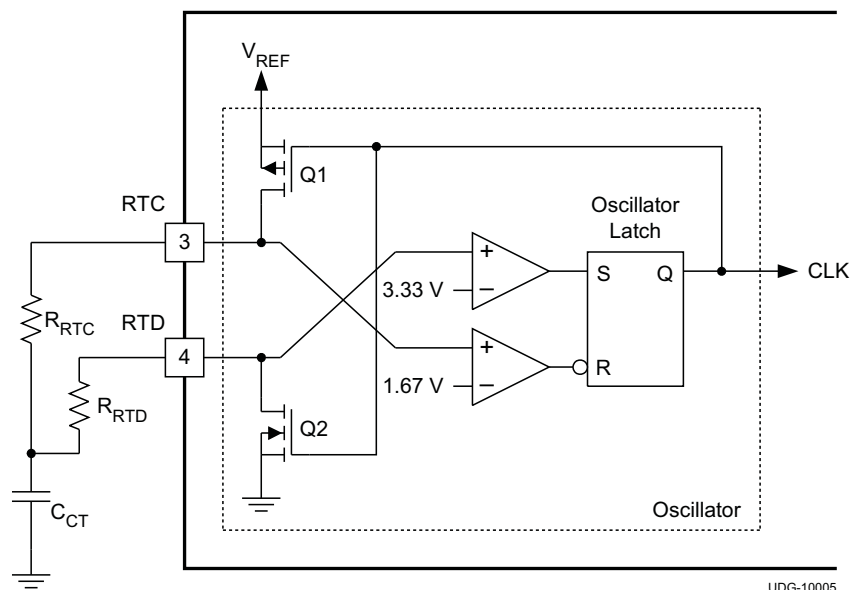


Figure 1. Oscillator Function

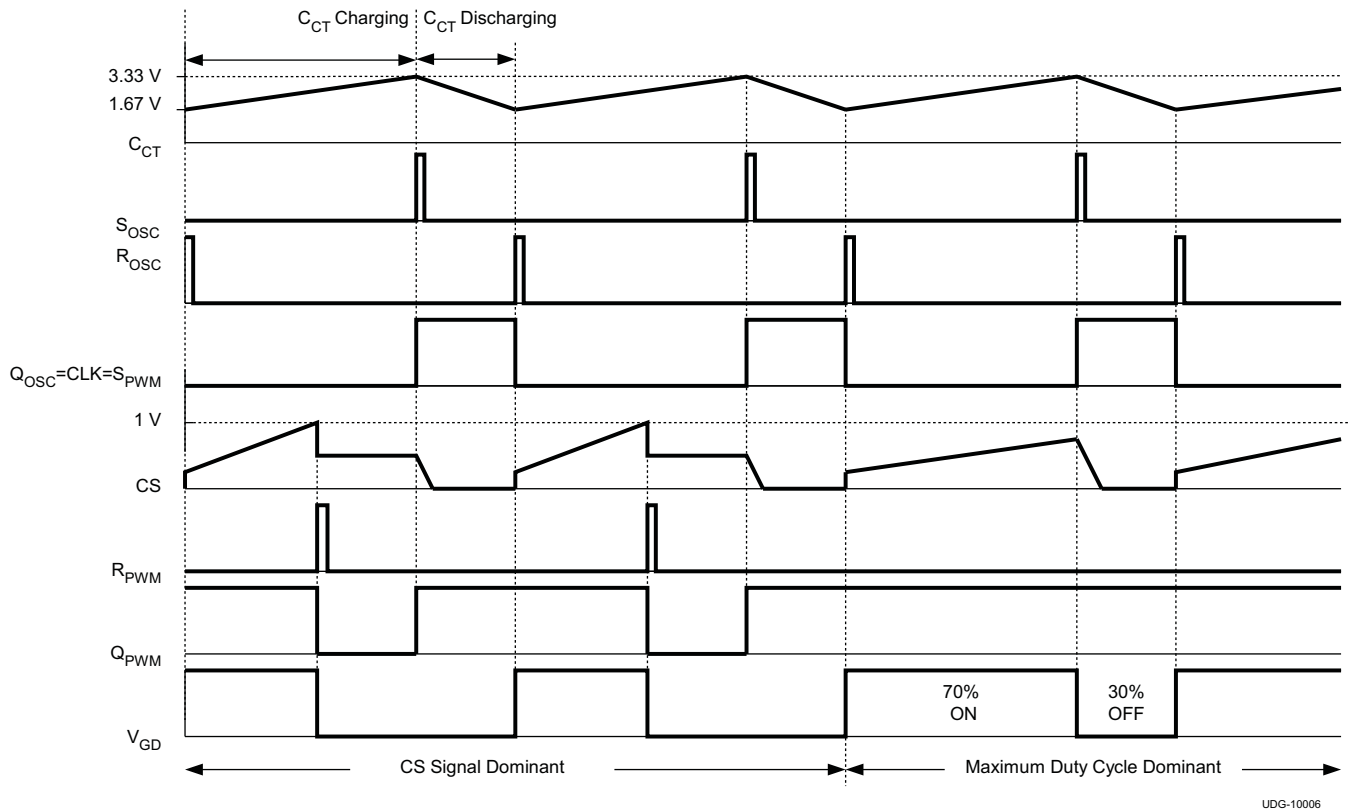


Figure 2. Oscillator Latch and PWM Latch Waveforms

Figure 2 shows the waveforms associated with the oscillator latch and the PWM latch (shown in the Typical Application Diagram). A high CLK signal not only initiates a discharge cycle for C_{CT} , it also turns on the internal N-channel MOSFET on the CS pin causing any external capacitance used for leading edge blanking connected to this pin to be discharged to ground. By discharging any external capacitor completely to ground during the external switch off-time, the noise immunity of the converter is enhanced allowing the user to design in smaller R-C components for leading edge blanking. A high CLK signal also sets the level sensitive S input of the PWM latch, S_{PWM} , high, resulting in a high output, Q_{PWM} , as shown in Figure 2. This Q_{PWM} signal remains high until a reset signal, R_{PWM} , is received. A high R_{PWM} signal results from the CS signal crossing the 1-V threshold, or during soft-start or if the SS pin is disabled.

Assuming the UVLO threshold is satisfied, the GD signal of the device remains high as long as Q_{PWM} is high and S_{PWM} , also referred to as CLK, is low. The GD signal is dominated by the CS signal as long as the CS signal trips the 1-V threshold while CLK is low. If the CS signal does not cross the 1-V threshold while CLK is low, the GD signal will be dominated by the maximum duty cycle programmed by the user. Figure 2 illustrates the various waveforms for a design set up for a maximum duty cycle of 70%.

The recommended value for C_{CT} is 1 nF for frequencies in the 100 kHz or less range and smaller C_{CT} for higher frequencies. The minimum recommended values of R_{RTC} is 10 k Ω . The minimum recommended value of R_{RTD} is 4.32 k Ω . Using these values maintains a ratio of at least 20:1 between the $R_{DS(on)}$ of the internal FETs and the external timing resistors, resulting in minimal change in frequency over temperature. Because of the oscillator susceptibility to capacitive coupling, examine the oscillator frequency by looking at the common RTC-RTD-CT node on the circuit board as opposed to looking at pins 3 and 4 directly. For good noise immunity, the RTC and RTD resistors should be placed as close to pins 3 and 4 of the device as possible. The timing capacitor should be returned directly to the ground pin of the device with minimal stray inductance and capacitance.

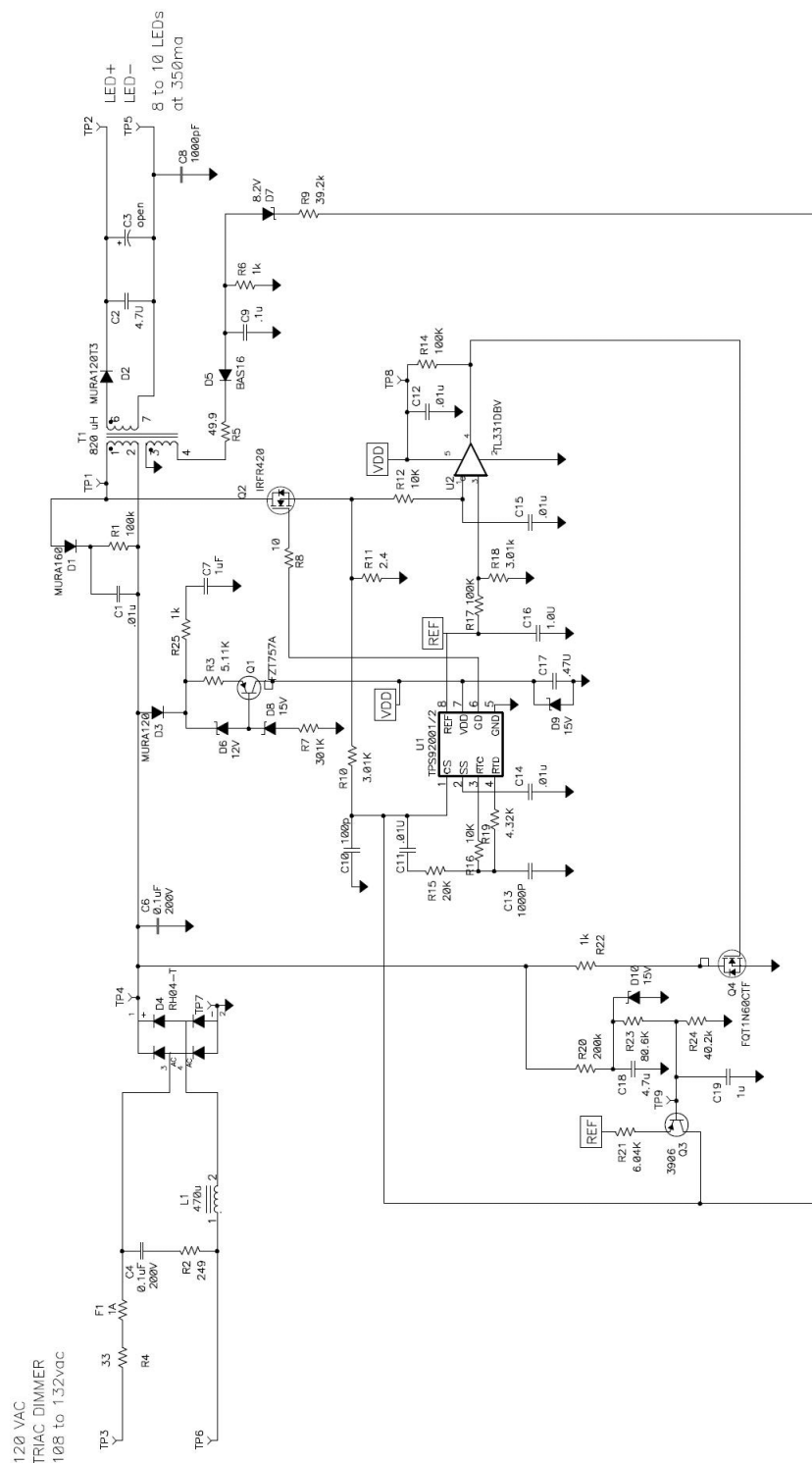


Figure 3. Isolated Flyback with TRIAC Dimming Interface

CAUTION

Do not operate the Isolated Flyback described in [Figure 3](#) without load.

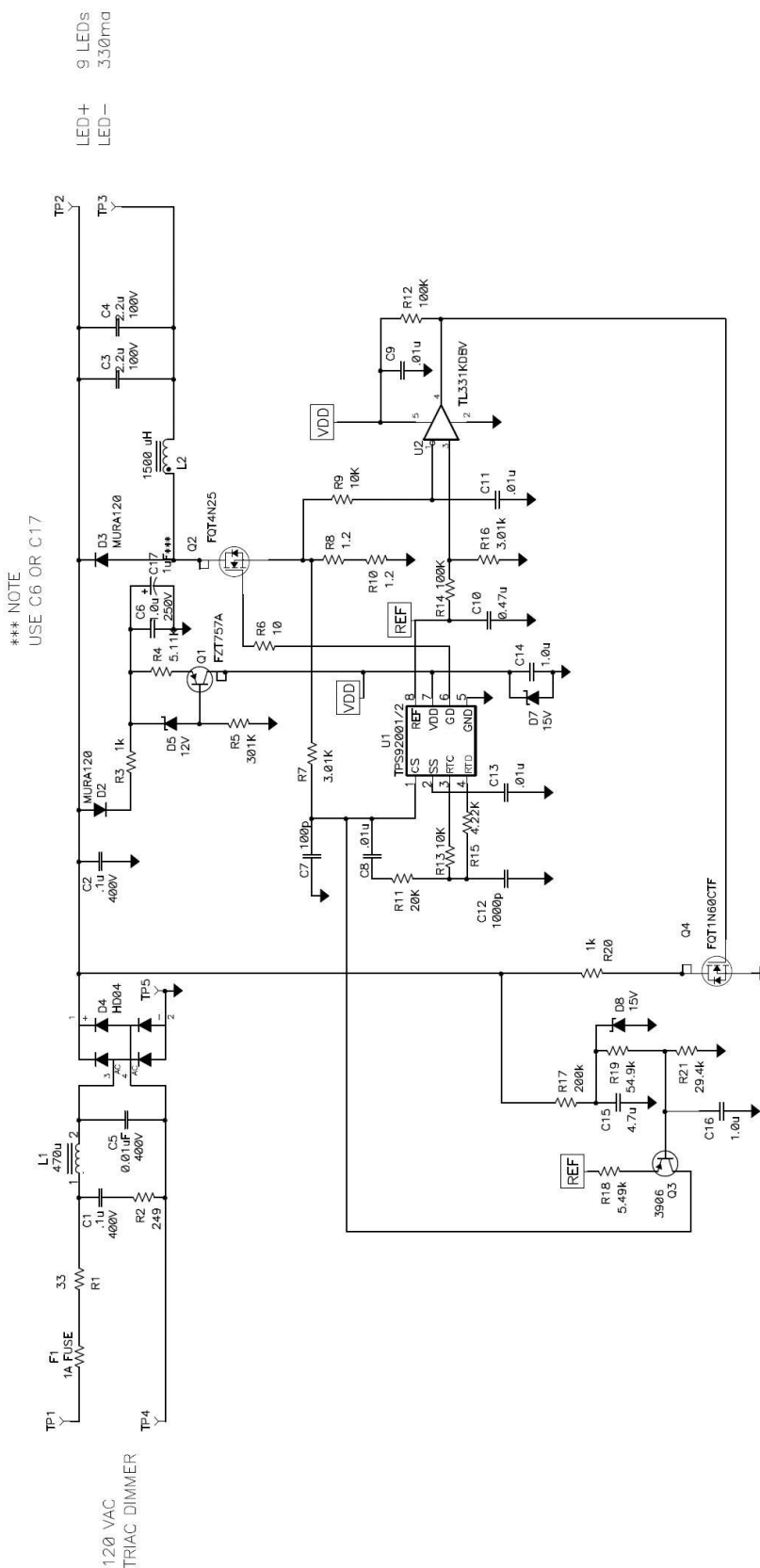


Figure 4. Low-Side (Inverted) Buck with TRIAC Dimming Interface

TYPICAL CHARACTERISTICS

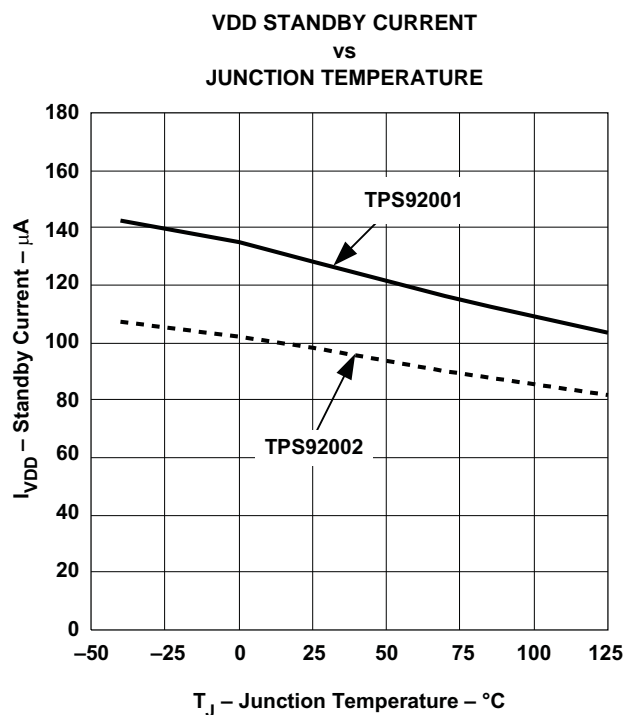


Figure 5.

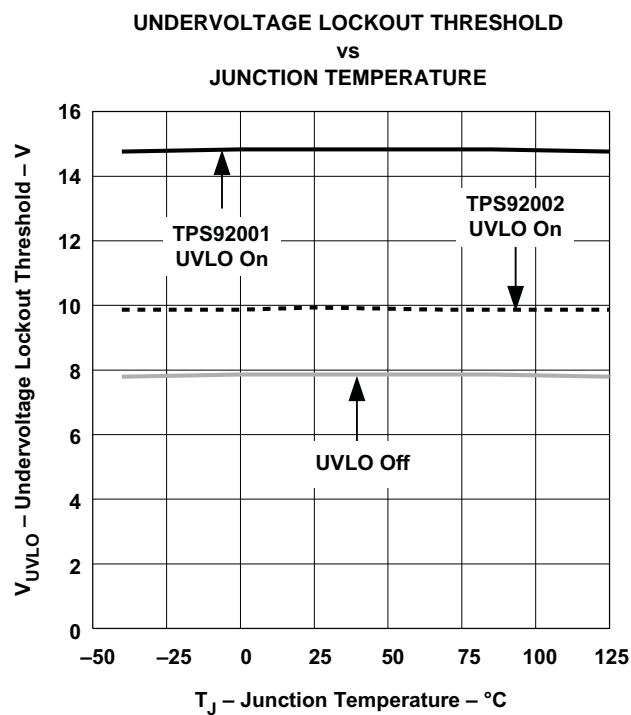


Figure 6.

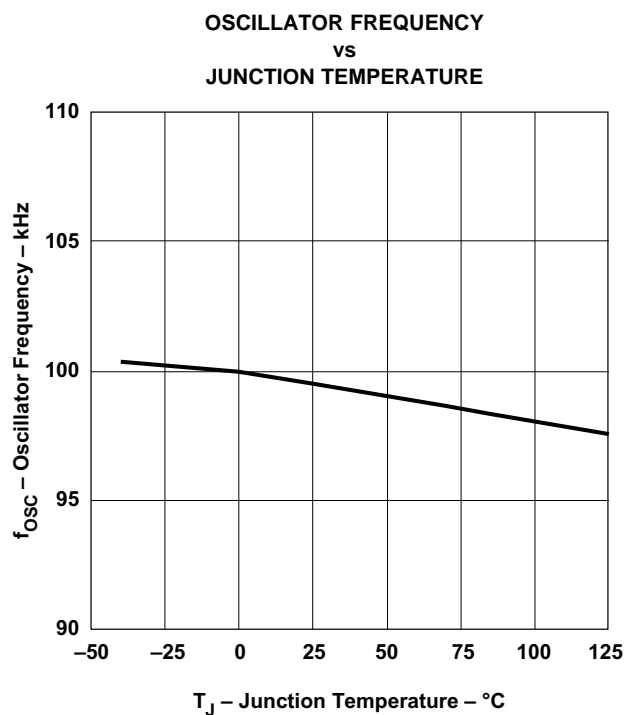


Figure 7.

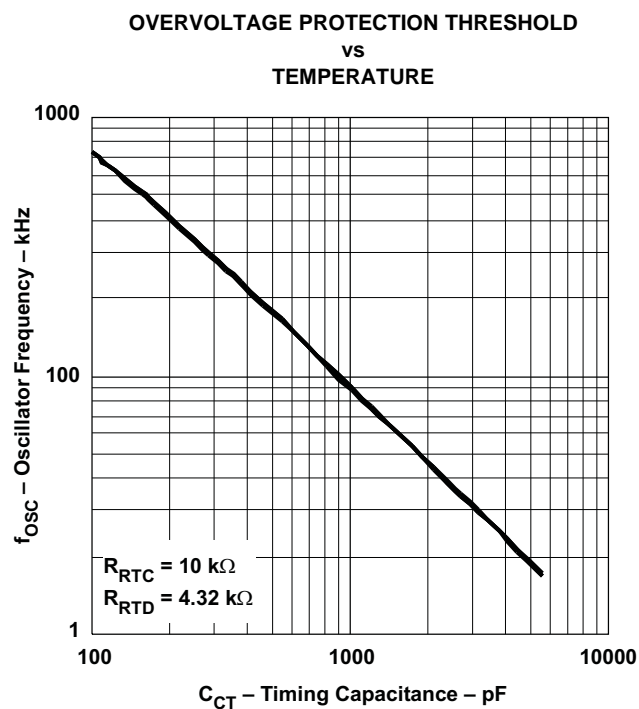


Figure 8.

REVISION HISTORY

| Changes from Original (FEBRUARY 2010) to Revision A | Page |
|---|-------------------|
| • Changed diode direction | 1 |
| • Changed Figure 4 title | 9 |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TPS92001D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TPS92001DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | |
| TPS92001DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | |
| TPS92001DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TPS92002D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TPS92002DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | |
| TPS92002DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | |
| TPS92002DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS92001DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS92001DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS92002DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS92002DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS92001DGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS92001DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS92002DGKR | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS92002DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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