

# 300-mA 40-V LOW-DROPOUT REGULATOR WITH 25- $\mu$ A QUIESCENT CURRENT

Check for Samples: [TPS7A6533-Q1](#), [TPS7A6550-Q1](#)

## FEATURES

- **Low Dropout Voltage**
  - 300 mV at  $I_{OUT} = 150$  mA
- **4-V to 40-V Wide Input Voltage Range With up to 45-V Transients**
- **300-mA Maximum Output Current**
- **25- $\mu$ A (Typ) Ultralow Quiescent Current at Light Loads**
- **3.3-V and 5-V Fixed Output Voltage With  $\pm 2\%$  Tolerance**
- **Low-ESR Ceramic Output Stability Capacitor**
- **Integrated Fault Protection**
  - Short-Circuit and Overcurrent Protection
  - Thermal Shutdown
- **Low Input-Voltage Tracking**
- **Thermally Enhanced Power Package**
  - 3-Pin TO-252 (KVU /DPAK)

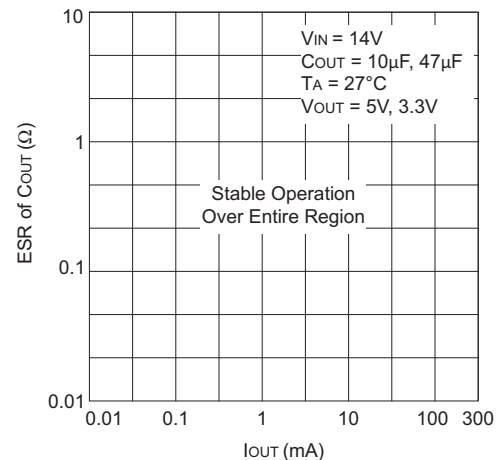
## APPLICATIONS

- **Qualified for Automotive Applications**
- **Infotainment Systems With Sleep Mode**
- **Body Control Modules**
- **Always-On Battery Applications**
  - Gateway Applications
  - Remote Keyless Entry Systems
  - Immobilizers

## DESCRIPTION

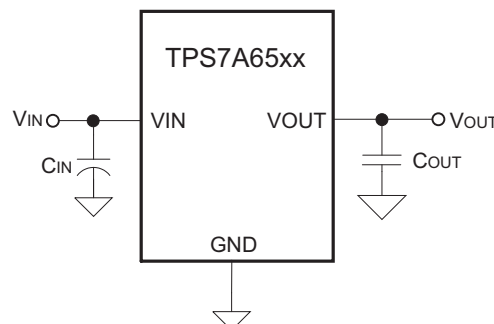
The TPS7A65xx-Q1 is a family of low-dropout linear voltage regulators designed for low power consumption and quiescent current less than 25  $\mu$ A in light-load applications. These devices feature integrated overcurrent protection and a design to achieve stable operation even with low-ESR ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, these devices are well-suited in power supplies for various automotive applications.

### TYPICAL REGULATOR STABILITY



**Figure 1. ESR versus Load Current for TPS7A6550-Q1**

### TYPICAL APPLICATION SCHEMATIC



**Figure 2. Application Schematic**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION<sup>(1)</sup>

OUTPUT VOLTAGE	PACKAGE	TOP-SIDE MARKING	ORDERABLE PART NUMBER
5 V	3-pin KVVU	Tube of 70	7A6550Q1
		Reel of 2500	7A6550Q1
3.3 V	3-pin KVVU	Reel of 2500	7A6533Q1

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

NO.	DESCRIPTION	VALUE	UNIT
1.1	$V_{IN}$ Unregulated input <sup>(2)(3)</sup>	45	V
1.2	$V_{OUT}$ Regulated output	7	V
1.3	$\theta_{JP}$ Thermal impedance junction to exposed pad KVVU (DPAK) package	1.2	°C/W
1.4	$\theta_{JA}$ Thermal impedance junction to ambient KVVU (DPAK) package <sup>(4)</sup>	29.3	°C/W
1.5	$\theta_{JA}$ Thermal impedance junction to ambient KVVU (DPAK) package <sup>(5)</sup>	38.6	°C/W
1.6	ESD Electrostatic discharge <sup>(6)</sup>	2	kV
1.7	$T_A$ Operating ambient temperature	125	°C
1.8	$T_{stg}$ Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
- (2) Absolute negative voltage on these pins not to go below –0.3 V.
- (3) Absolute maximum voltage for duration less than 480 ms.
- (4) The thermal data is based on JEDEC standard high-K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
- (5) The thermal data is based on JEDEC standard low-K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
- (6) The human-body model is a 100-pF capacitor discharged through a 1.5-k $\Omega$  resistor into each pin.

## DISSIPATION RATINGS

NO.	JEDEC STANDARD	PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING (W)	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ (°C/W)	$T_A = 85^\circ\text{C}$ POWER RATING (W)
2.1	JEDEC Standard PCB - low K, JESD 51-3	3 pin KVVU	3.24	38.6	1.68
2.2	JEDEC Standard PCB - high K, JESD 51-5	3 pin KVVU	4.27	29.3	2.22

## RECOMMENDED OPERATING CONDITIONS

NO.	DESCRIPTION	MIN	MAX	UNIT
3.1	$V_{IN}$ Unregulated input voltage	4	40	V
3.2	$T_J$ Operating junction temperature range	–40	150	°C

## ELECTRICAL CHARACTERISTICS

 $V_{IN} = 14V$ ,  $T_J = -40^{\circ}C$  to  $150^{\circ}C$  (unless otherwise noted)

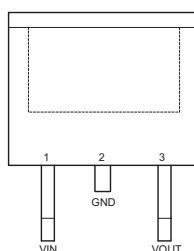
NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4. Input Voltage (VIN pin)							
4.1	VIN	Input voltage	Fixed 5-V output, IOUT = 1 mA	5.3		40	V
			Fixed 3.3-V output, IOUT = 1 mA	3.6		40	
4.2	IQUIESCENT	Quiescent current	VIN = 8.2 V to 18 V, IOUT = 0.01 mA to 0.75 mA		25	40	μA
4.3	VIN-UVLO	Undervoltage lockout voltage	Ramp VIN down until output is turned OFF		3.16		V
4.4	VIN(POWERUP)	Power-up voltage	Ramp VIN up until output is turned ON		3.45		V
5. Regulated Output Voltage (VOUT pin)							
5.1	VOUT	Regulated output voltage	Fixed VOUT value (3.3 V or 5 V as applicable), IOUT = 10 mA, 10 mA to 300 mA, VIN = VOUT + 1 V to 16 V	-2%		2%	
5.2	ΔVLINE-REG	Line regulation	VIN = 6 V to 28 V, IOUT = 10 mA, VOUT = 5 V			15	mV
			VIN = 6 V to 28 V, IOUT = 10 mA, VOUT = 3.3 V			20	mV
5.3	ΔVLOAD-REG	Load regulation	IOUT = 10 mA to 300 mA, VIN= 14 V, VOUT = 5 V			25	mV
			IOUT = 10 mA to 300 mA,VIN = 14 V, VOUT = 3.3 V			35	mV
5.4	VDROPOUT <sup>(1)</sup>	Dropout voltage (VIN – VOUT)	IOUT = 250 mA			500	mV
			IOUT = 150 mA			300	mV
5.5	R <sub>SW</sub> <sup>(2)</sup>	Switch resistance	VIN to VOUT resistance			2	Ω
5.6	IOUT	Output current	VOUT in regulation	0		300	mA
5.7	ICL	Output current limit	VOUT = 0 V (VOUT pin is shorted to ground)	350		1000	mA
5.8	PSRR <sup>(2)</sup>	Power-supply ripple rejection	VIN-RIPPLE = 0.5 Vpp, IOUT = 300 mA, frequency = 100 Hz, VOUT = 5 V, and VOUT = 3.3 V		60		dB
			VIN-RIPPLE = 0.5 Vpp, IOUT = 300 mA, frequency = 150 kHz, VOUT = 5 V, and VOUT = 3.3 V		30		
6. Operating Temperature Range							
6.1	TJ	Operating junction temperature		-40		150	°C
6.2	TSHUTDOWN	Thermal shutdown trip point			165		°C
6.3	THYST	Thermal shutdown hysteresis			10		°C

(1) This test is done with  $V_{OUT}$  in regulation and  $V_{IN} - V_{OUT}$  parameter is measured when  $V_{OUT}$  (3.3 V or 5 V) drops by 100 mV at specified loads.

(2) Specified by design – not tested

## DEVICE INFORMATION

KVU PACKAGE  
(TOP VIEW)



## TERMINAL FUNCTIONS

NO.	NAME	TYPE	DESCRIPTION
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between VIN pin and GND pin to dampen input line transients.
2	GND	I/O	Ground pin: This is signal ground pin of the IC.
3	VOUT	O	Regulated output voltage pin: This is a regulated voltage output ( $V_{OUT} = 3.3\text{ V}$ or $5\text{ V}$ , as applicable) pin with a limitation on maximum output current. In order to achieve stable operation and prevent oscillation, an external output capacitor ( $C_{OUT}$ ) with low ESR is connected between this pin and the GND pin.

## FUNCTIONAL BLOCK DIAGRAM

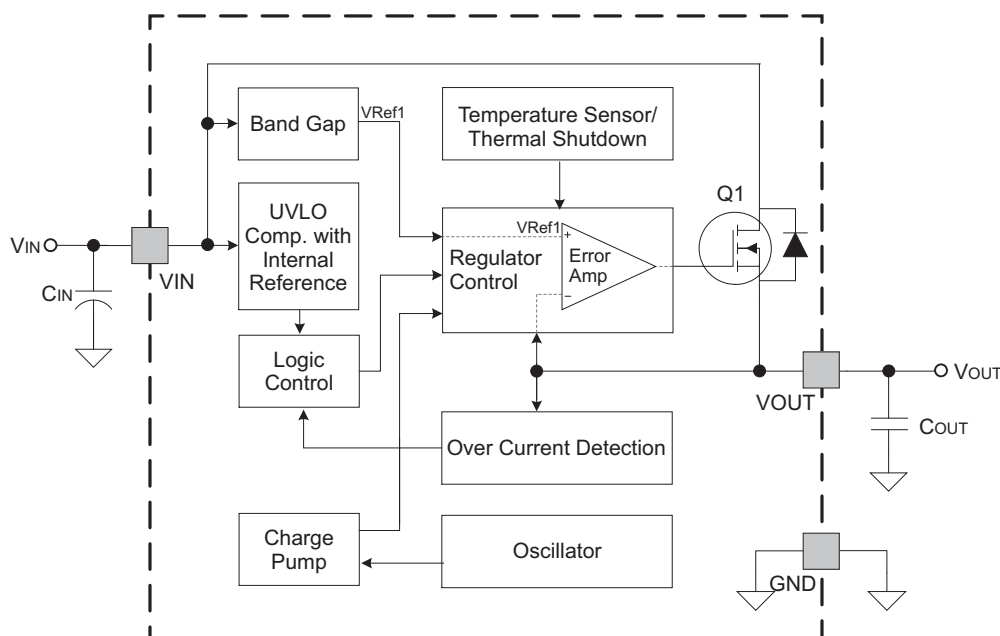
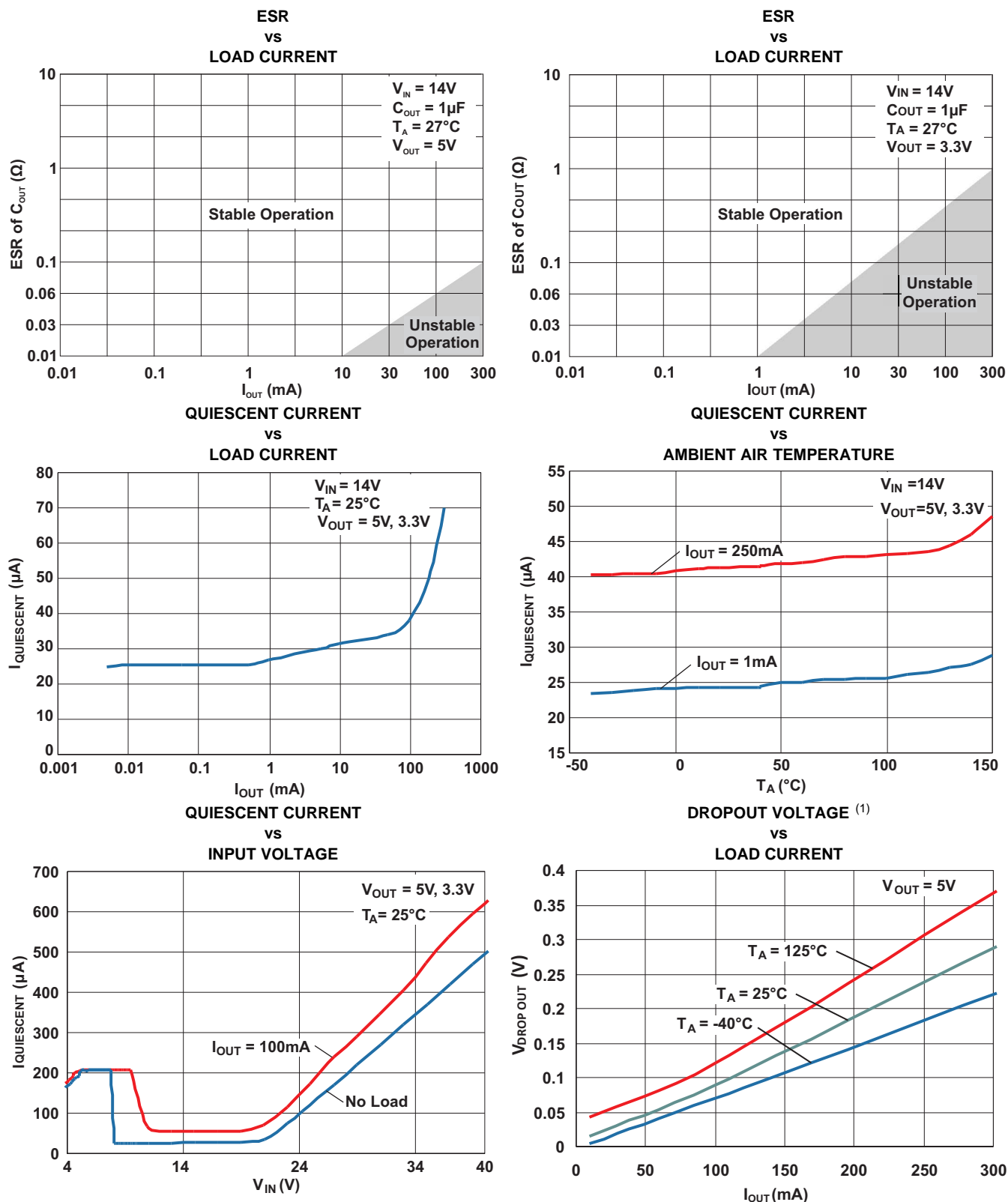


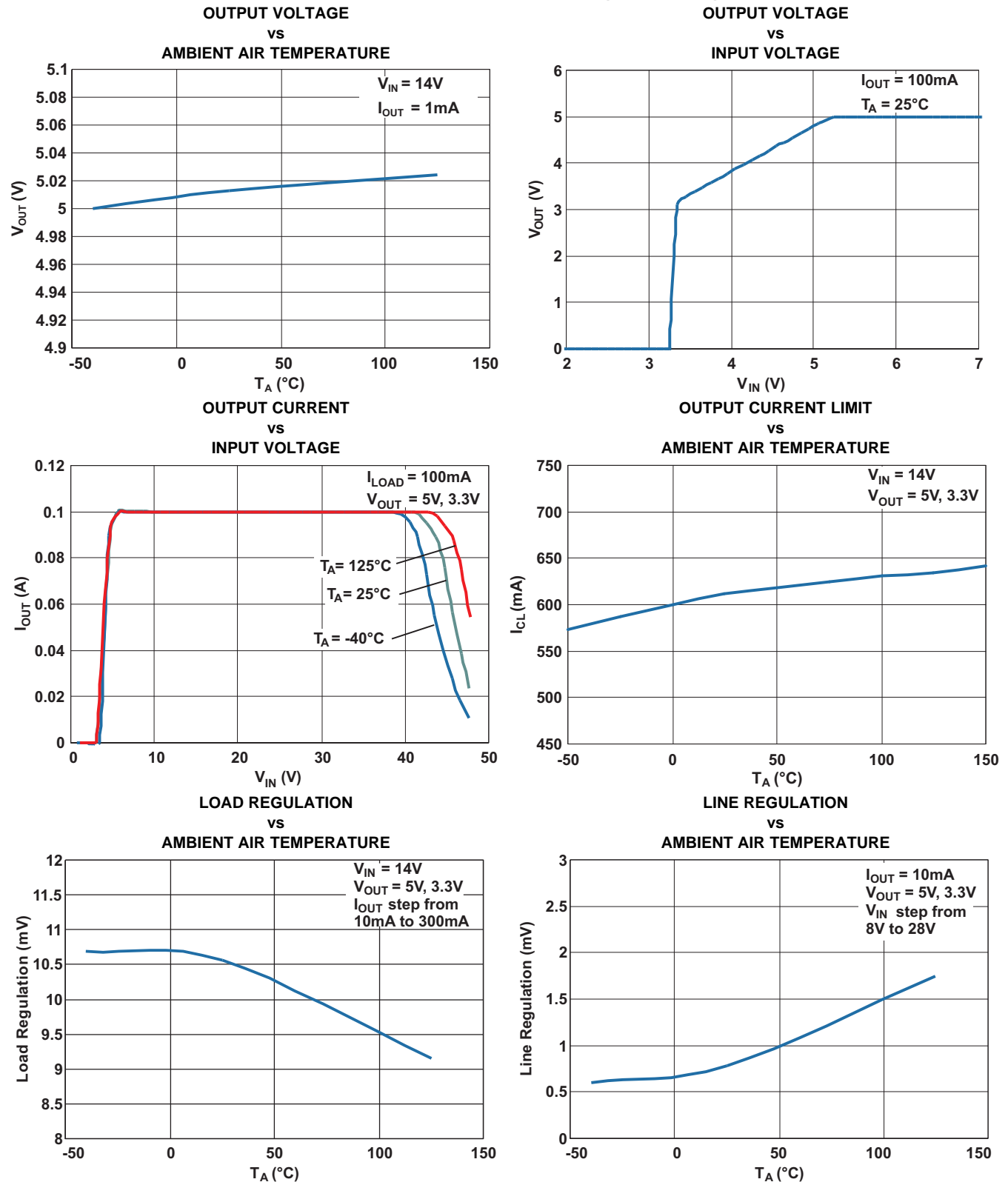
Figure 3. TPS7A65xx-Q1 Functional Block Diagram

## TYPICAL CHARACTERISTICS

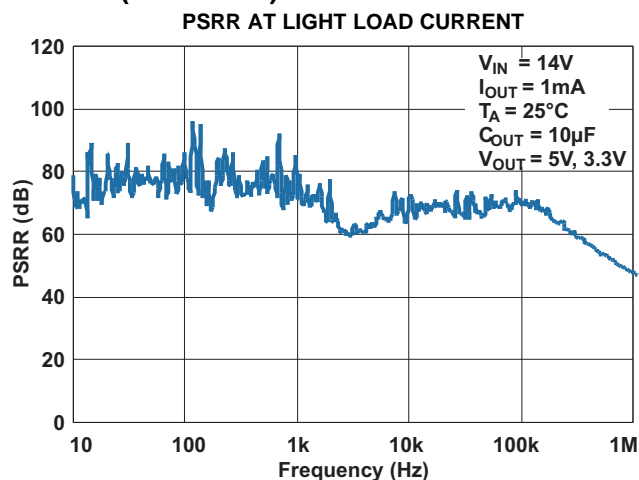
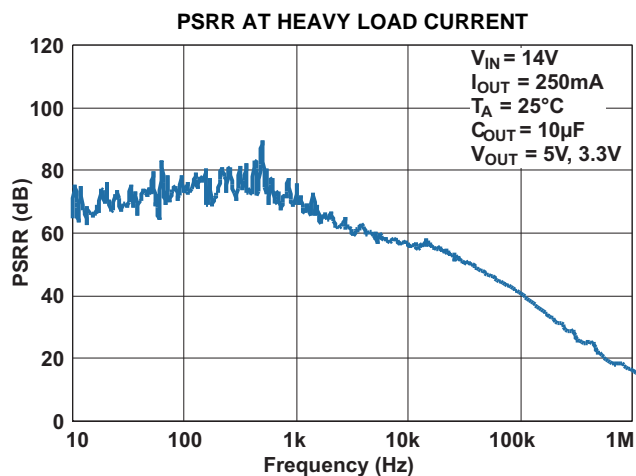


(1) Dropout voltage is measured when the output voltage drops by 100mV from the regulated output voltage level. (For example, the drop out voltage for TPS7A6550 is measured when the output voltage drops down to 4.9V from 5V.)

## TYPICAL CHARACTERISTICS (continued)



## TYPICAL CHARACTERISTICS (continued)



## DETAILED DESCRIPTION

TPS7A65xx-Q1 is a family of monolithic low-dropout linear voltage regulators designed for low power consumption and quiescent current less than 25  $\mu\text{A}$  in light-load applications. Because of an integrated fault protection, these devices are well-suited in power supplies for various automotive applications.

These devices are available in two fixed-output-voltage versions as follows:

- 5-V output version (TPS7A6550-Q1)
- 3.3-V output version (TPS7A6533-Q1)

The following section describes the features of TPS7A65xx-Q1 voltage regulators in detail.

### Power Up

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ( $V_{\text{IN(POWERUP)}}$ ) level, the output voltage begins to ramp up; see Figure 4.

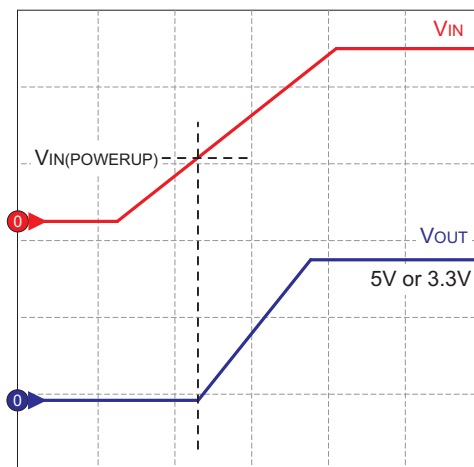


Figure 4. Power-Up Sequence

### Charge-Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry does not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input

voltages. The charge-pump switching thresholds are hysteretic. Figure 5 and Figure 6 show typical switching thresholds for the charge pump at light ( $I_{\text{OUT}} < \text{approximately } 2 \text{ mA}$ ) and heavy ( $I_{\text{OUT}} > \text{approximately } 2 \text{ mA}$ ) loads, respectively.

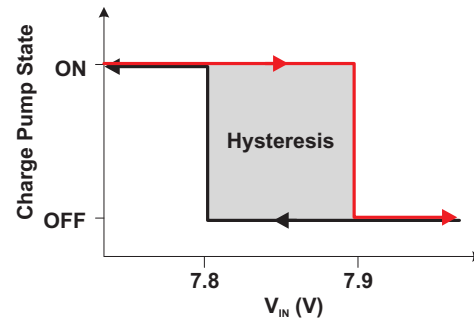


Figure 5. Charge-Pump Operation at Light Loads

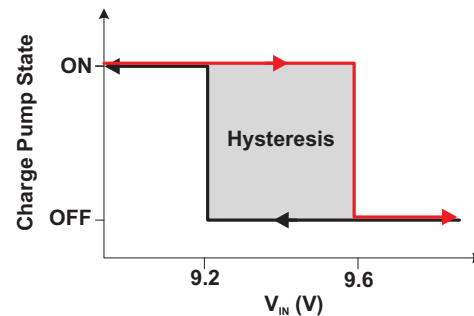


Figure 6. Charge-Pump Operation at Heavy Loads

### Low-Power Mode

At light loads and high input voltages ( $V_{\text{IN}} > \text{approximately } 8 \text{ V}$  such that charge pump is off) the device operates in the low-power mode and the quiescent current consumption decreases to 25  $\mu\text{A}$  (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

$I_{\text{OUT}}$	Charge Pump ON	Charge Pump OFF
$I_{\text{OUT}} < \text{approximately } 2 \text{ mA}$ (light load)	250 $\mu\text{A}$	25 $\mu\text{A}$ (low-power mode)
$I_{\text{OUT}} > \text{approximately } 2 \text{ mA}$ (heavy load)	280 $\mu\text{A}$	70 $\mu\text{A}$

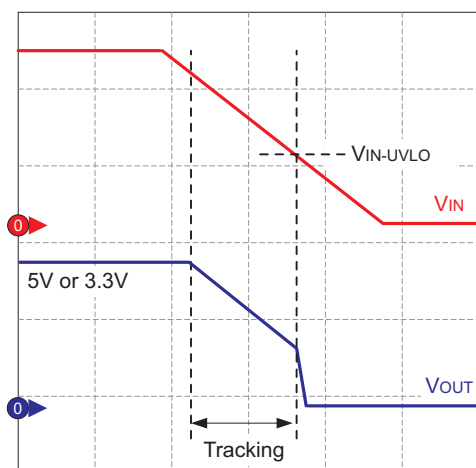


## Undervoltage Shutdown

These devices have an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage ( $V_{IN}$ ) falls below an internally fixed UVLO threshold level ( $V_{IN-UVLO}$ ) as shown in Figure 7. This ensures that the regulator does not latch into an unknown state during low input-voltage conditions. The regulator normally powers up when the input voltage exceeds the  $V_{IN(PowerUP)}$  threshold.

## Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks input minus a voltage based on the load current ( $I_{OUT}$ ) and switch resistance ( $R_{SW}$ ) as shown in Figure 7. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions.



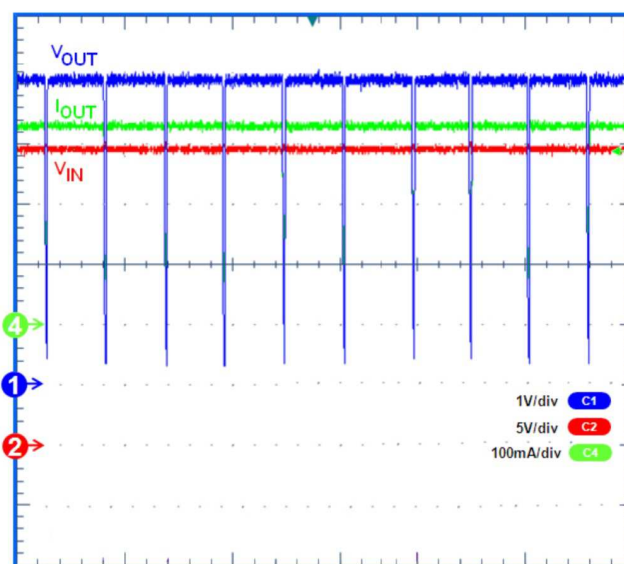
**Figure 7. Undervoltage Shutdown and Low-Voltage Tracking**

## Integrated Fault Protection

These devices feature integrated fault protection to make them ideal for use in automotive applications. In order to keep them in a safe area of operation during certain fault conditions, they use internal current-limit protection and current-limit foldback to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short-circuit condition on the output; limiting current through the pass element to  $I_{CL}$  protects the device from excessive power dissipation.

## Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again. Figure 8 shows this.



**Figure 8. Thermal Cycling Waveform for TPS7A6550-Q1 ( $V_{IN} = 24\text{ V}$ ,  $I_{OUT} = 300\text{ mA}$ ,  $V_{OUT} = 5\text{ V}$ )**

## APPLICATION INFORMATION

A typical application circuit for TPS7A65xx-Q1 is [Figure 9](#). Depending on the end application, one may use different values of external components. An application may require a larger output capacitor during fast load steps to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. The user can additionally connect a bypass capacitor at the output to decouple high-frequency noise as per the end application.

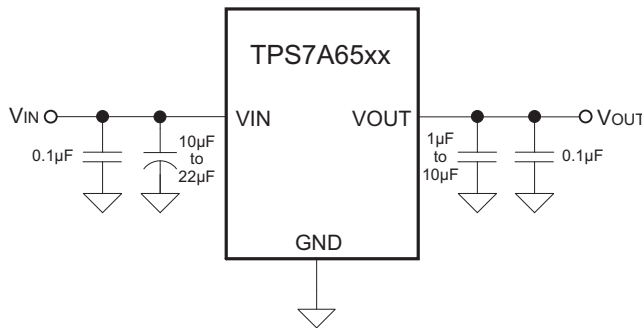


Figure 9. Typical Application Schematic

### Power Dissipation and Thermal Considerations

Calculate the power dissipated in the device using [Equation 1](#).

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN} \quad (1)$$

where,

$P_D$  = continuous power dissipation

$I_{OUT}$  = output current

$V_{IN}$  = input voltage

$V_{OUT}$  = output voltage

$I_{QUIESCENT}$  = quiescent current

$I_{QUIESCENT} \ll I_{OUT}$ ; therefore, ignore the term  $I_{QUIESCENT} \times V_{IN}$  in [Equation 1](#).

For a device under operation at a given ambient air temperature ( $T_A$ ), calculate the junction temperature ( $T_J$ ) using [Equation 2](#).

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (2)$$

where,

$\theta_{JA}$  = junction-to-ambient air thermal impedance

Calculate the rise in junction temperature due to power dissipation using [Equation 3](#).

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (3)$$

For a given maximum junction temperature ( $T_{J-Max}$ ), calculate the maximum ambient air temperature ( $T_{A-Max}$ ) at which the device can operate using [Equation 4](#).

$$T_{A-Max} = T_{J-Max} - (\theta_{JA} \times P_D) \quad (4)$$

### Example

If  $I_{OUT} = 100 \text{ mA}$ ,  $V_{OUT} = 5 \text{ V}$ ,  $V_{IN} = 14 \text{ V}$ ,  $I_{QUIESCENT} = 250 \text{ }\mu\text{A}$  and  $\theta_{JA} = 30^\circ\text{C/W}$ , the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is  $27^\circ\text{C}$ . For a maximum junction temperature of  $150^\circ\text{C}$ , maximum ambient air temperature at which the device can operate is  $123^\circ\text{C}$ .

For adequate heat dissipation, TI recommends soldering the power pad (exposed heat sink) to the thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. [Figure 10](#) shows power derating curves for the TPS7A65xx-Q1 family of devices in the KVVU (DPAK) package.

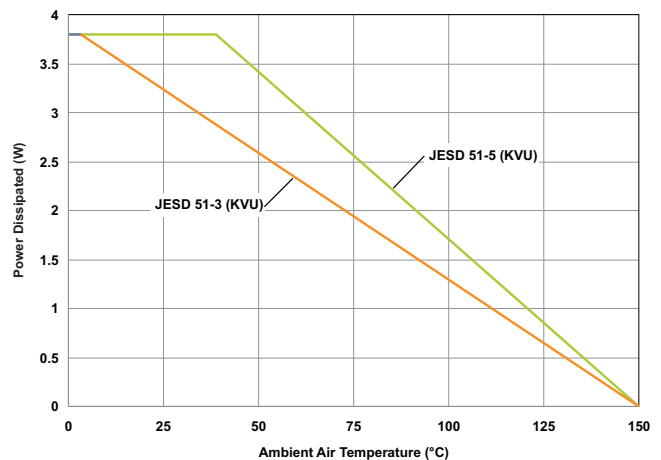
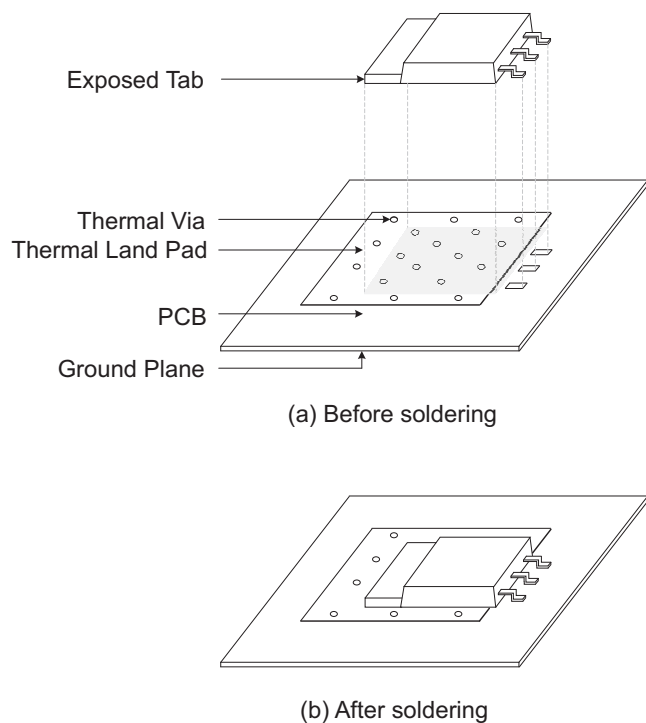


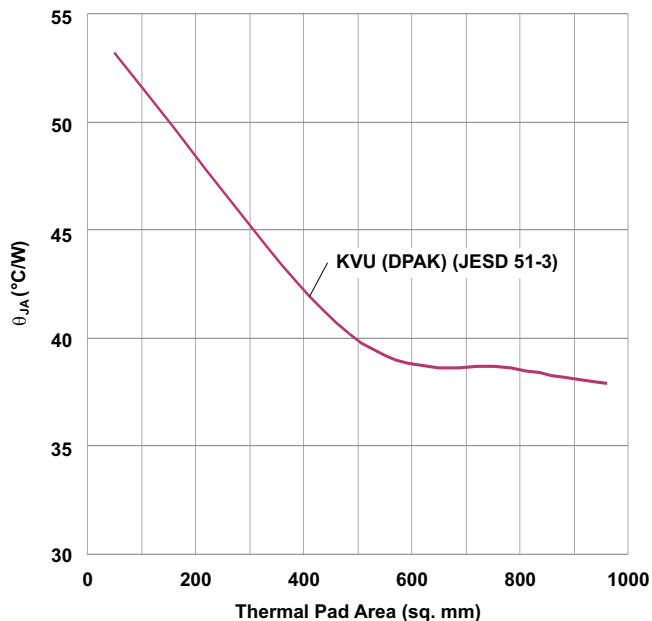
Figure 10. Power Derating Curves

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad. [Figure 11](#) (a) and (b) show this. Further, a design can improve the heat-spreading capabilities of a PCB considerably by using a thicker ground plane and a thermal land pad with a larger surface area.



**Figure 11. Using a Multilayer PCB and Thermal Vias For Adequate Heat Dissipation**

Keeping other factors constant, the surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 12 shows the variation of  $\theta_{JA}$  with surface area of the thermal land pad (soldered to the exposed pad) for the KVU package.



**Figure 12.  $\theta_{JA}$  versus Thermal Pad Area**

## REVISION HISTORY

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Changes from Original (May 2010) to Revision A	Page
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- |                                     |                   |
|-------------------------------------|-------------------|
| • Removed all KKT information. .... | <a href="#">2</a> |
|-------------------------------------|-------------------|
- 

Changes from Revision A (November 2011) to Revision B	Page
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- |   |                   |
|---|-------------------|
| • Changed the $\theta_{JP}$ value in the Abs Max Table From: 12.7 To: 1.2°C/W ..... | <a href="#">2</a> |
|---|-------------------|
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Changes from Revision B (November 2011) to Revision C	Page
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- |  |                   |
|--|-------------------|
| • Deleted the TPS7A6533-Q1 device .....  | <a href="#">1</a> |
| • Changed the Regulated Output Voltage (5.1). Added to Test Conditions "10mA to 300mA, $V_{IN} = V_{OUT} + 1V$ to 16V" ..... | <a href="#">3</a> |
-

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS7A6533QKVURQ1	ACTIVE	PFM	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	
TPS7A6550QKVURQ1	ACTIVE	PFM	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6533QKVURQ1	PFM	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6550QKVURQ1	PFM	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

## TAPE AND REEL BOX DIMENSIONS



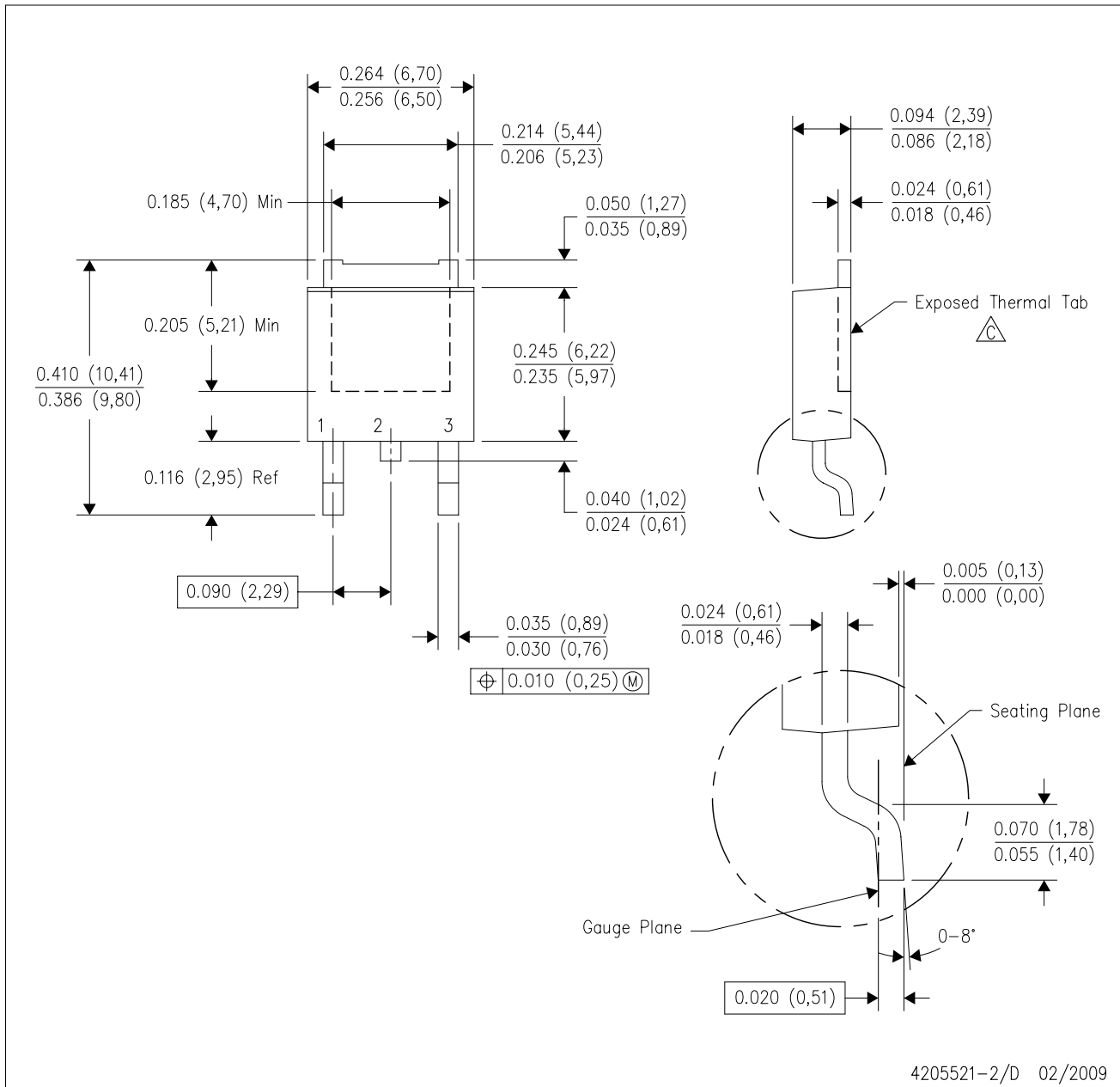
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6533QKVURQ1	PFM	KVU	3	2500	340.0	340.0	38.0
TPS7A6550QKVURQ1	PFM	KVU	3	2500	340.0	340.0	38.0

## MECHANICAL DATA

KVU (R-PSFM-G3)

# PLASTIC FLANGE-MOUNT PACKAGE



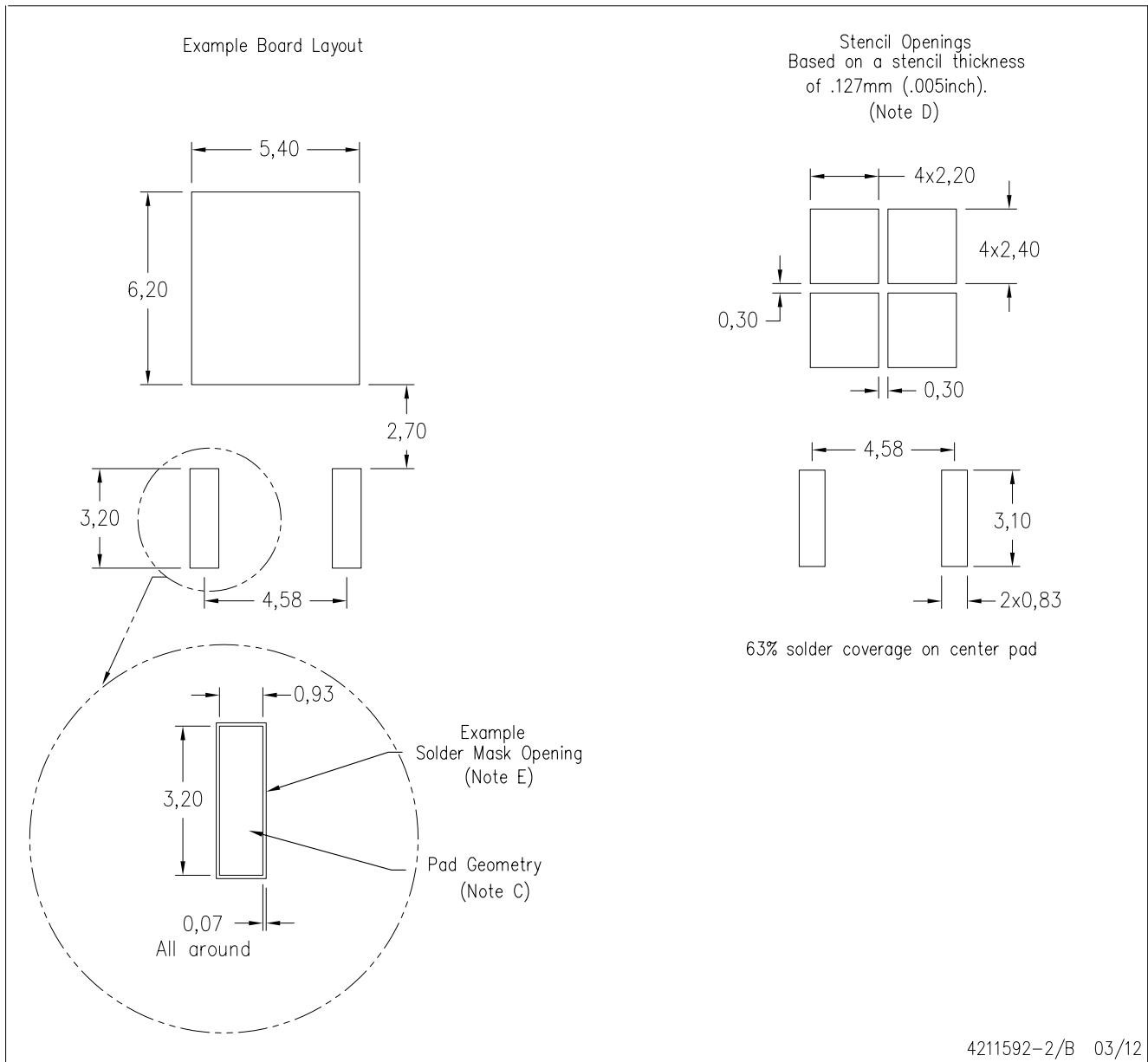
NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
**C.** The center lead is in electrical contact with the exposed thermal tab.  
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.  
E. Falls within JEDEC TO-252 variation AA.



KVU (R-PSFM-G3)

PLASTIC FLANGE MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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