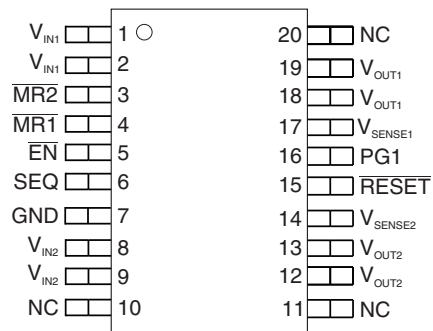


DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS WITH POWER UP SEQUENCING FOR SPLIT VOLTAGE DSP SYSTEMS

FEATURES

- Dual Output Voltages for Split-Supply Applications
- Selectable Power Up Sequencing for DSP Applications
- –55°C to 125°C Operating Temperature
- Output Current Range of 1 A on Regulator 1 and 2 A on Regulator 2
- Fast Transient Response
- Voltage Options Are 3.3 V/2.5 V
- Open Drain Power-On Reset With 120-ms Delay
- Open Drain Power Good for Regulator 1
- Ultralow 185-μA (typical) Quiescent Current
- 2-μA Input Current During Standby
- Low Noise: 78-μVRMS Without Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- Two Manual Reset Inputs
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 20-Pin Ceramic Flatpack Package
- Thermal Shutdown Protection

**HKH PACKAGE
(TOP VIEW)**



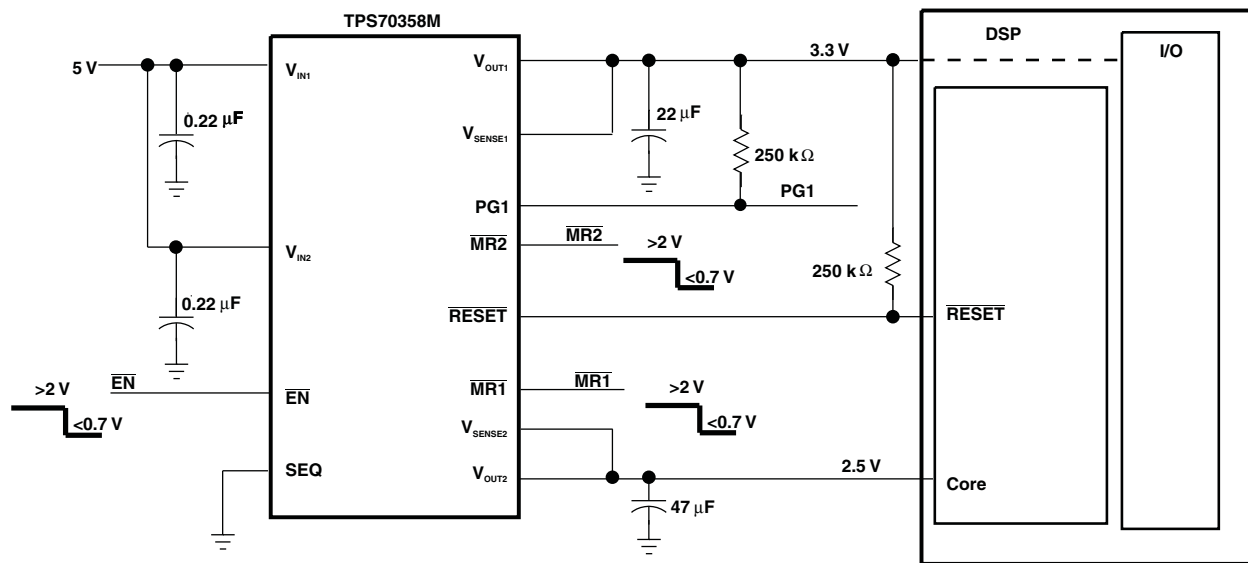
NC - No internal connection

DESCRIPTION

The TPS70358 is designed to provide a complete power management solution for TI DSP, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any TI DSP applications with power sequencing requirement. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset inputs, and enable function, provide a complete system solution.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



DESCRIPTION (CONTINUED)

The TPS70358 regulator offers very low dropout voltage and dual outputs with power up sequence control, which is designed primarily for DSP applications. These devices have low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 47-µF low ESR capacitors.

The TPS70358 has a fixed 3.3-V/2.5-V voltage option. Regulator 1 can support up to 1 A, and regulator 2 can support up to 2 A. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low (typically 160 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 250 µA over the full range of output current). This LDO family also features a sleep mode; applying a high signal to EN (enable) shuts down both regulators, reducing the input current to 1 µA at $T_j = 25^\circ\text{C}$.

The device is enabled when the EN pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the V_{SENSE1} and V_{SENSE2} pins respectively.

The input signal at the SEQ pin controls the power-up sequence of the two regulators. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time V_{OUT1} is turned on. If V_{OUT2} is pulled below 83% (i.e. overload condition) of its regulated voltage, V_{OUT1} will be turned off. Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} is turned on first. The SEQ pin is connected to an internal pullup current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage conditions at V_{OUT1} . The PG1 pin can be used to implement a SVS (power on reset) for the circuitry supplied by regulator 1.

The TPS70358 features a RESET (SVS, POR, or power on reset). RESET is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, RESET goes to a high impedance state (i.e. logic high) after a 120-ms delay when all three of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset (MR) pin must be in a high impedance state. Third, V_{OUT2} must be above approximately 95% of its regulated voltage. To monitor V_{OUT1} , the PG1 output pin can be connected to MR1 or MR2. RESET can be used to drive power on reset or a low-battery indicator. If RESET is not used, it can be left floating.

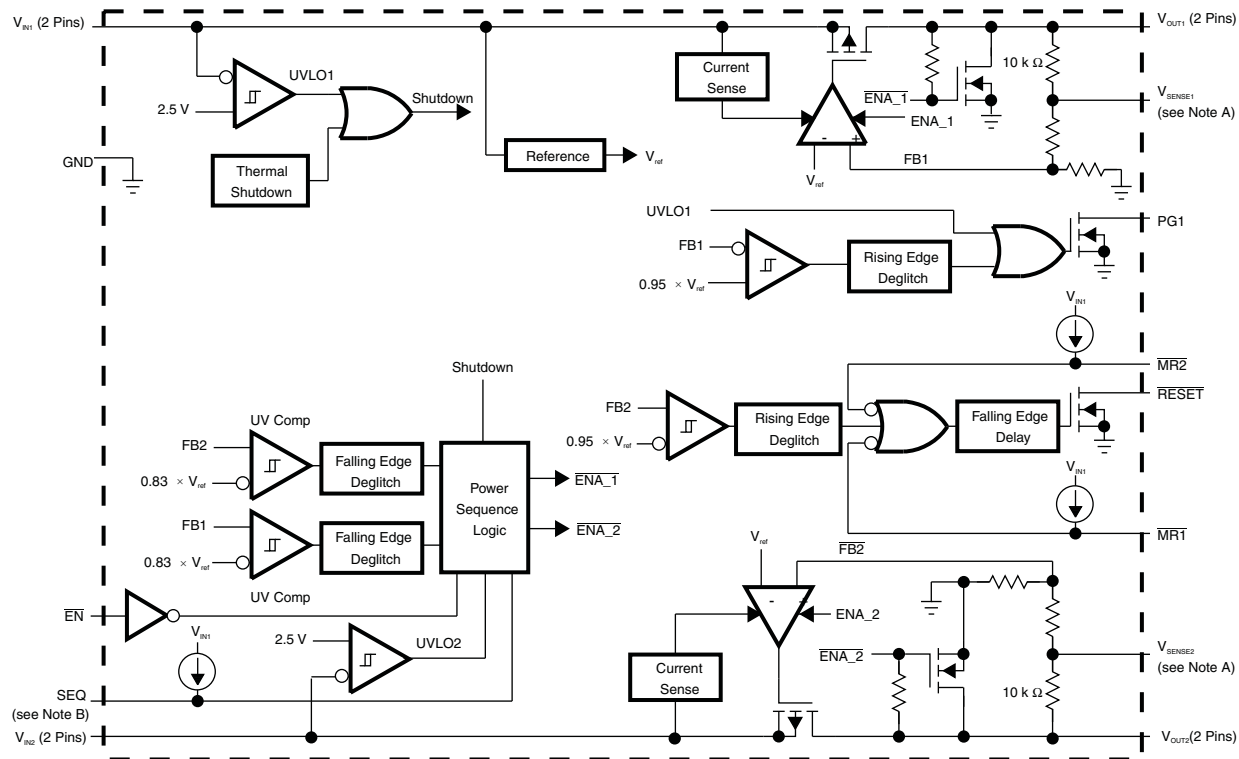
Internal bias voltages are powered by V_{IN1} and require 2.7 V for full functionality. Each regulator input has an undervoltage lockout circuit that prevents each output from turning on until the respective input reaches 2.5 V.

ORDERING INFORMATION⁽¹⁾

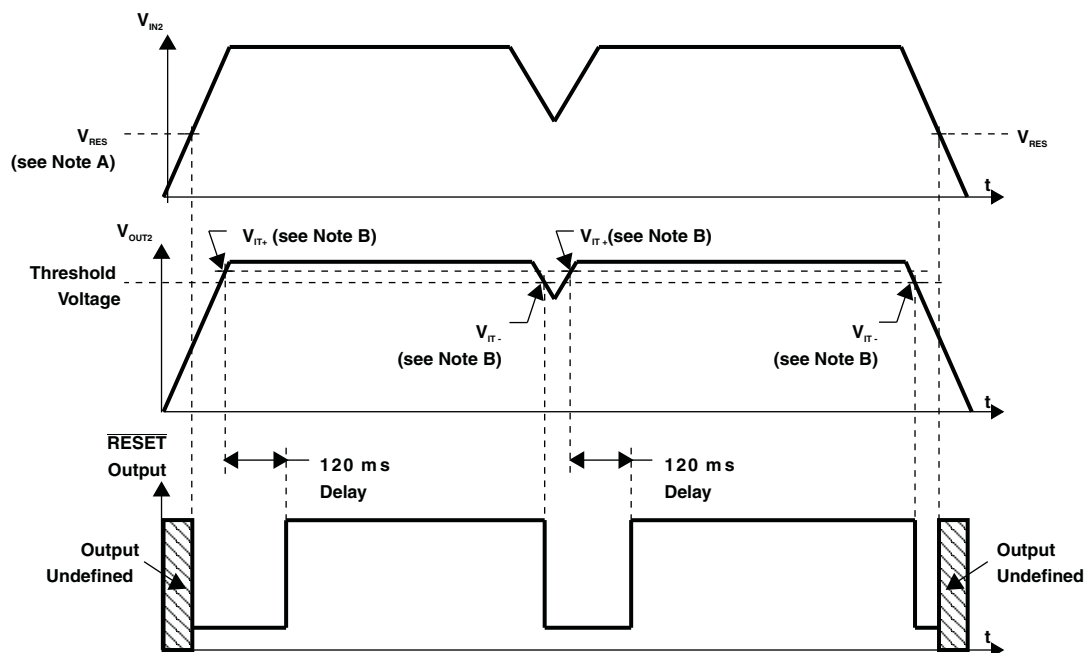
PRODUCT	VOLTAGE (V)		PACKAGE-LEAD (DESIGNATOR)	T _J	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	V _{OUT1}	V _{OUT2}				
TPS70358M	3.3 V	2.5 V	DFP-20 (HKH)	–55°C to 125°C	TPS70358MHKH	TPS70358MHKH

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DETAILED BLOCK DIAGRAM - FIXED VOLTAGE VERSION



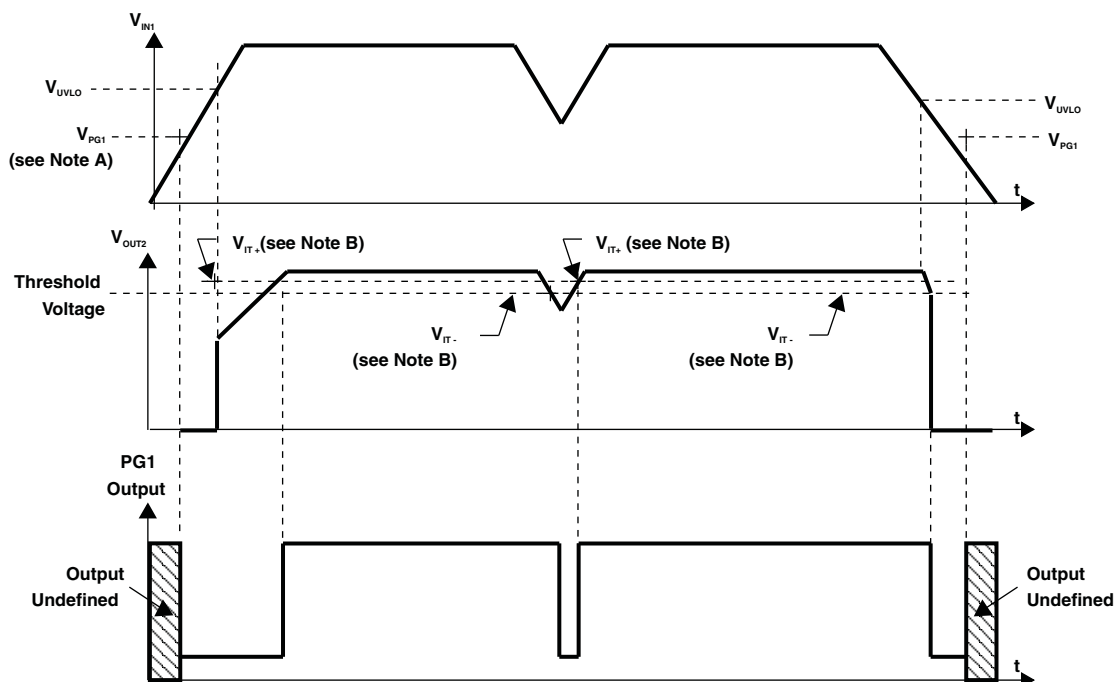
- NOTES: A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT} as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the Application Information section.
B. If the SEQ terminal is floating at the input, V_{OUT2} powers up first.



NOTES: A. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} - Trip voltage is typically 5% lower than the output voltage ($95\%V_O$). V_{IT-} to V_{IT+} is the hysteresis.

Figure 1. RESET Timing Diagram (With V_{IN1} Powered Up and MR1 and MR2 at Logic High)



NOTES: A. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} - Trip voltage is typically 5% lower than the output voltage ($95\%V_O$). V_{IT-} to V_{IT+} is the hysteresis.

Figure 2. PG1 Timing Diagram

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{EN}}$	5	I	Active low enable
GND	7		Regulator ground
$\overline{\text{MR1}}$	4	I	Manual reset input 1, active low, pulled up internally
$\overline{\text{MR2}}$	3	I	Manual reset input 2, active low, pulled up internally
NC	10, 11, 20		No connection
PG1	16	O	Open drain output, low when V_{OUT1} voltage is less than 95% of the nominal regulated voltage
$\overline{\text{RESET}}$	15	O	Open drain output, SVS (power on reset) signal, active low
SEQ	6	I	Power up sequence control: SEQ=High, V_{OUT2} powers up first; SEQ=Low, V_{OUT1} powers up first, SEQ terminal pulled up internally.
V_{IN1}	1, 2	I	Input voltage of regulator 1
V_{IN2}	8, 9	I	Input voltage of regulator 2
V_{OUT1}	18, 19	O	Output voltage of regulator 1
V_{OUT2}	12, 13	O	Output voltage of regulator 2
V_{SENSE2}	14	I	Regulator 2 output voltage sense
V_{SENSE1}	17	I	Regulator 1 output voltage sense

DETAILED DESCRIPTION

The TPS70358 low dropout regulator family provides dual regulated output voltages for DSP applications that require a high performance power management solution. These devices provide fast transient response and high accuracy, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs without any external component requirements. This reduces the component cost and board space while increasing total system reliability. TPS703xx family has an enable feature which puts the device in sleep mode reducing the input current to 1 μA . Other features are the integrated SVS (power on reset, RESET) and power good (PG1). These monitor output voltages and provide logic output to the system. These differentiated features provide a complete DSP power solution.

The TPS703xx, unlike many other LDOs, features very low quiescent current which remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS703xx uses a PMOS transistor to pass current. Because the gate of the PMOS is voltage driven, operating current is low and stable over the full load range.

PIN FUNCTIONS

Enable

The $\overline{\text{EN}}$ terminal is an input which enables or shuts down the device. If $\overline{\text{EN}}$ is at a logic high signal the device is in shutdown mode. When the $\overline{\text{EN}}$ goes to voltage low, then the device is enabled.

Sequence

The SEQ terminal is an input that programs which output voltage (V_{OUT1} or V_{OUT2}) is turned on first. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. If V_{OUT2} is pulled below 83% (i.e., over load condition) V_{OUT1} is turned off. This terminal has a 6- μA pullup current to V_{IN1} .

Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} is turned on first. For detail timing diagrams refer to [Figure 35](#) through [Figure 41](#).

Power Good (PG1)

The PG1 terminal is an open drain, active high output terminal which indicates the status of the V_{OUT1} regulator. When the V_{OUT1} reaches 95% of its regulated voltage, PG1 goes to a high impedance state. PG1 goes to a low impedance state when V_{OUT1} is pulled below 95% (i.e., over load condition) of its regulated voltage. The open drain output of the PG1 terminal requires a pullup resistor.

Manual Reset Pins ($\overline{MR1}$ and $\overline{MR2}$)

$\overline{MR1}$ and $\overline{MR2}$ are active low input terminals used to trigger a reset condition. When either $\overline{MR1}$ or $\overline{MR2}$ is pulled to logic low, a POR ($\overline{RESET}$) occurs. These terminals have a 6- μ A pullup current to V_{IN1} . It is recommended that these pins be pulled high to V_{IN} when they are not used.

Sense (V_{SENSE1} , V_{SENSE2})

The sense terminals of fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, the sense terminals connect to high-impedance wide-bandwidth amplifiers through resistor-divider networks and noise pickup feeds through to the regulator output. It is essential to route the sense connections in such a way to minimize/avoid noise pickup. Adding RC networks between the V_{SENSE} terminals and V_{OUT} terminals to filter noise is not recommended because it can cause the regulators to oscillate.

 $\overline{RESET}$ Indicator

$\overline{RESET}$ is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, $\overline{RESET}$ goes to a high impedance state (i.e. logic high) after a 120-ms delay when all three of the following conditions are met. First, V_{IN1} must be above the undervoltage condition. Second, the manual reset ($\overline{MR}$) pin must be in a high impedance state. Third, V_{OUT2} must be above approximately 95% of its regulated voltage. To monitor V_{OUT1} , the PG1 output pin can be connected to $\overline{MR1}$ or $\overline{MR2}$.

 V_{IN1} and V_{IN2}

V_{IN1} and V_{IN2} are inputs to the regulators.

 V_{OUT1} and V_{OUT2}

V_{OUT1} and V_{OUT2} are output terminals of each regulator.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{IN1} , V_{IN2}	Input voltage range ⁽²⁾	–0.3 to 7	V
	Voltage range at $\overline{EN}$	–0.3 to 7	V
V_{OUT1} , V_{SENSE1} , V_{OUT2} , V_{SENSE2}	Output voltage range	5.5	V
	Maximum $\overline{RESET}$, PG1 voltage	7	V
	Maximum $\overline{MR1}$, $\overline{MR2}$ and SEQ voltage	V_{IN1}	
	Peak output current	Internally limited	
T_J	Operating virtual junction temperature range	–55 to 150	°C
Package thermal impedance	θ_{JC} (die to package top)	17.2	°C/W
	θ_{JC} (die to package bottom)	5.49	
	θ_{JB} (die to standard PCB trace)	38.4	
T_{stg}	Storage temperature range	–65 to 150	°C
	ESD rating (HBM, human body model)	2	kV

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are tied to network ground.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage ⁽¹⁾	2.7		6	V
I_O	Output current	Regulator 1		0	A
		Regulator 2		2	
T_J	Operating virtual storage temperature	–55		125	°C

- (1) To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

ELECTRICAL CHARACTERISTICS

over operating junction temperature range ($T_J = -55^\circ\text{C}$ to 125°C) V_{IN1} or $V_{IN2} = V_{OUTX(nom)} + V$, $I_{OUTX} = 1\text{ mA}$, $\overline{EN} = 0$, $C_{OUT1} = 22\text{ }\mu\text{F}$, $C_{OUT2} = 47\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _O	Output voltage ⁽¹⁾⁽²⁾	2.5 V output (V _{OUT2})		3.5 V < V _I < 6 V, T _J = 25°C		2.5	V
		3.5 V < V _I < 6 V		2.45		2.55	
		3.3 V output (V _{OUT1})		4.3 V < V _I < 6 V, T _J = 25°C		3.3	
		4.3 V < V _I < 6 V		3.234		3.366	
Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{\text{EN}}$ = 0 V ⁽²⁾⁽¹⁾		T _J = 25°C		185		μA	
				250			
Load regulation for V _{OUT1} and V _{OUT2} ⁽³⁾		T _J = 25°C		1		mV	
Ouput voltage line regulation for regulator 1 and regulator 2 ⁽¹⁾		V _O + 1 V < V _I < 6 V, T _J = 25°C		0.01%		mV	
		Regulator 1	V _O + 1 V < V _I < 6 V,		5.6		
		Regulator 2			6.25		

- (1) Minimum input operating voltage is 2.7 V or $V_{O(typ)} + 1\text{ V}$, whichever is greater. Maximum input voltage = 6 V , minimum output current is 1 mA .
- (2) Input voltage (V_{IN1} or V_{IN2}) = $V_{O(Typ)} - 100\text{ mV}$. For the 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3-V regulator input voltage is set to 3.2 V to perform this test.
- (3) $I_O = 1\text{ mA}$ to 1 A for regulator 1 and 1 mA to 2 A for regulator 2.

ELECTRICAL CHARACTERISTICS (continued)

over operating junction temperature range ($T_J = -55^\circ\text{C}$ to 125°C) V_{IN1} or $V_{IN2} = V_{OUTX(nom)} + V$, $I_{OUTX} = 1\text{ mA}$, $\overline{EN} = 0$, $C_{OUT1} = 22\text{ }\mu\text{F}$, $C_{OUT2} = 47\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ouput current limit	Regulator 1	V _O = 0 V	1.75		2.2	A
	Regulator 2		3.8		4.5	
Thermal shutdown junction temperature			150			°C
I _{I(standby)} Standby current	EN = V _I , T _J = 25°C		1		2	μA
	EN = V _I				10	
RESET TERMINAL						
Minimum input voltage for valid RESET		I _(RESET) = 300 μA, V _(RESET) ≤ 0.8 V	1		1.45	V
Trip threshold voltage		V _O decreasing	92%	95%	98%	V _O
Hysteresis voltage		Measured at V _O	0.5%			V _O
t _(RESET) ⁽⁴⁾		RESET pulse duration T _J = 25°C	80	120	160	ms
t _{r(RESET)} ⁽⁴⁾		Rising edge deglitch	30			μs
Output low voltage		V _I = 3.5 V, I _(RESET) = 1 mA	0.15		0.4	V
Leakage current		V _(RESET) = 6 V			1	μA
PG TERMINAL						
Minimum input voltage for valid PG		I _(PG) = 300 μA, V _(PG1) ≤ 0.8 V	1		1.45	V
Trip threshold voltage		V _O decreasing	92%	95%	98%	V _O
Hysteresis voltage		Measured at V _O	0.5%			V _O
t _{r(PG1)}		Rising edge deglitch	30			μs
Output low voltage		V _I = 2.7 V, I _(PG) = 1 mA	0.15		0.4	V
Leakage current		V _(PG1) = 6 V			1	μA
EN TERMINAL						
High-level EN input voltage			2			V
Low-level EN input voltage					0.7	V
Input current (EN)			-1		1	μA
SEQ TERMINAL						
High-level SEQ input voltage			2			V
Low-level SEQ input voltage					0.7	V
SEQ pullup current source			6			μA
MR1 / MR2 TERMINAL						
High-level input voltage			2			V
Low-level input voltage					0.7	V
Pullup current source			6			μA
V _{OUT2} TERMINAL						
V _{OUT2} UV comparator - positive-going input threshold voltage of V _{OUT2} UV comparator			80% V _O	83% V _O	86% V _O	V
V _{OUT2} UV comparator - hysteresis			3% V _O			mV
V _{OUT2} UV comparator - falling edge deglitch ⁽⁴⁾		V _{SENSE2} decreasing below threshold	140			μs
Peak output current		2-ms pulse width	3			A
Discharge transistor current		V _{OUT2} = 1.5 V	7.5			mA
V _{OUT1} TERMINAL						
V _{OUT1} UV comparator - positive-going input threshold voltage of V _{OUT1} UV comparator			80% V _O	83% V _O	86% V _O	V
V _{OUT1} UV comparator - hysteresis			3% V _O			mV
V _{OUT1} UV comparator - falling edge deglitch		V _{SENSE1} decreasing below threshold	140			μs

(4) Not production tested. Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

over operating junction temperature range ($T_J = -55^{\circ}\text{C}$ to 125°C) V_{IN1} or $V_{IN2} = V_{OUTX(nom)} + V$, $I_{OUTX} = 1\text{ mA}$, $\overline{EN} = 0$, $C_{OUT1} = 22\text{ }\mu\text{F}$, $C_{OUT2} = 47\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout voltage ⁽⁵⁾	$I_O = 1\text{ A}$, $V_{IN1} = 3.2\text{ V}$, $T_J = 25^{\circ}\text{C}$		160		mV
	$I_O = 1\text{ A}$, $V_{IN1} = 3.2\text{ V}$			400	
Peak output current	2-ms pulse width		1.2		A
Discharge transistor current	$V_{OUT1} = 1.5\text{ V}$		7.5		mA
VIN1 / VIN2 TERMINAL					
UVLO threshold		2.3		2.65	V
UVLO hysteresis			110		mV

(5) Input voltage(V_{IN1} or V_{IN2}) = $V_O(\text{Typ}) - 100\text{ mV}$. For the 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3-V regulator input voltage is set to 3.2 V to perform this test.

TYPICAL CHARACTERISTICS

Table 1. TPS70358M

PRODUCT	VOLTAGE (V)		PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE (T _J)	ORDERING NUMBER	TOP-SIDE MARKING
	V _{OUT1}	V _{OUT2}				
TPS70358M	3.3 V	2.5 V	DFP-20 (HKH)	–55°C to 125°C	TPS70358MHKH	TPS70358MHKH

Table 2. Table of Graphs

			FIGURE
V _O	Output voltage	vs Output current	Figure 3, Figure 4
		vs Junction temperature	Figure 5, Figure 6
	Ground current	vs Junction temperature	Figure 7
PSRR	Power supply rejection ratio	vs Frequency	Figure 8 - Figure 11
	Output spectral noise density	vs Frequency	Figure 12 - Figure 15
Z _O	Output impedance	vs Frequency	Figure 16 - Figure 19
	Dropout voltage	vs Temperature	Figure 20, Figure 21
		vs Input voltage	Figure 22, Figure 23
	Load transient response		Figure 24, Figure 25
	Line transient response		Figure 26, Figure 27
V _O	Output voltage and enable voltage	vs Time (start-up)	Figure 28, Figure 29
	Equivalent series resistance	vs Output current	Figure 31 - Figure 34

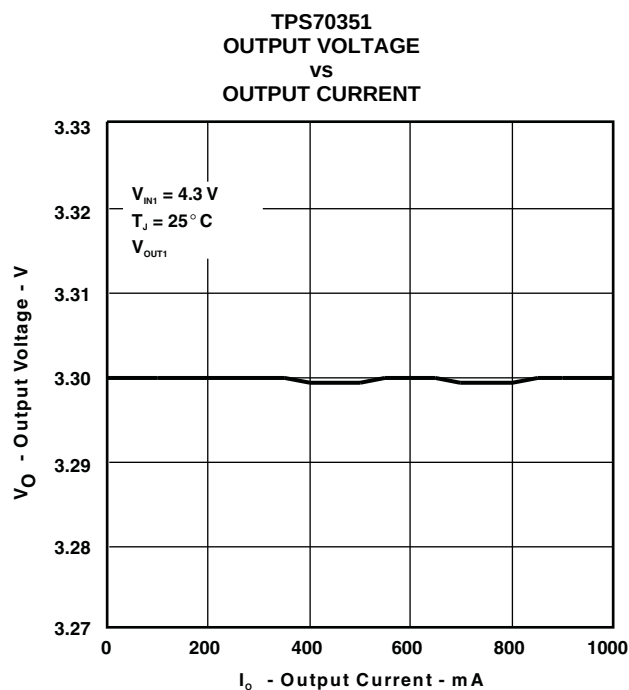


Figure 3.

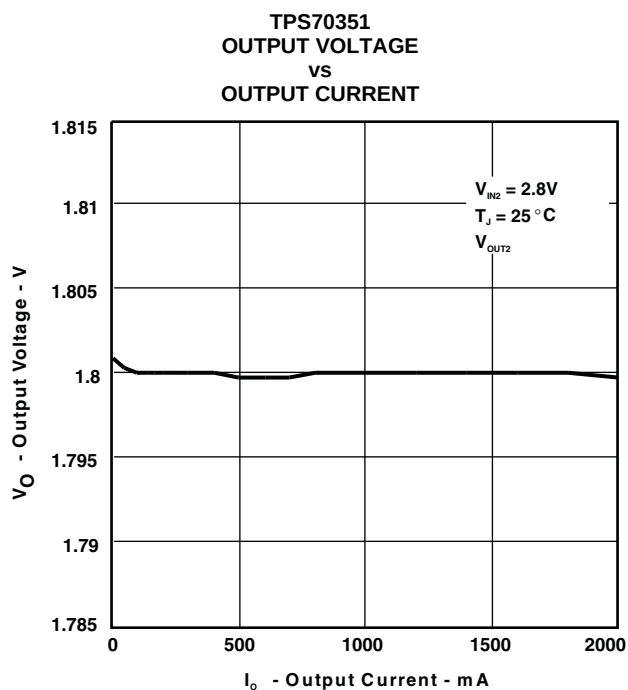


Figure 4.

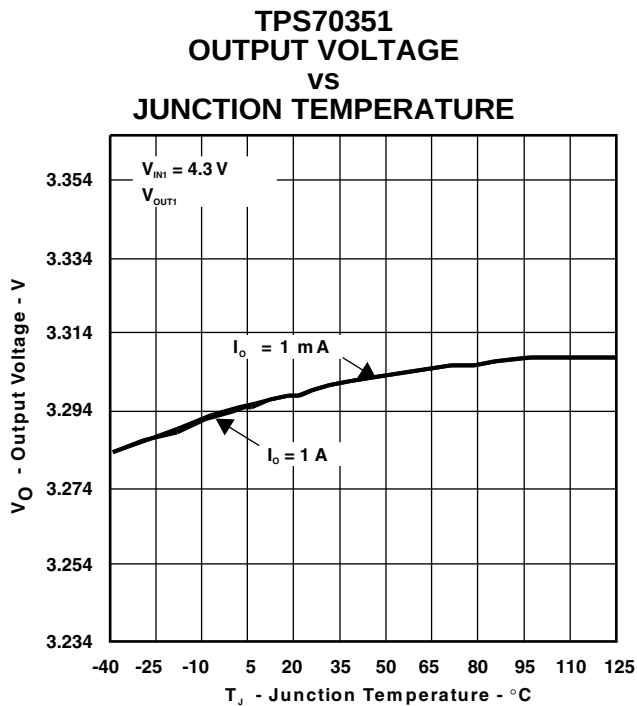


Figure 5.

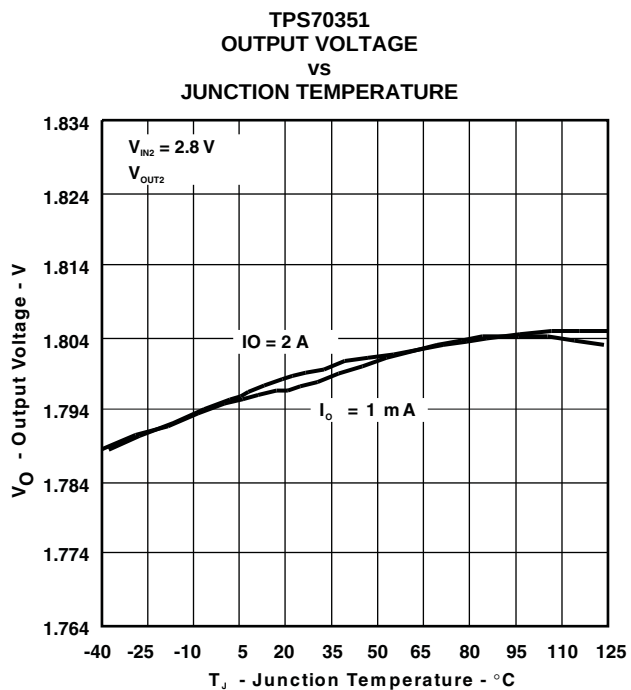


Figure 6.

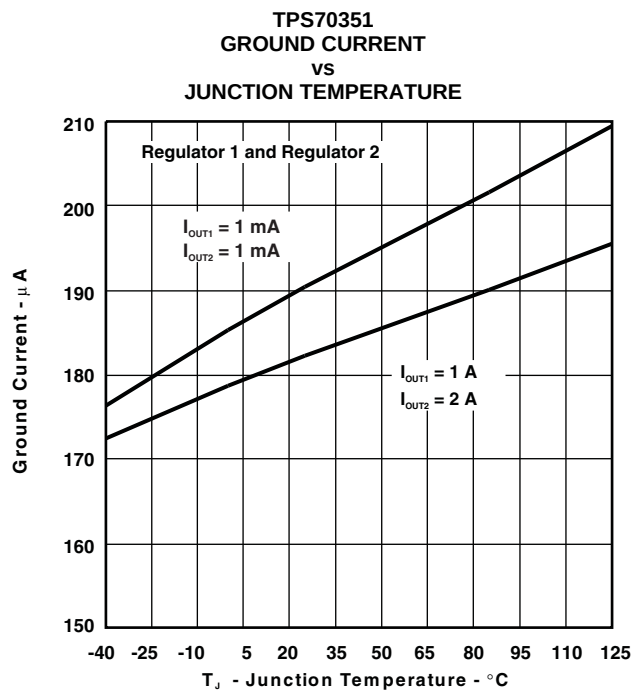


Figure 7.

TPS70351 OUTPUT VOLTAGE VS JUNCTION TEMPERATURE (continued)

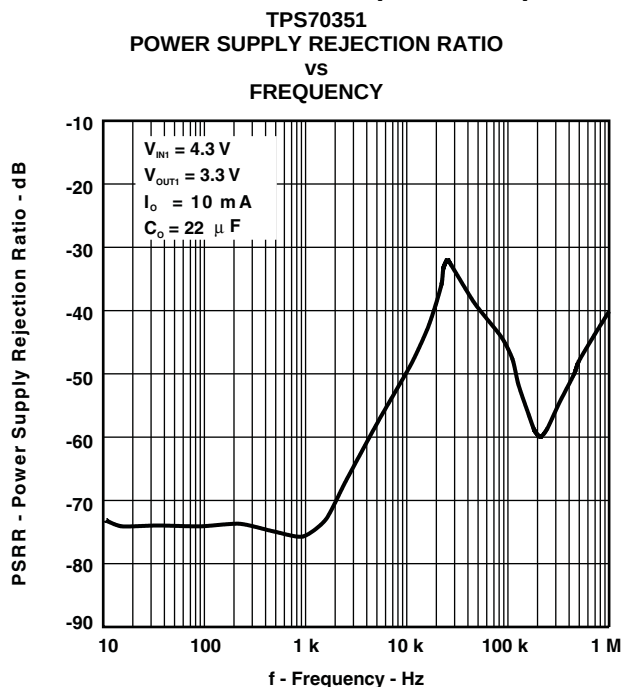


Figure 8.

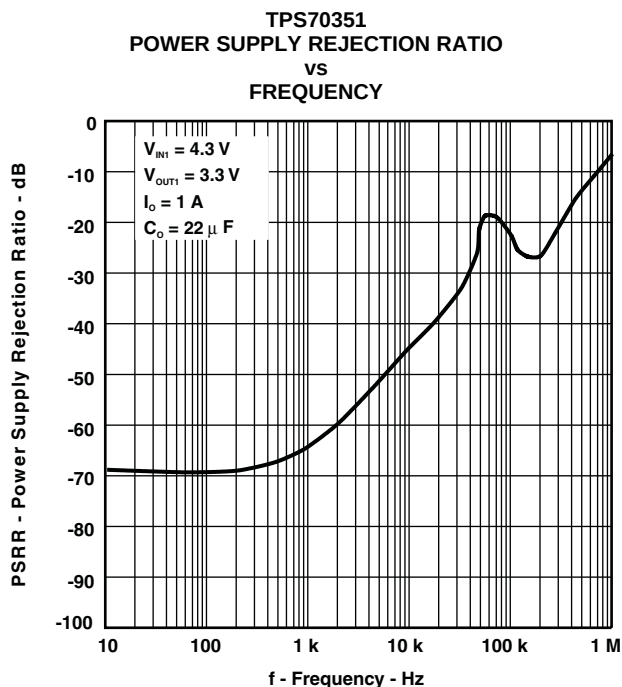


Figure 9.

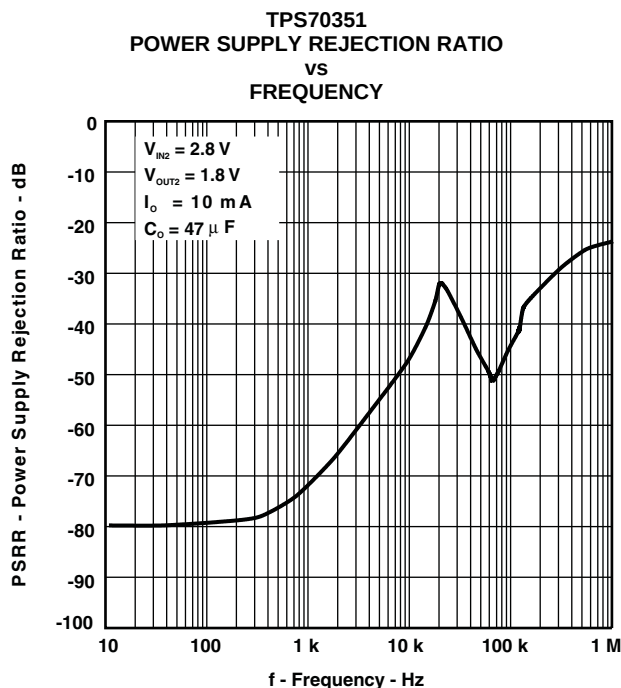


Figure 10.

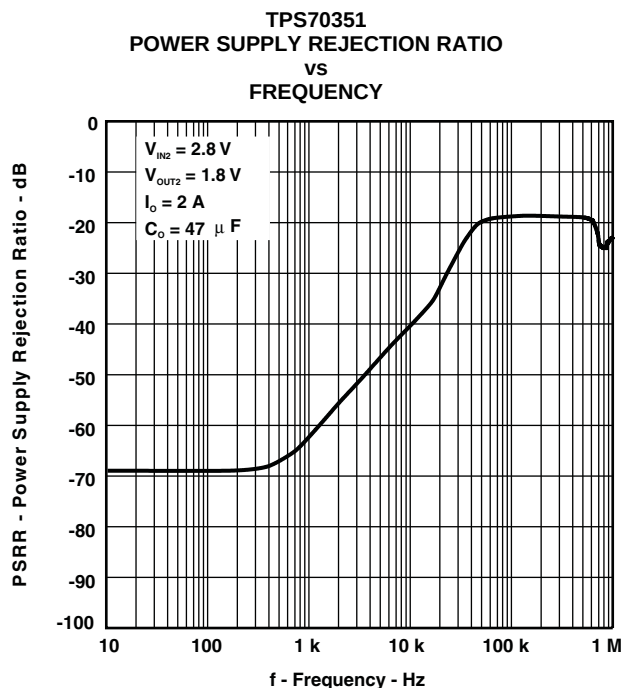


Figure 11.

TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)

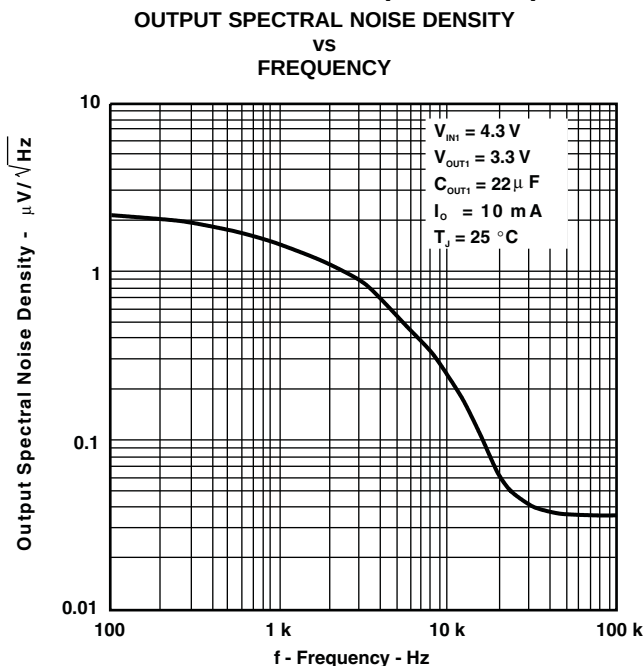


Figure 12.

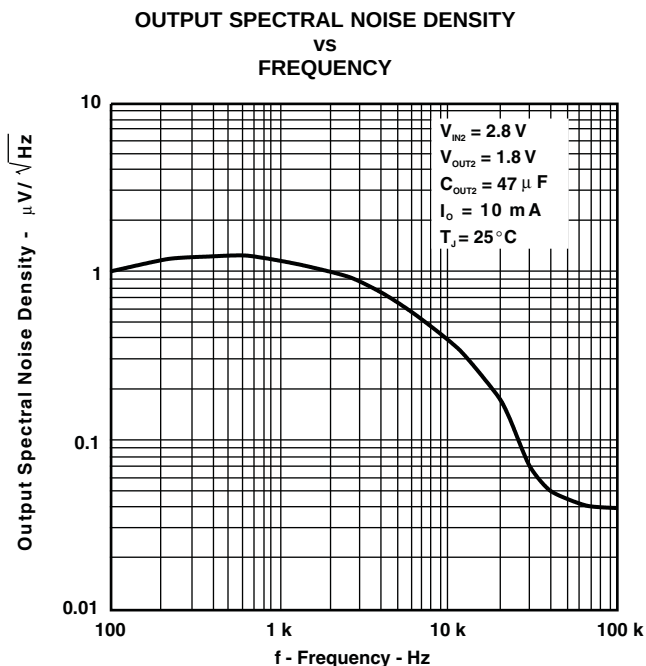


Figure 13.

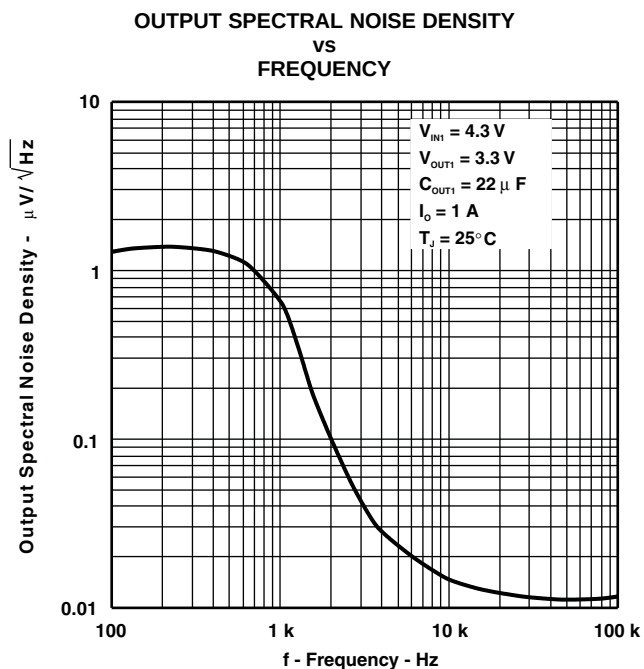


Figure 14.

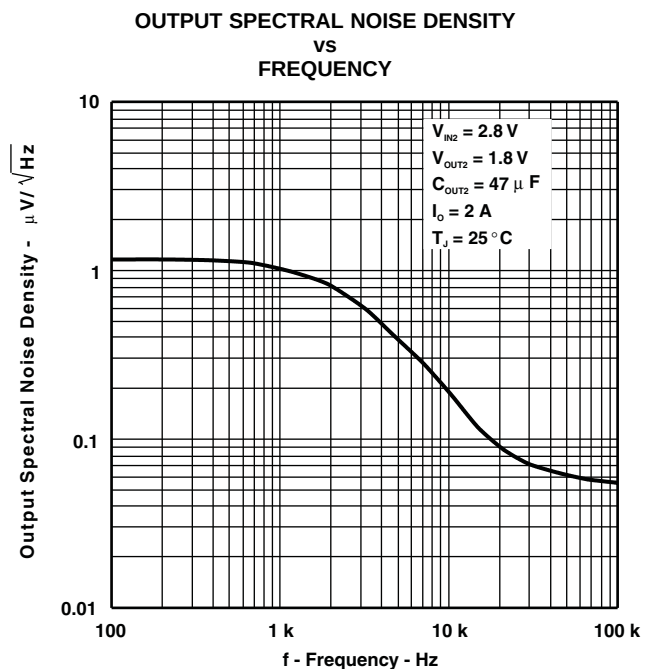


Figure 15.

TPS70351 OUTPUT VOLTAGE VS JUNCTION TEMPERATURE (continued)

OUTPUT IMPEDANCE
VS
FREQUENCY

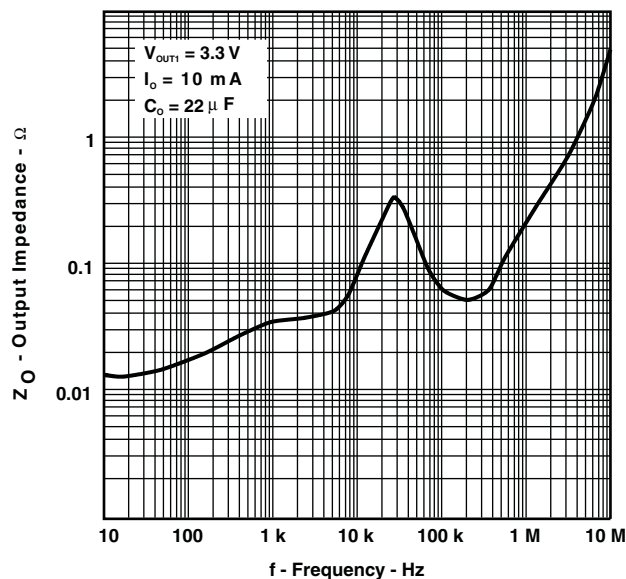


Figure 16.

OUTPUT IMPEDANCE
VS
FREQUENCY

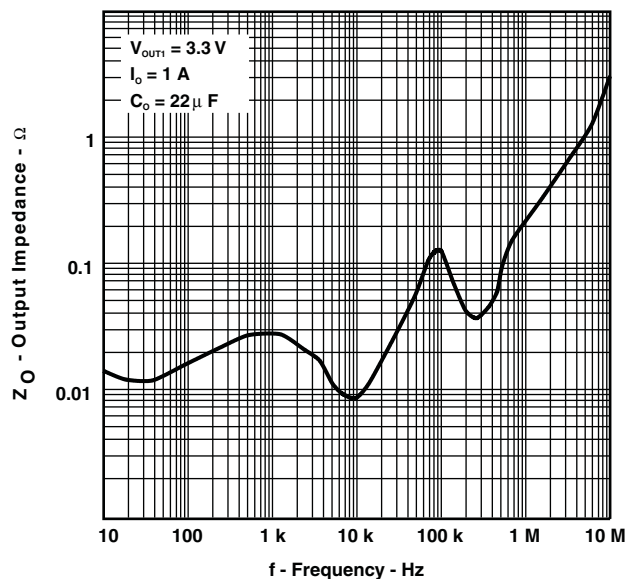


Figure 17.

OUTPUT IMPEDANCE
VS
FREQUENCY

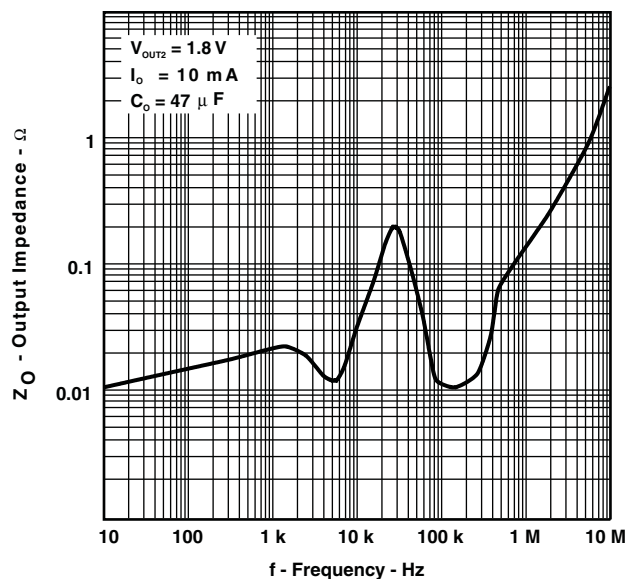


Figure 18.

OUTPUT IMPEDANCE
VS
FREQUENCY

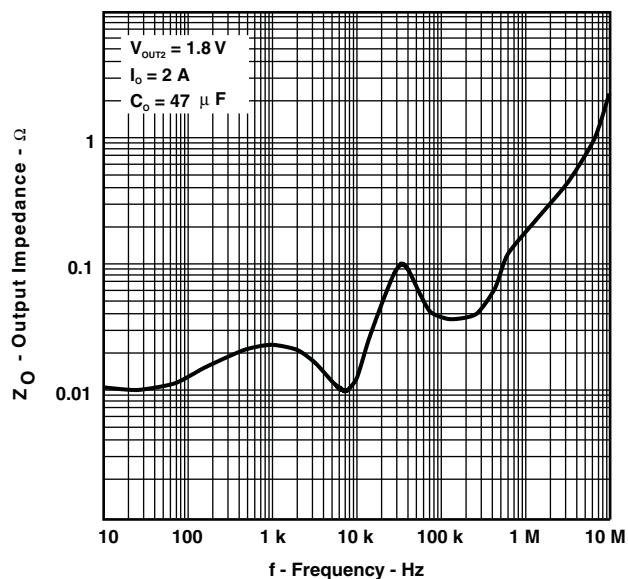


Figure 19.

**TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)**

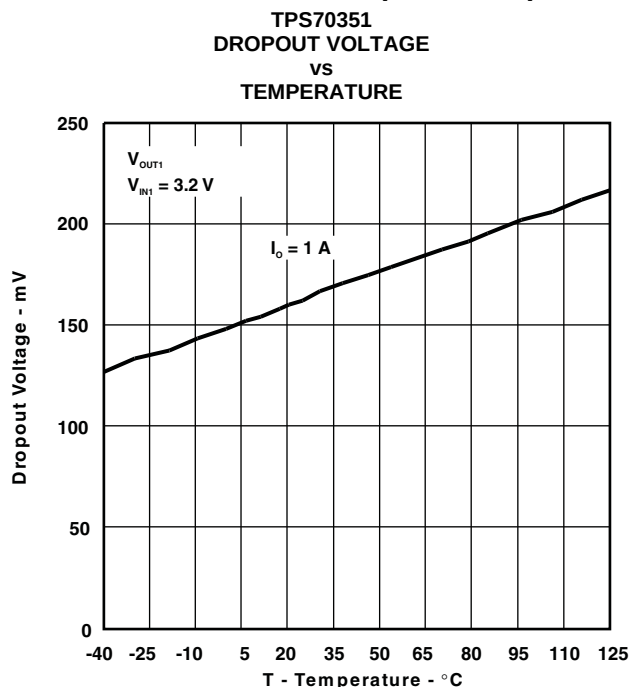


Figure 20.

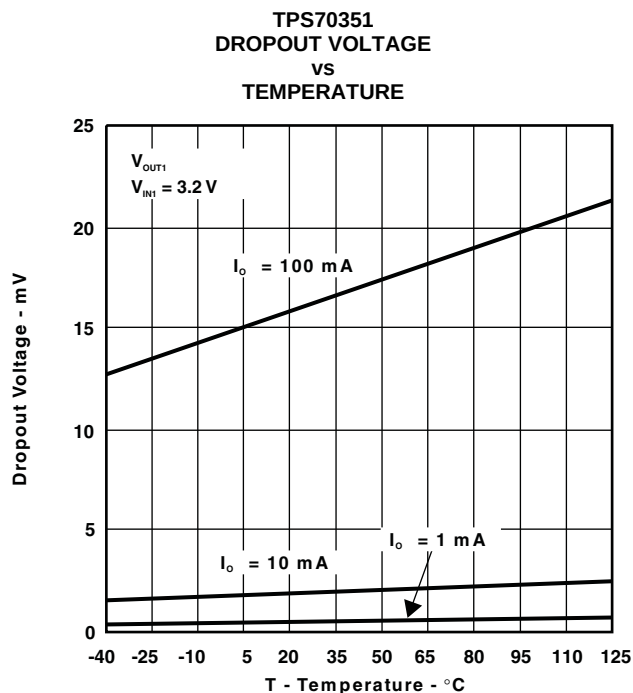


Figure 21.

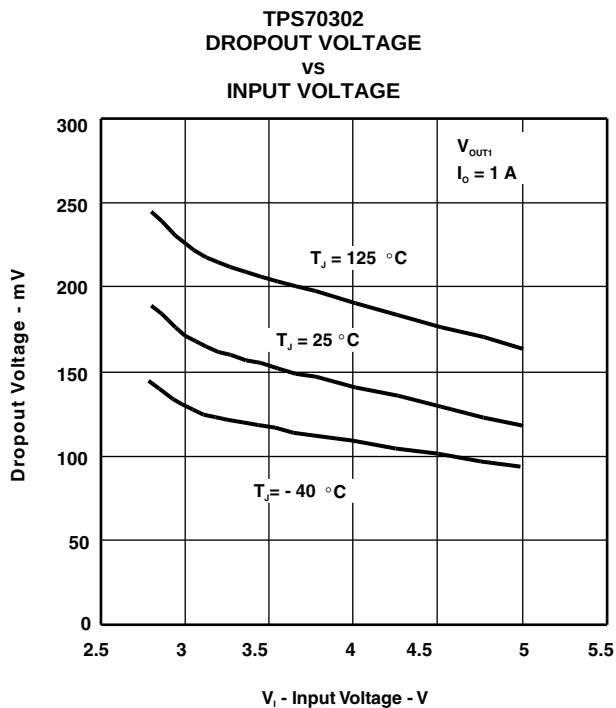


Figure 22.

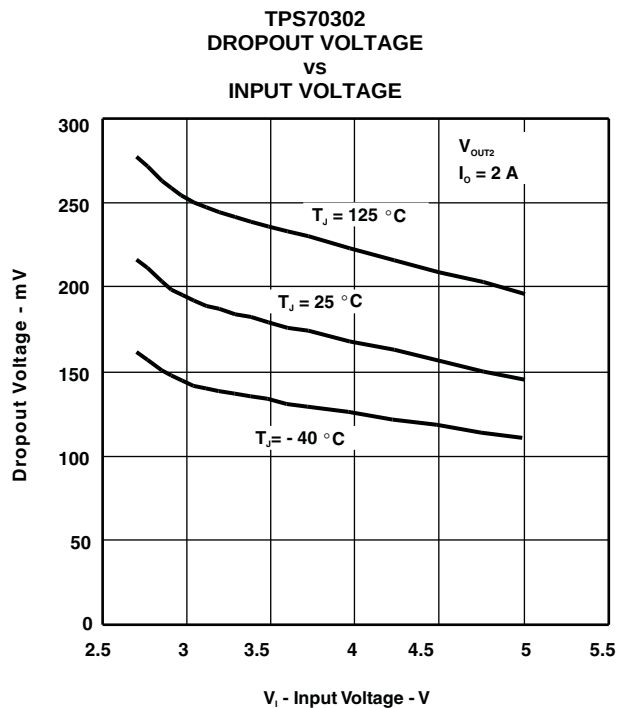


Figure 23.

TPS70351 OUTPUT VOLTAGE VS JUNCTION TEMPERATURE (continued)

LOAD TRANSIENT RESPONSE

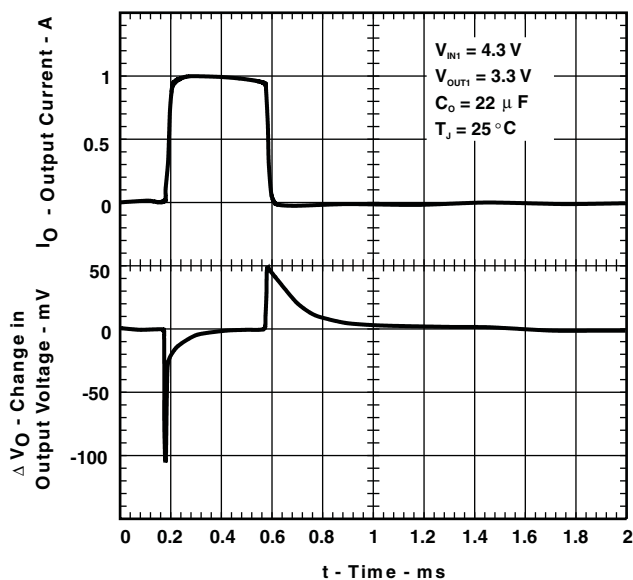


Figure 24.

LOAD TRANSIENT RESPONSE

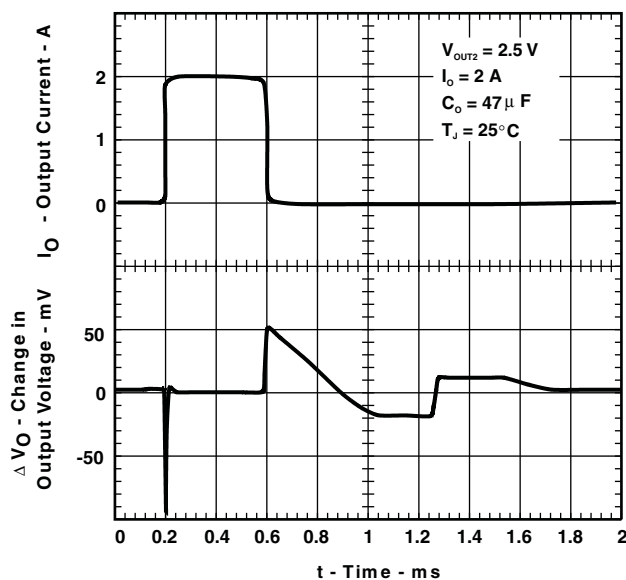


Figure 25.

LINE TRANSIENT RESPONSE

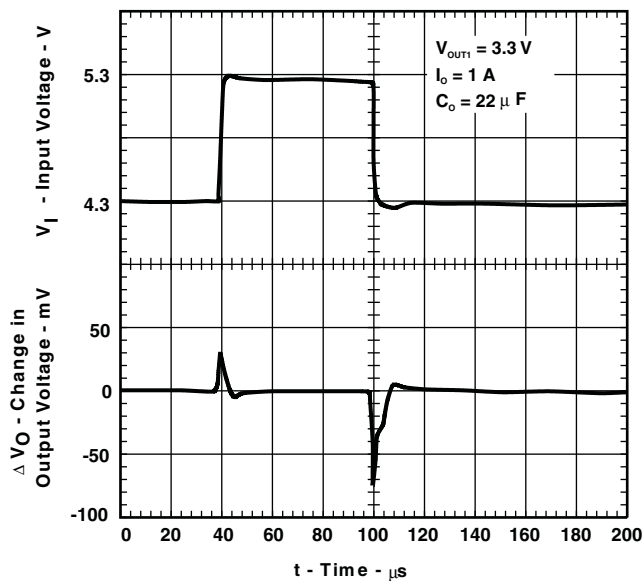


Figure 26.

LINE TRANSIENT RESPONSE

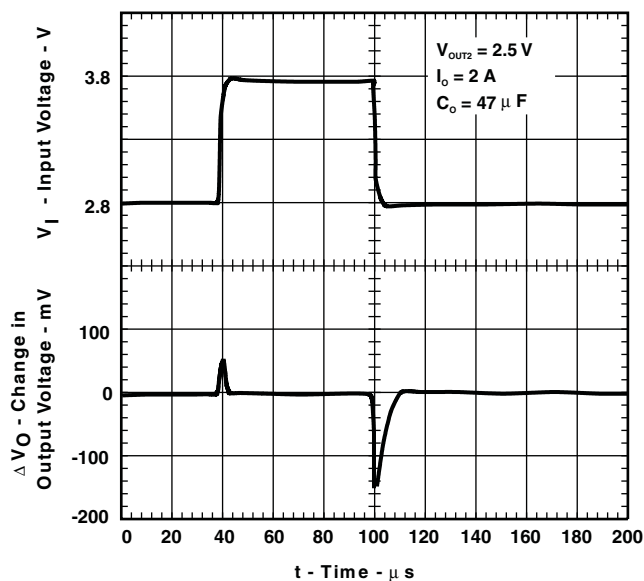


Figure 27.

TPS70351 OUTPUT VOLTAGE VS JUNCTION TEMPERATURE (continued)

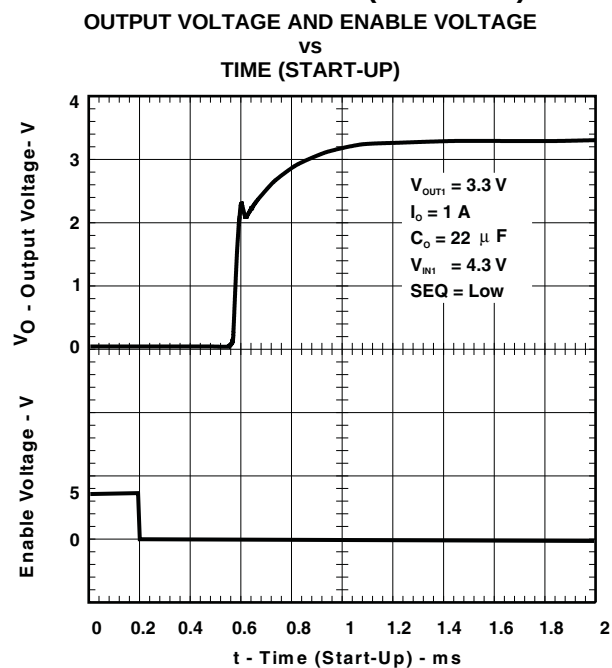


Figure 28.

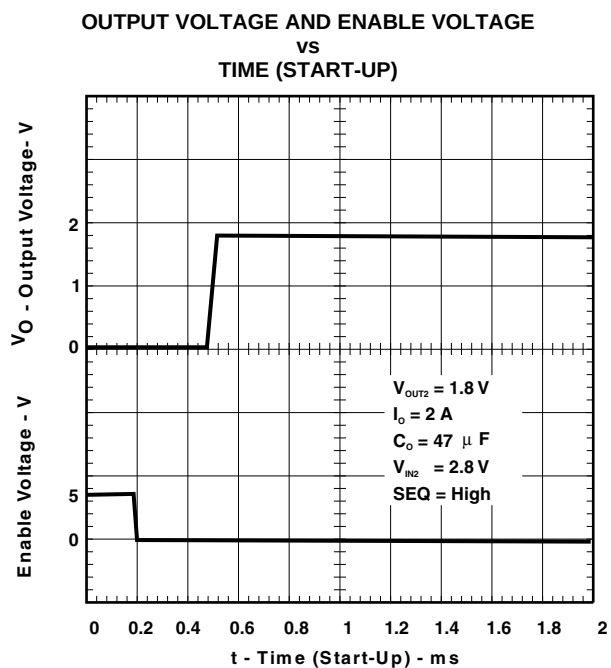


Figure 29.

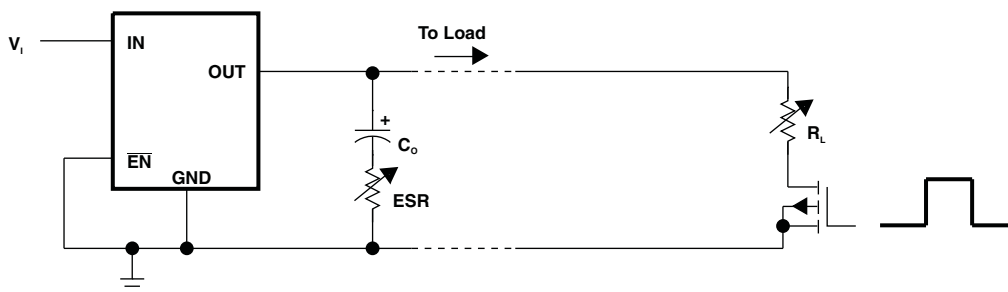


Figure 30. Test Circuit for Typical Regions of Stability

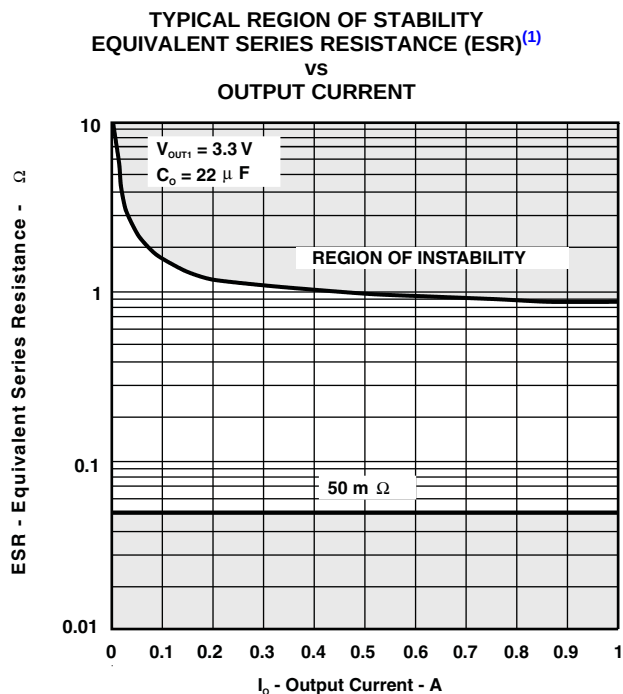


Figure 31.

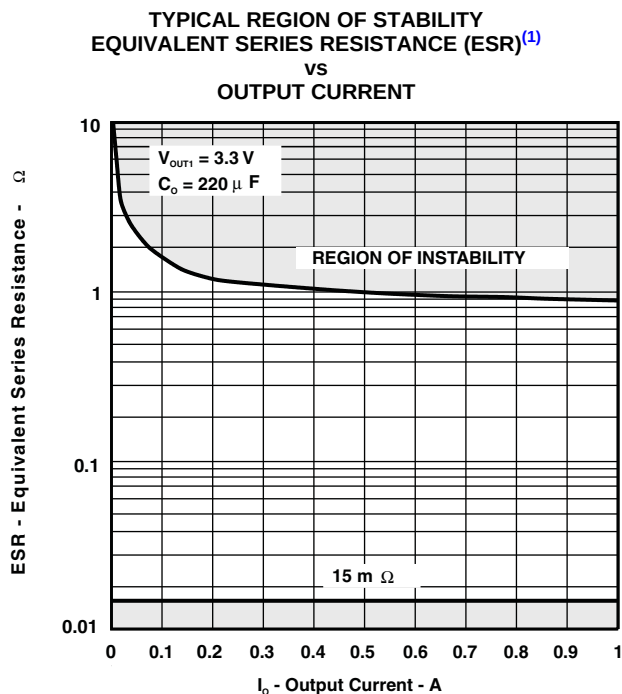


Figure 32.

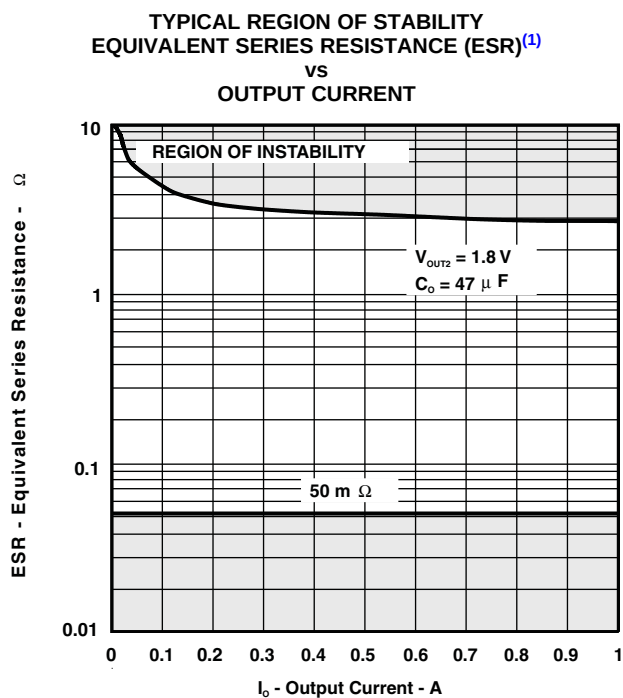


Figure 33.

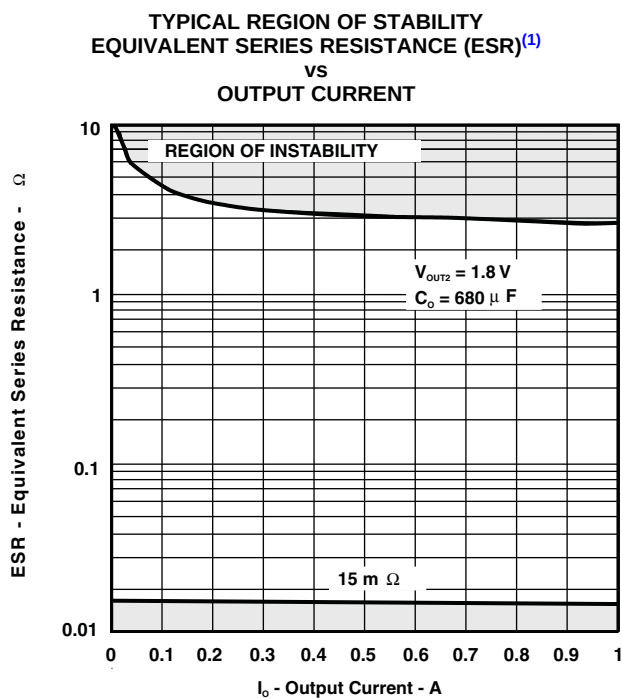


Figure 34.

APPLICATION INFORMATION

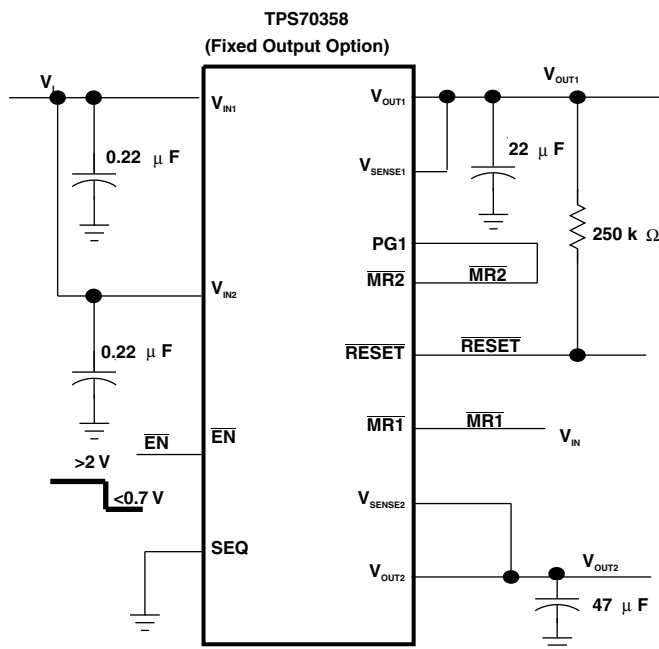
Sequencing Timing Diagrams

The following figures provide a timing diagram of how this device functions in different configurations.

SEQ = Low

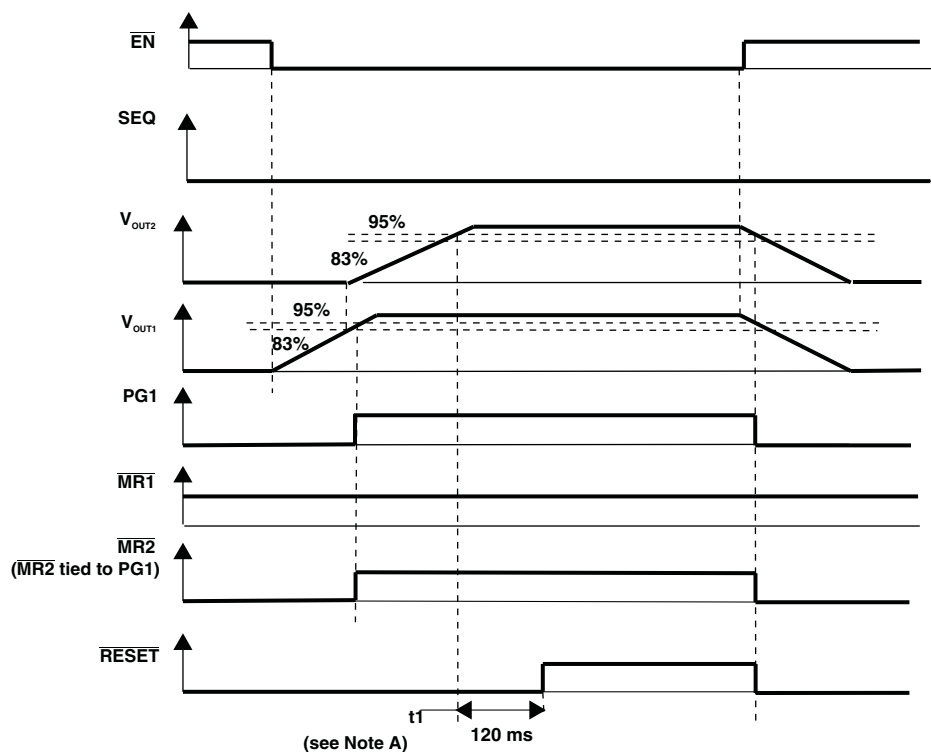
Application Conditions Not Shown in Block Diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO} ; SEQ is tied to logic low; PG1 is tied to MR2; MR1 is not used and is connected to V_{IN} .



Explanation of Timing Diagram:

$\overline{EN}$ is initially high; therefore, both regulators are off and $PG1$ and $\overline{RESET}$ are at logic low. With SEQ at logic low, when EN is taken to logic low, V_{OUT1} turns on. V_{OUT2} turns on after V_{OUT1} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, $PG1$ (tied to $MR2$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $MR1$ and $MR2$ (tied to $PG1$) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay. When $\overline{EN}$ is returned to logic high, both devices power down and both $PG1$ (tied to $MR2$) and $\overline{RESET}$ return to logic low.



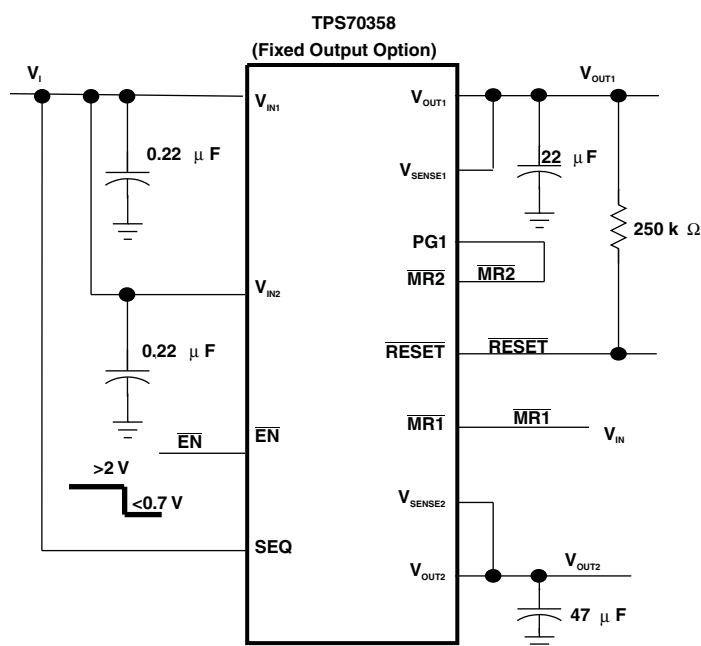
NOTE A: t_1 - Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and MR1 is logic high.

Figure 35. Timing When SEQ = Low

SEQ = High

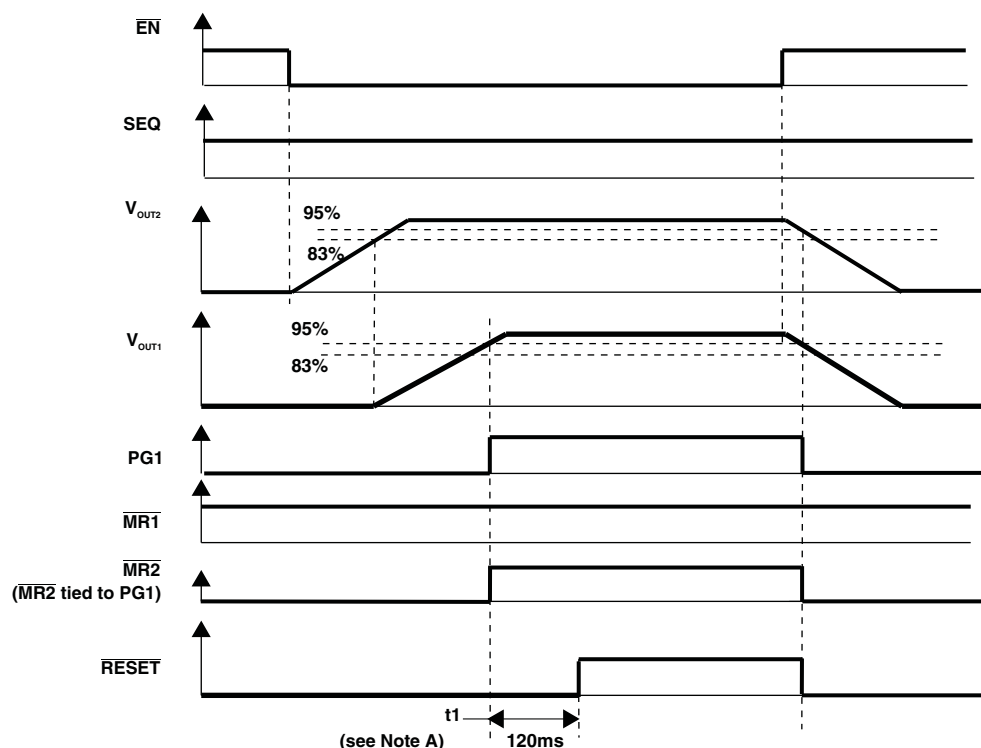
Application Conditions Not Shown in Block Diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to MR2; MR1 is not used and is connected to V_{IN}.



Explanation of Timing Diagram:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken to logic low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both MR1 and MR2 (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay. When $\overline{EN}$ is returned to logic high, both devices turn off and both PG1 (tied to MR2) and $\overline{RESET}$ return to logic low.



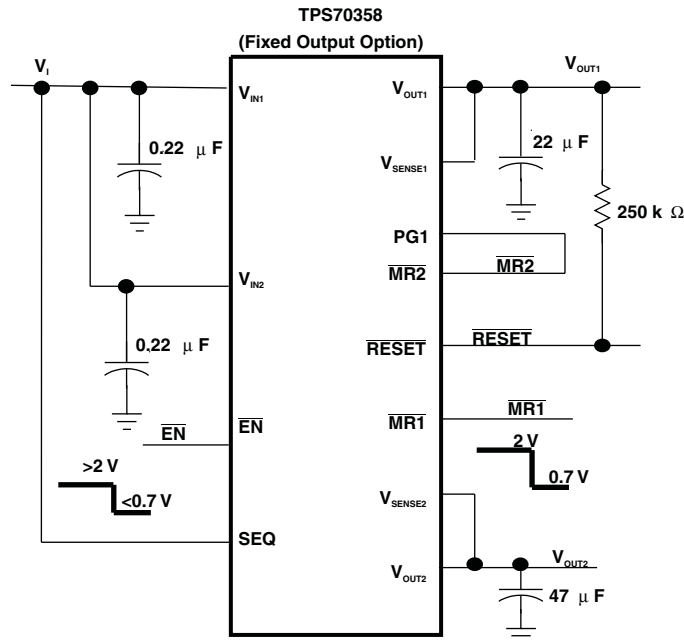
NOTE A: t_1 - Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 36. Timing When SEQ = High

Toggled $\overline{\text{MR1}}$

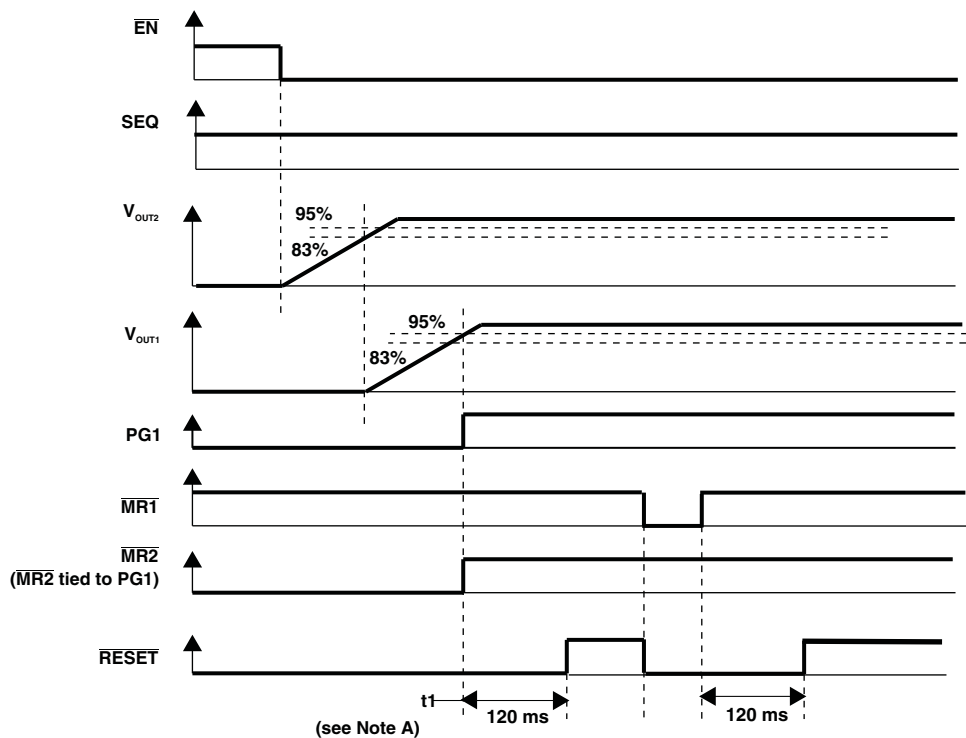
Application Conditions Not Shown in Block Diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO} ; SEQ is tied to logic high; PG1 is tied to MR2; MR1 is initially at logic high but is eventually toggled.



Explanation of Timing Diagram:

$\overline{\text{EN}}$ is initially high; therefore, both regulators are off and PG1 and $\overline{\text{RESET}}$ are at logic low. With SEQ at logic high, when EN is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ (tied to PG1) are at logic high, $\overline{\text{RESET}}$ is pulled to logic high after a 120-ms delay. When $\overline{\text{MR1}}$ is taken low, $\overline{\text{RESET}}$ returns to logic low but the outputs remain in regulation. When $\overline{\text{MR1}}$ is returned to logic high, since both V_{OUT1} and V_{OUT2} remain above 95% of their respective regulated output voltages and $\overline{\text{MR2}}$ (tied to PG1) remains at logic high, $\overline{\text{RESET}}$ is pulled to logic high after a 120-ms delay.



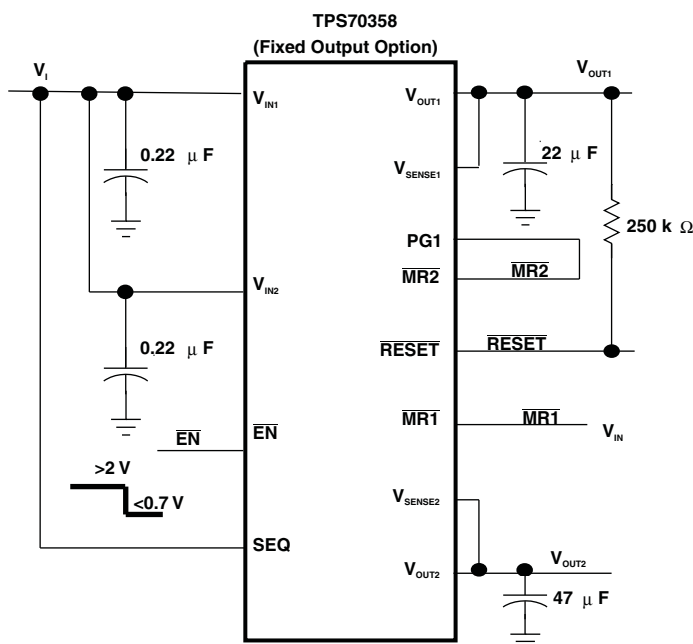
NOTE A: t₁ - Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and MR1 is logic high.

Figure 37. Timing When MR1 is Toggled

V_{OUT1} FAULT

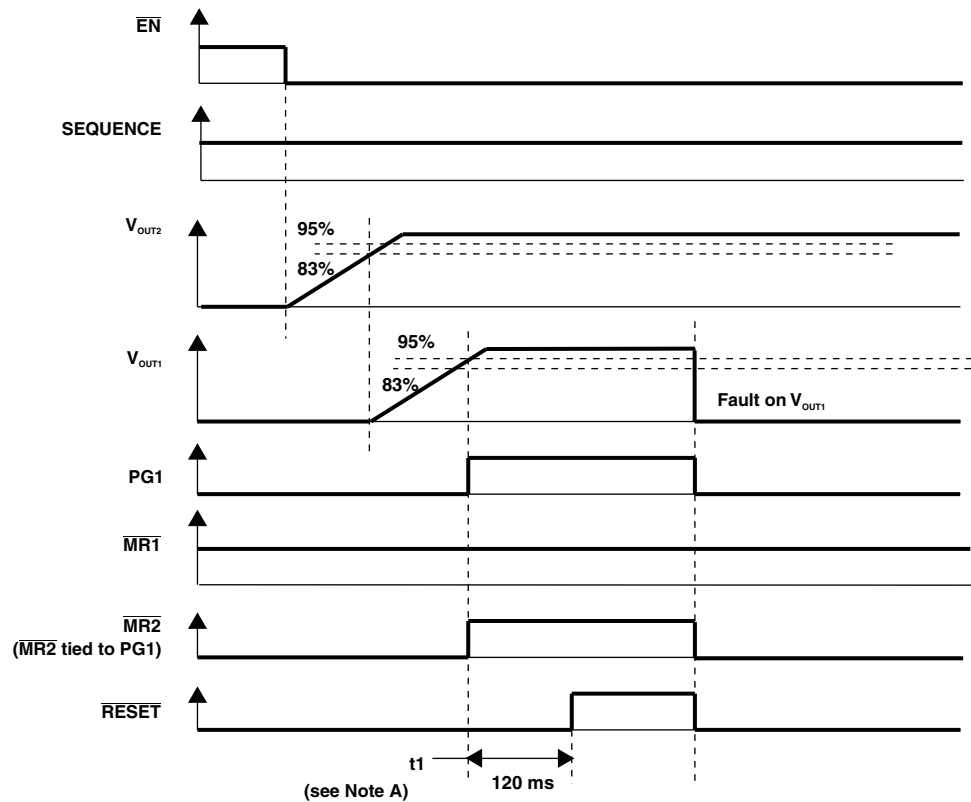
Application Conditions Not Shown in Block Diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to MR2; MR1 is not used and is connected to V_{IN}.



Explanation of Timing Diagram:

$\overline{\text{EN}}$ is initially high; therefore, both regulators are off and PG1 and $\overline{\text{RESET}}$ are at logic low. With SEQ at logic high, when $\overline{\text{EN}}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both MR1 and MR2 (tied to PG1) are at logic high, $\overline{\text{RESET}}$ is pulled to logic high after a 120-ms delay. When a fault on V_{OUT1} causes it to fall below 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic low.



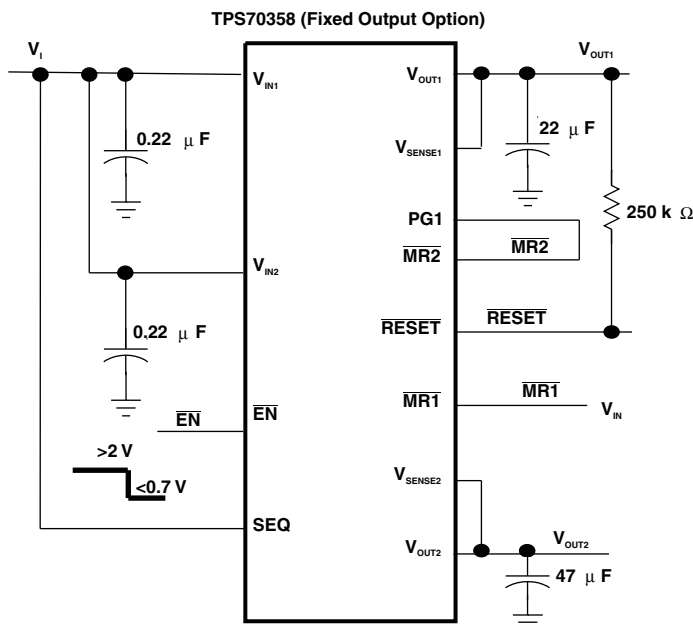
NOTE A: t_1 - Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{\text{MR1}}$ is logic high.

Figure 38. Timing When a Fault Occurs on V_{OUT1}

V_{OUT2} FAULT

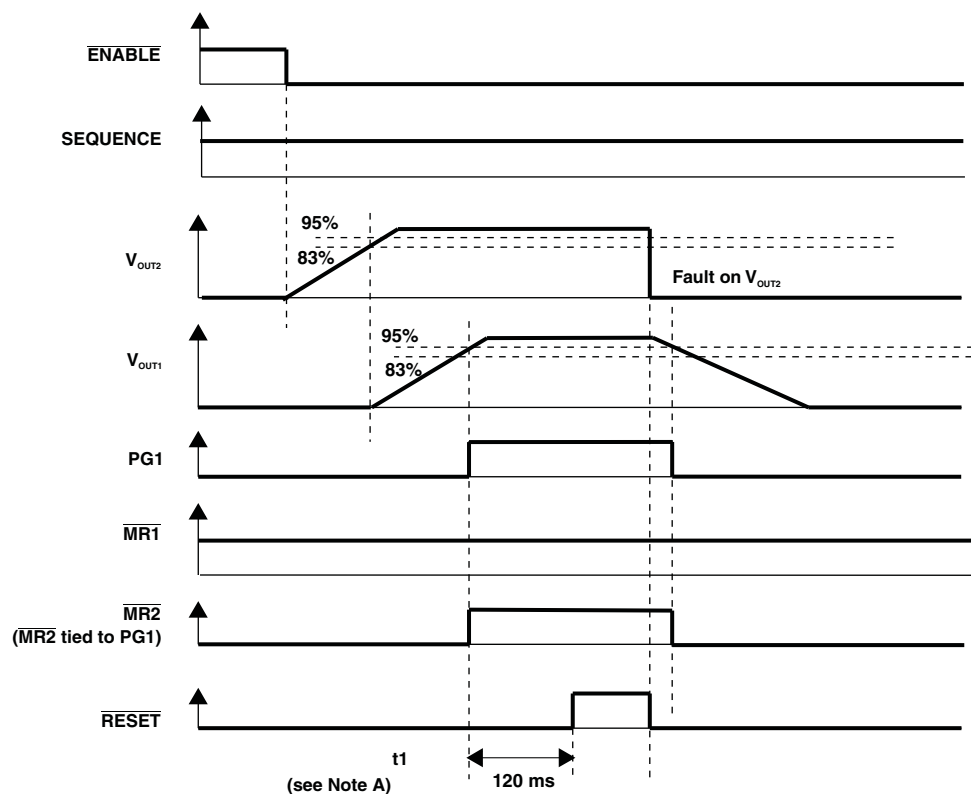
Application Conditions Not Shown in Block Diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to MR2; MR1 is not used and is connected to V_{IN}.



Explanation of Timing Diagram:

EN is initially high; therefore, both regulators are off and PG1 and RESET are at logic low. With SEQ at logic high, when EN is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both MR1 and MR2 (tied to PG1) are at logic high, RESET is pulled to logic high after a 120-ms delay. When a fault on V_{OUT2} causes it to fall below 95% of its regulated output voltage, RESET returns to logic low and V_{OUT1} begins to power down because SEQ is high. When V_{OUT1} falls below 95% of its regulated output voltage, PG1 (tied to MR2) returns to logic low.

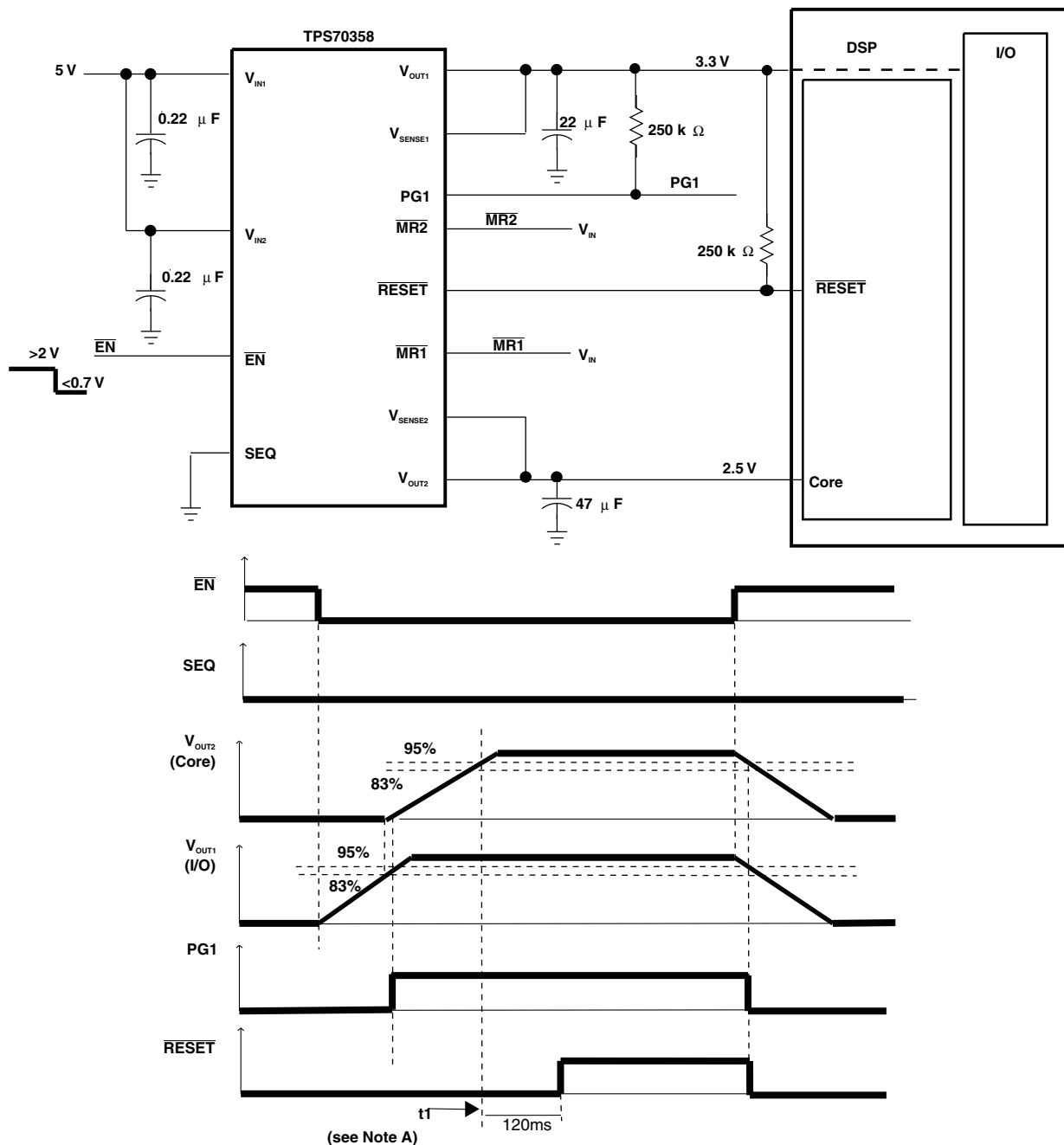


NOTE A: t1 - Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 39. Timing When a Fault Occurs on V_{OUT2}

Split Voltage DSP Application

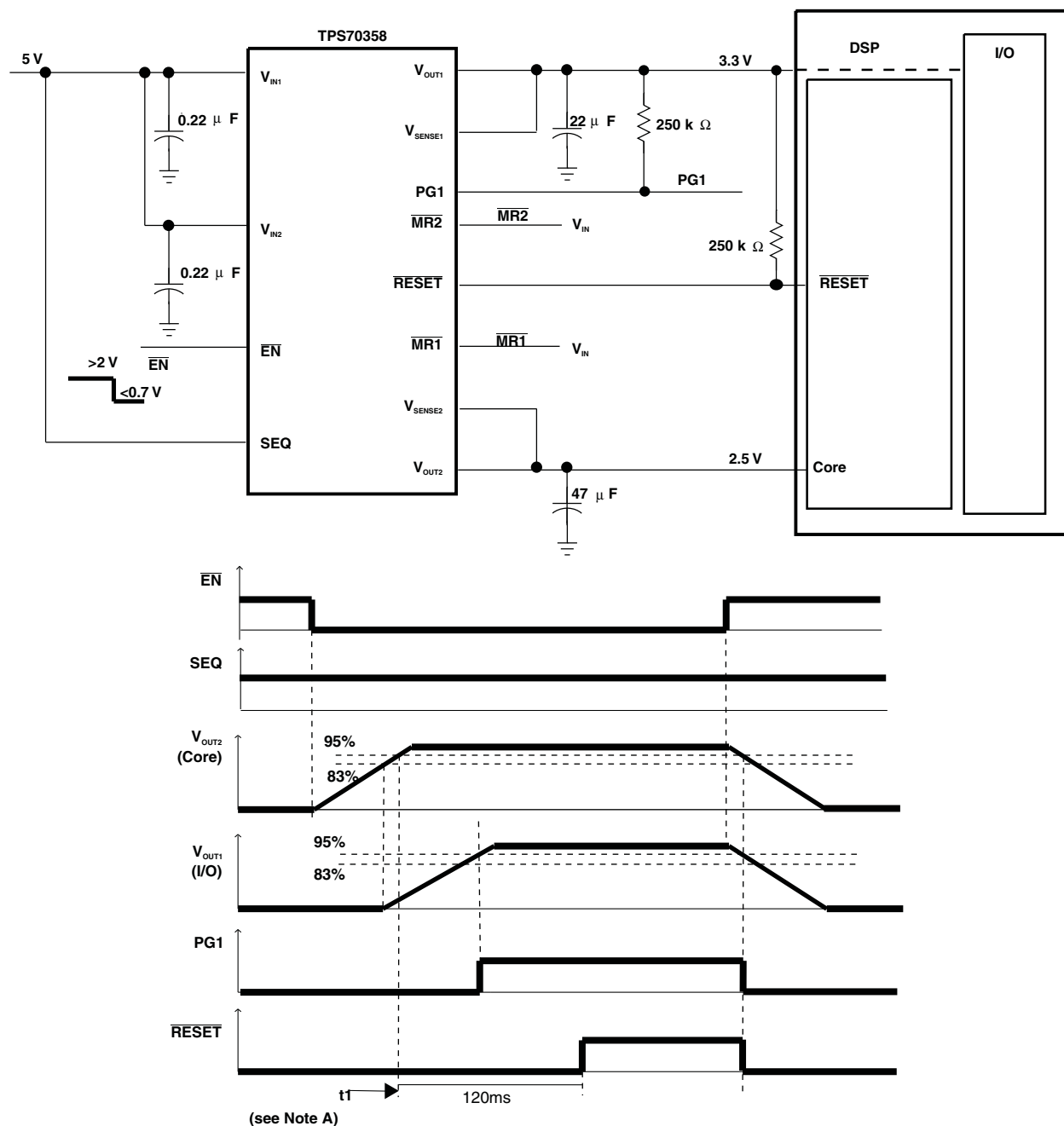
Figure 40 shows a typical application where the TPS70358 is powering up a DSP. In this application, by grounding the SEQ pin, V_{OUT1} (I/O) is powered up first, and then V_{OUT2} (core).



NOTE A: t_1 - Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and MR1 is logic high.

Figure 40. Application Timing Diagram (SEQ = Low)

Figure 41 shows a typical application where the TPS70358 is powering up a DSP. In this application, by pulling up the SEQ pin, V_{OUT2} (Core) is powered up first, and then V_{OUT1} (I/O).



NOTE A: t_1 - Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

Figure 41. Application Timing Diagram (SEQ = High)

Input Capacitor

For a typical application, a ceramic input bypass capacitor ($0.22\mu\text{F} - 1\mu\text{F}$) is recommended to ensure device stability. This capacitor should be as close as possible to the input pin. Due to the impedance of the input supply, large transient currents causes the input voltage to droop. If this droop causes the input voltage to drop below

the UVLO threshold, the device turns off. Therefore, it is recommended that a larger capacitor be placed in parallel with the ceramic bypass capacitor at the regulator's input. The size of this capacitor depends on the output current, response time of the main power supply, and the main power supply's distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

Output Capacitor

As with most LDO regulators, the TPS70358 requires an output capacitor connected between each OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value for V_{OUT1} is 22 μF and the ESR (equivalent series resistance) must be between 50 m Ω and 800 m Ω . The minimum recommended capacitance value for V_{OUT2} is 47 μF and the ESR must be between 50 m Ω and 2 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Below is a partial listing of surface-mount capacitors usable with the TPS703xx for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

VALUE	MANUFACTURER	PART NO.
680 μF	Kemet	T510X6871004AS
470 μF	Sanyo	4TPB470M
150 μF	Sanyo	4TPC150M
220 μF	Sanyo	2R5TPC220M
100 μF	Sanyo	6TPC100M
68 μF	Sanyo	10TPC68M
68 μF	Kemet	T495D6861006AS
47 μF	Kemet	T495D4761010AS
33 μF	Kemet	T495C3361016AS
22 μF	Kemet	T495C2261010AS

Regulator Protection

Both TPS70358 PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS70358 also features internal current limiting and thermal protection. During normal operation, the TPS70358 regulator 1 limits output current to approximately 1.75 A (typ) and regulator 2 limits output current to approximately 3.8 A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS70358MHKH	ACTIVE	CFP	HKH	20	25	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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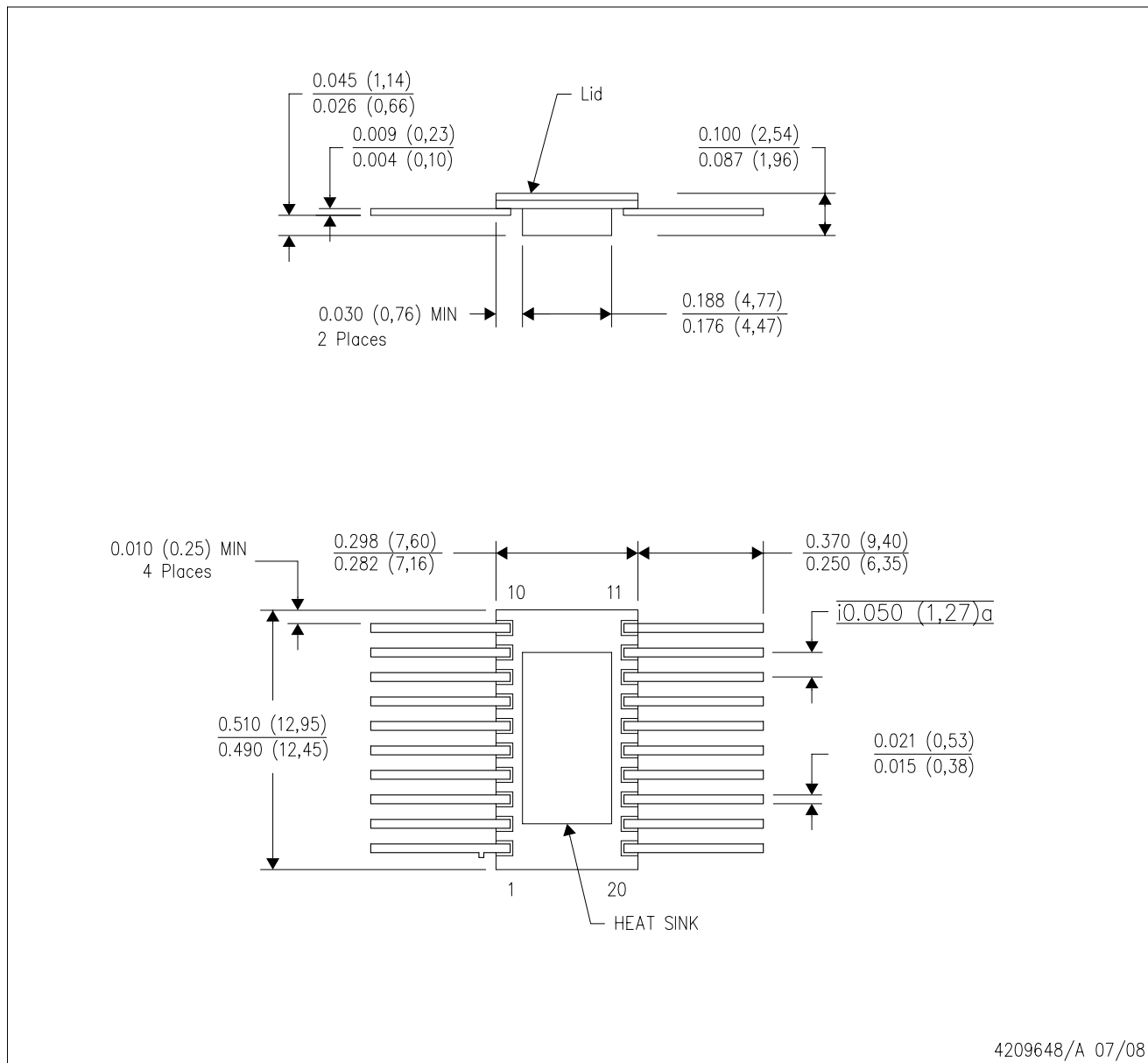
- Catalog: [TPS70358](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

HKH (R-CDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals will be gold plated.
 - E. Falls within MIL STD 1835 CDFP3-F20.

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