

Integrated Power Management Unit Top Specification

Check for Samples: [TPS659119-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 3: –40°C to 85°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C4A
- Embedded Power Controller (EPC) With EEPROM Programmability
- Two Efficient Step-Down DCDC Converters with Dynamic Voltage Scaling for Processor Cores (VDD1, VDD2)
- One Efficient Step-Down DCDC Converter for I/O Power (VIO)
- An Interface to Control an External DCDC Converter (EXTCTRL)
- Eight LDO Voltage Regulators and One RTC LDO (Supply for Internal RTC)
- One High-Speed I²C™ Interface for General-Purpose Control Commands (CTL-I²C)
- Two Independent Enable Signals for Controlling Power Resources (EN1, EN2) Which can be Used as a High-Speed I²C Interface Dedicated for VDD1 and VDD2 Voltage Scaling.
- Thermal Shutdown Protection and Hot-Die Detection
- A Real-Time Clock (RTC) Resource with:
 - Fast Start-Up 16.384-MHz Crystal Oscillator
 - Configurable Clock Source from Crystal Oscillator, External 32-kHz Clock or Internal 32-kHz RC Oscillator
 - Date, Time, and Calendar
 - Alarm Capability
- Nine Configurable GPIOs with Multiplexed Feature Support:
 - Four can be Used as Enable for External Resources, Included into Power-Up Sequence and Controlled by State-Machine
 - As GPI, GPIOs Support Logic-level Detection and Can Generate Maskable Interrupt for Wake-Up

- Two of the GPIOs Have 10-mA Current Sink Capability for Driving LEDs
- DCDCs Switching Synchronization Through an External 3-MHz Clock
- Two Reset Inputs, for Cold Reset (HDRST) and a Power Initialization Reset (PWRDN) for Thermal Reset Input
- 32-kHz Clock Output (CLK32KOUT) and System Reset (NRESPWRON) Included in Power Sequence
- Watchdog
- Two ON/OFF LED Pulse Generators and One PWM Generator

APPLICATIONS

- Automotive Applications
- Infotainment
- ADAs
- Instrument Cluster

DESCRIPTION

The TPS659119-Q1 is an integrated power management integrated circuit (PMIC) available in an 80-pin, 0.5-mm pitch, LQFP with thermal pad, and dedicated to applications powered by a 5-V input, and which require multiple power rails. The device provides three step-down converters and an interface to control an external converter, eight LDOs, and is designed to be a flexible PMIC for supporting different processors and applications.

Two of the step-down converters support dynamic voltage scaling by a dedicated I²C interface for optimum power savings. The third converter provides power for the I/Os and memory in the system.

The device includes eight general-purpose LDOs providing a wide range of voltage and current capabilities. Five of the LDOs support 1 to 3.3 V with 100-mV step and three (LDO1, LDO2, LDO4) support 1 to 3.3 V with 50-mV step. All LDOs are fully controllable by the I²C interface.

In addition to the power resources, the device contains an EPC to manage the power sequencing requirements of systems and an RTC. Power sequencing is programmable by EEPROM.

[Figure 1](#) shows the top-level diagram of the device.



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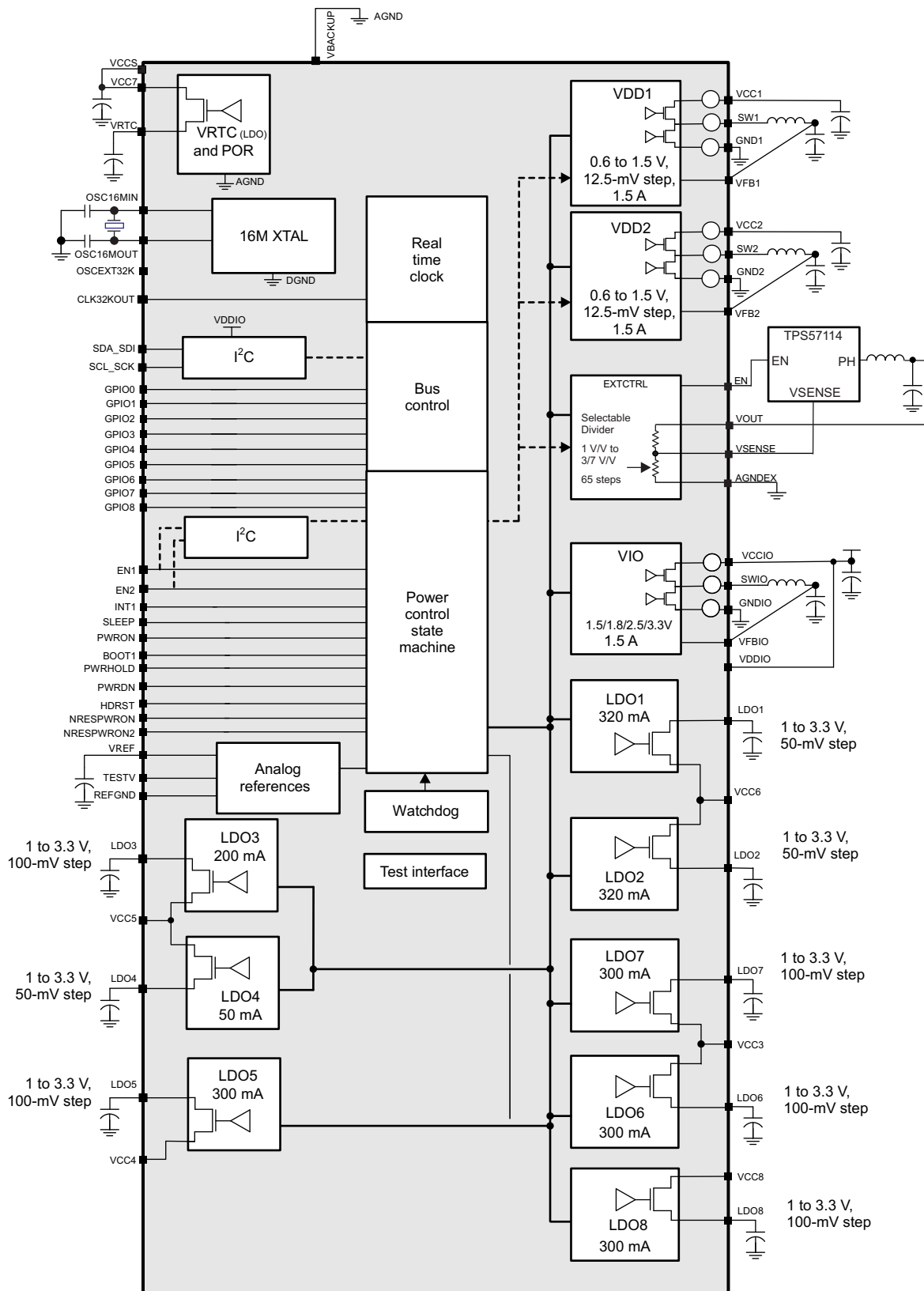


Figure 1. Top-Level Diagram

To request a full datasheet or the EVM hardware and software, please send an e-mail to tps659119@list.ti.com.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|--------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TPS659119AIPFPRQ1 | ACTIVE | HTQFP | PFP | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | T659119A1 | Samples |
| TPS659119BAIPFPRQ1 | ACTIVE | HTQFP | PFP | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | T659119BA | Samples |
| TPS659119CAIPFPRQ1 | ACTIVE | HTQFP | PFP | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | T659119CA | Samples |
| TPS659119DAIPFPRQ1 | ACTIVE | HTQFP | PFP | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | T659119DA | Samples |
| TPS659119EAIPFPRQ1 | ACTIVE | HTQFP | PFP | 80 | 1 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS659119AIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |
| TPS659119BAIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |
| TPS659119CAIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |
| TPS659119DAIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |
| TPS659119EAIPFPRQ1 | HTQFP | PFP | 80 | 1 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

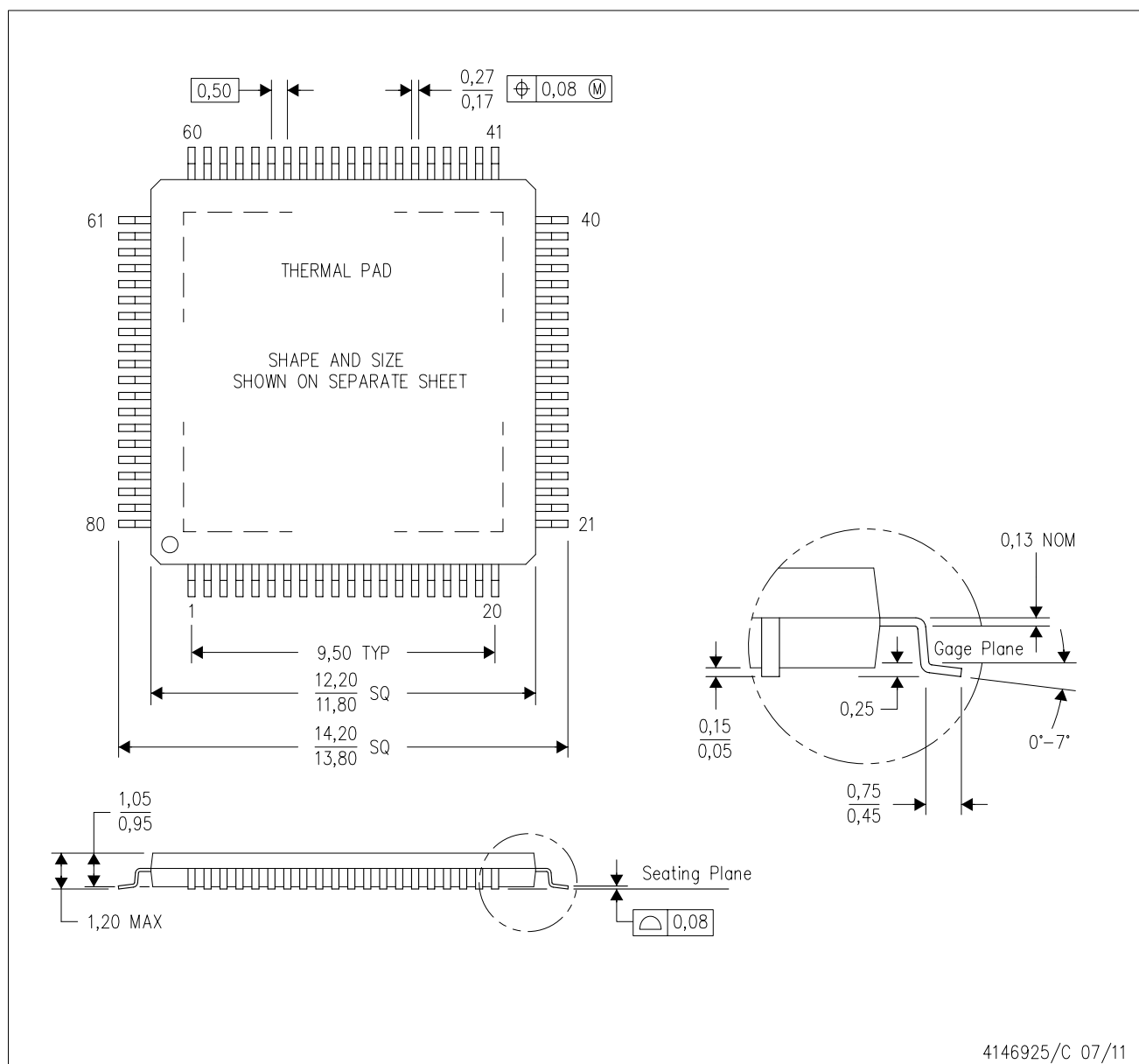


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS659119AIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| TPS659119BAIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| TPS659119CAIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| TPS659119DAIPFPRQ1 | HTQFP | PFP | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| TPS659119EAIPFPRQ1 | HTQFP | PFP | 80 | 1 | 367.0 | 367.0 | 55.0 |

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PFP (S-PQFP-G80)

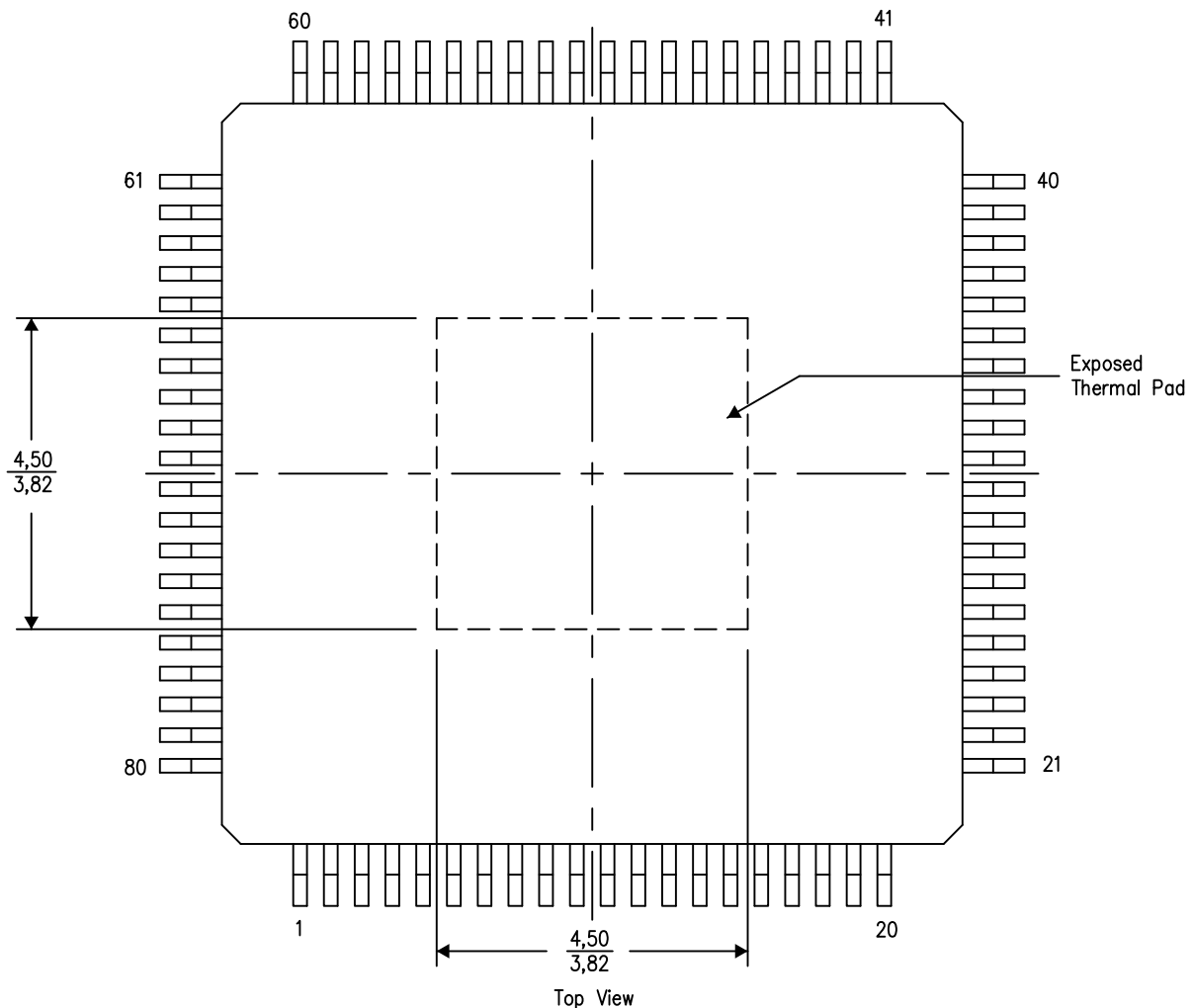
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



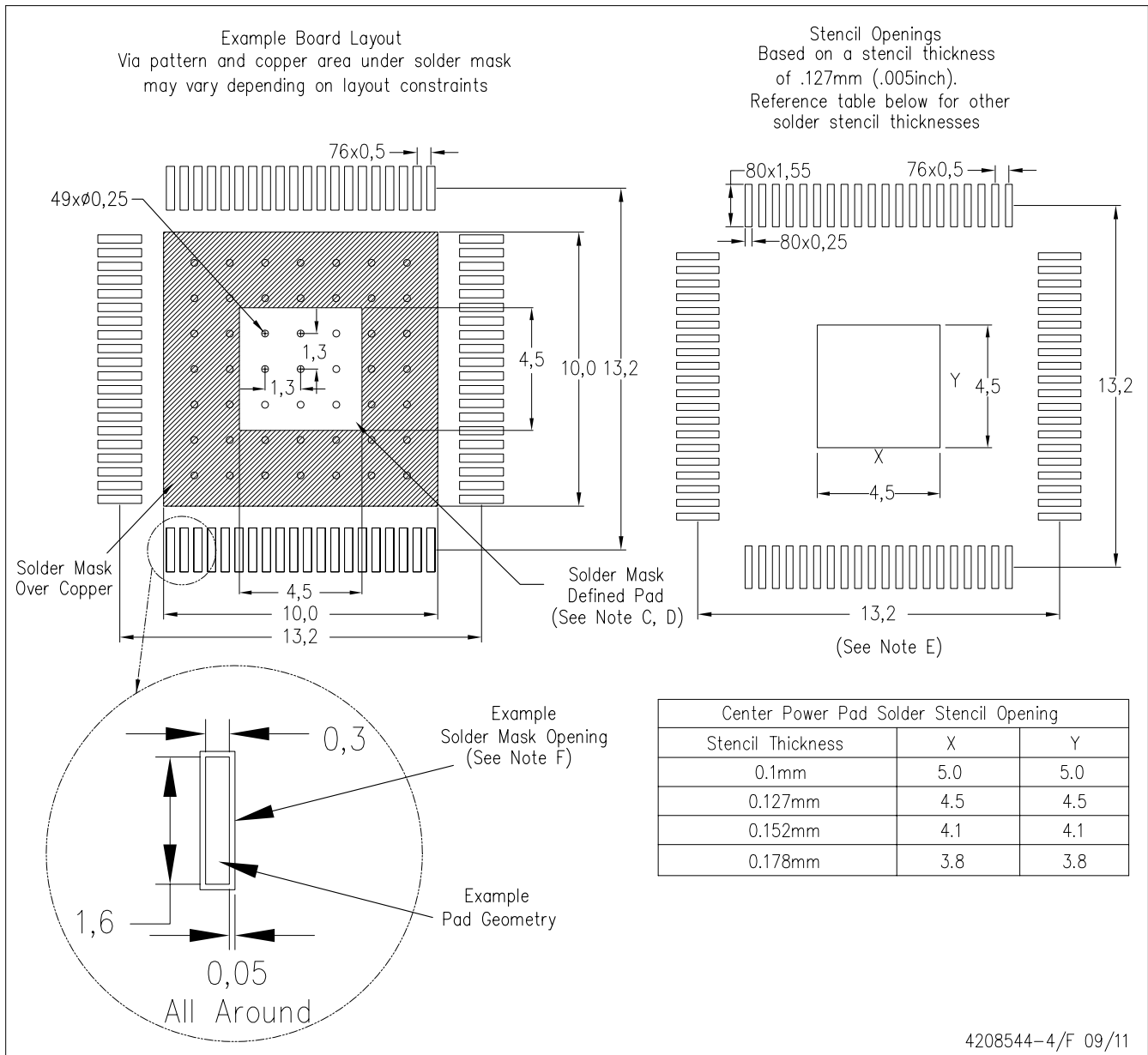
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NOTE: A. All linear dimensions are in millimeters

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PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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