

Small, Triple-Input Power Multiplexer with Auto-Select and Low Drop-out Voltage Regulator

Check for Samples: [TPS22933](#)

FEATURES

- Three Integrated Load Switches Automatically Choose Highest Input
- Integrated 3.6-V fixed LDO
- Switched and Always on LDO Outputs
- Small μ QFN package 1.5mm $\times$ 1.5mm
- Input Voltage Range: 2.5-V to 12-V
- Low ON-Resistance (r_{ON})
 - $r_{ON} = 2.4\Omega$ at $V_{IN} = 5.0\text{-V}$
 - $r_{ON} = 2.6\Omega$ at $V_{IN} = 4.2\text{-V}$
- 50-mA Maximum Continuous Current
- Low Threshold Control Input (EN)
- Switchover time 18- μ s Typical

APPLICATIONS

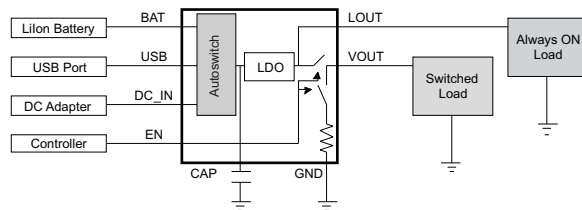
- Smart Phones
- GPS Devices
- Digital Cameras
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Portable Instrumentation

DESCRIPTION

The TPS22933 is a small, low r_{ON} , triple-input power multiplexer with auto-input selection and a Low Drop-Out linear regulator. The device contains three P-channel MOSFETs that can operate over an input voltage range of 2.5-V to 12-V. The TPS22933 automatically selects the highest level (from BAT, USB, and DC_IN) and enables that input to source the LDO. LOU $\bar{T}$ is an always-on output from the LDO. The Enable function (EN pin) allows VOUT to be switched on or off, enables a quick discharge resistor, and is capable of interfacing directly with low-voltage control signals.

The TPS22933 is available in a small, space-saving 8-pin μ QFN package and is characterized for operation over the free-air temperature range of -40°C to 85°C .

TYPICAL APPLICATION



FEATURE LIST ⁽¹⁾

	r_{ON} (typical) at 5.0 V	OUTPUT VOLTAGE	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	VOUT ENABLE
TPS22933A	2.4 Ω	3.6 V	yes	50 mA	Active High

(1) This feature discharges the output of the switch to ground through a 64- Ω resistor, preventing the output from floating



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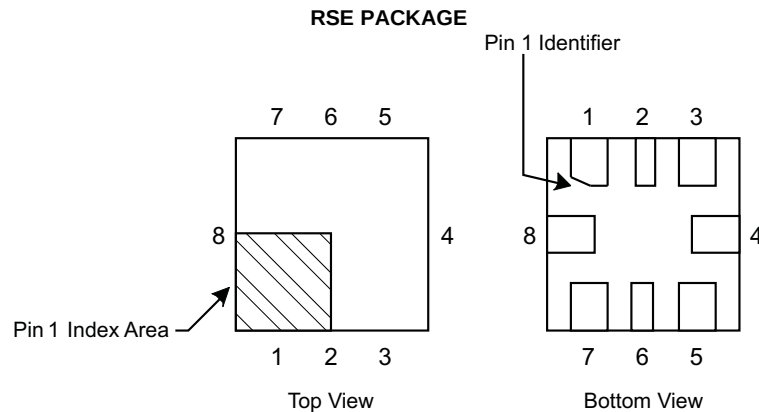


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	LDO VOLTAGE	TOP-SIDE MARKING
-40°C to 85°C	RSE (0.5mm pitch)	Reel of 3,000	TPS22933ARSER	3.6 V	4Q
		Reel of 250	TPS22933ARSET		

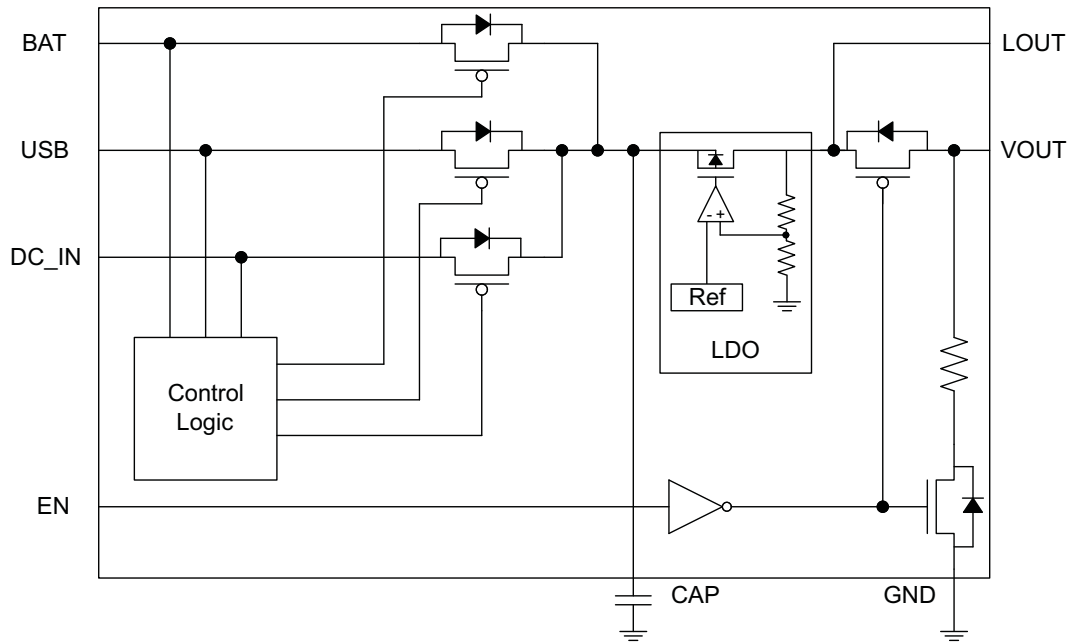
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



PIN FUNCTIONS

PIN		
NUMBER	NAME	DESCRIPTION
1	BAT	Source Voltage 1 (Battery)
2	USB	Source Voltage 2 (V+ USB)
3	DC_IN	Source Voltage 3 (DC Adapter)
4	GND	Ground
5	EN	VOUT Enable (Cannot be left floating)
6	CAP	Capacitor for LDO
7	VOUT	Switched LDO Output
8	LOUT	Always on LDO Output

BLOCK DIAGRAM



FUNCTION TABLE

EN	LDO to LOUT	LDO to VOUT	VOUT to GND
L	ON	OFF	ON
H	ON	ON	OFF

INPUT SELECTION TABLE (V1 > V2 > V3)

BAT	USB	DC_IN	LDO Supply
V1	V2 or V3	V2 or V3	BAT
V2 or V3	V1	V2 or V3	USB
V2 or V3	V2 or V3	V1	DC_IN
V1	V1	V1	See ⁽¹⁾

(1) Whichever source achieves the highest level the fastest will supply the LDO.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
VIN	Input voltage range	BAT, USB, DC_IN	–0.3 to 14.0	V
VOUTPUT	Output voltage range	VOUT, LOUT	–0.3 to 6.0	V
VEN	Input voltage range	EN	–0.3 to 6.0	V
IMAX	Maximum continuous switch current		75	mA
IPLS	Maximum pulsed switch current, pulse <300 μs, 2% duty cycle		100	mA
T _A	Operating free-air temperature range		–40 to 85	°C
T _{stg}	Storage temperature range		–65 to 150	°C
T _{lead}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	2000	V
		Charged-Device Model (CDM)	1000	

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THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS22933	UNITS
		RSE (7 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	115.6	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	59.9	
θ_{JB}	Junction-to-board thermal resistance	27.4	
ψ_{JT}	Junction-to-top characterization parameter	2.1	
ψ_{JB}	Junction-to-board characterization parameter	27.3	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	–	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	BAT, USB, DC_IN	2.5		12.0	V
V_{EN}		EN	0.0		5.5	V
V_{IH}	EN pin High-level input voltage, (EN > V_{IH} Min, VOUT = LDO Output)	BAT = 2.5-V to 5.5-V, USB, DC_IN = 2.5-V to 12-V	1.15		5.5	V
V_{IL}	EN pin Low-level input voltage, (EN < V_{IL} Max, VOUT = pull-down)	BAT = 2.5-V to 5.5-V, USB, DC_IN = 2.5-V to 12-V	0.0		0.6	V
$I_{OUT-LOUT}$	LOUT Current	$V_{BAT} = 4.2\text{ V OR }V_{USB} = 5\text{ V OR }V_{DC_IN} = 5\text{ V},$ EN = 3.4 V, $I_{OUT-VOUT} = 0\text{ mA}$			50	mA
$I_{OUT-VOUT}$	VOUT Current	$V_{BAT} = 4.2\text{ V OR }V_{USB} = 5\text{ V OR }V_{DC_IN} = 5\text{ V},$ EN = 3.4 V, $I_{OUT-LOUT} = 0\text{ mA}$			50	mA
$I_{OUT-TOTAL}$	LOUT + VOUT current	$V_{BAT} = 4.2\text{ V OR }V_{USB} = 5\text{ V OR }V_{DC_IN} = 5\text{ V},$ EN = 3.4 V			50	mA
CAP	LDO Capacitor (on CAP pin)		20 ⁽¹⁾			nF
	LOUT Capacitor			1		μF
	VOUT Capacitor			1		μF

(1) Refer to the application section

ELECTRICAL CHARACTERISTICS

BAT = 2.5-V to 12.0-V, USB = 2.5-V to 12.0-V, DC_IN = 2.5-V to 12.0-V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾ ⁽²⁾ ⁽³⁾	T _A	MIN	TYP ⁽⁴⁾	MAX	UNIT
I _{IN-BAT}	Operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 3 V, V _{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	μA
	Quiescent current	I _{OUT} = 0, V _{BAT} = 4.2 V, V _{USB} = 5 V, V _{DC_IN} = 3 V, EN = 3.4 V			0.7	2	
I _{IN-USB}	Operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 5 V, V _{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	μA
	Quiescent current	I _{OUT} = 0, V _{BAT} = 4.2V, V _{USB} = 5V, V _{DC_IN} = 5.5V, EN = 3.4 V			0.7	2	
I _{IN-DC_IN}	Operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 3 V, V _{DC_IN} = 5 V, EN = 3.4 V	Full		9.2	15	μA
	Quiescent current	I _{OUT} = 0, V _{BAT} = 4.2V, V _{USB} = 5.5V, V _{DC_IN} = 5V, EN = 3.4 V			0.7	2	
I _{IN-USB}	Hi-Voltage operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 12 V, V _{DC_IN} = 5 V, EN = 3.4 V	Full		10.8	20	μA
I _{IN-DC_IN}	Hi-Voltage operating current	I _{OUT} = 0 mA, V _{BAT} = 4.2 V, V _{USB} = 5 V, V _{DC_IN} = 12 V, EN = 3.4 V	Full		10.8	20	μA
R _{ON}	ON resistance (USB to CAP, BAT to CAP, DC_IN to CAP)	V _{IN} = 5.0 V, I _{OUT} = 10 mA	25°C		2.4	3.3	Ω
			Full			3.5	
		V _{IN} = 4.2 V, I _{OUT} = 10 mA	25°C		2.6	3.5	Ω
			Full			4	
		V _{IN} = 2.5 V, I _{OUT} = 10 mA	25°C		3.8	5	Ω
			Full			6	
R _{ONVOUT}	ON resistance (LDO output to VOUT)	V _{IN} = 4.2 V, I _{OUT-VOUT} = 10 mA	25°C		1.3	2.5	Ω
			Full			3.0	
R _{PD}	Output pull down resistance	V _{IN} = 4.2 V, V _{EN} = 0 V, I(into VOUT) = 10 mA	25°C		63.8	120	Ω
I _{EN}	EN input leakage	V _{EN} = 1.6 V to 5.5 V or GND	Full			1	μA
V _{DO-VOUT}	Dropout voltage VOUT ⁽⁵⁾⁽⁶⁾	I _{OUT} = 10 mA	Full		0.11		V
V _{DO-LOUT}	Dropout voltage LOUT	I _{OUT} = 10 mA ⁽⁵⁾⁽⁶⁾	Full		0.10		V
V _{LOUT}	Always on LDO output voltage (LOUT pin)	V _{IN} < 3.4 V, I _{OUT} = 10 mA, V _{EN} = 1.8 V	Full		V _{IN} – V _{DO-LOUT}		V
		V _{IN} > 4 V, I _{OUT} = 10 mA, V _{EN} = 1.8 V	Full	3.42	3.6	3.78	
V _{VOUT}	Switched LDO output voltage (VOUT pin)	V _{IN} < 3.4 V, I _{OUT} = 10 m A, V _{EN} = 1.8 V	Full		V _{IN} – V _{DO-VOUT}		V
		V _{IN} > 4 V, I _{OUT} = 10 mA, V _{EN} = 1.8 V	Full	3.39	3.57	3.75	
V _{CO}	Changeover voltage	V _{BAT} = 4.2 V, V _{USB} = 4.0 V rising to 4.4 V	Full		0.15		V
t _{CO}	Changeover time	V _{BAT} =4.2 V, V _{USB} = 4.0 V rising to 4.4 V, CAP = 0.01 μF, I _{OUT} = 10 mA	25°C		18		μs
			Full			50	
t _{OFF}	VOUT off time	EN high to low, C(VOUT) = 1 μF, VOUT load = 360 Ω	Full		32		μs
t _{ON}	VOUT on time	EN low to high, C(VOUT) = open, VOUT load = 360 Ω	Full		65		μs

(1) V_{IN} is defined as the highest voltage present on the BAT, USB and DC_IN pins.

(2) One of the voltages on BAT, USB and DC_IN must be > V_{IN} (Min), others can be 0 V.

(3) V_{BAT}, V_{USB} and V_{DC_IN} refer to the voltages on BAT, USB and DC_IN respectively. I_{OUT}, I_{OUT-VOUT} and I_{OUT-LOUT} refer to the currents for the combined output current for VOUT and LOUT, the current on VOUT and the current on LOUT respectively.

(4) TYP is 25°C, BAT = 4.2-V, USB = 0-V, DC_IN = 0-V.

(5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: V_{IN} – V_{DROPOUT}.

(6) Dropout voltage is measured at the V_{IN} that causes the output to drop to 100mV below its nominal voltage. For VOUT, the voltage drop across the output switch is included (10mA × R_{ONVOUT}).

PARAMETRIC MEASUREMENT INFORMATION

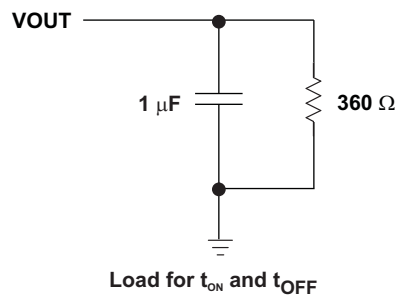


Figure 1. Test Circuit and t_{ON} / t_{OFF} Waveforms

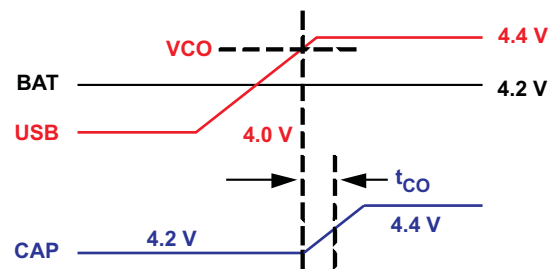


Figure 2. Switchover Timing

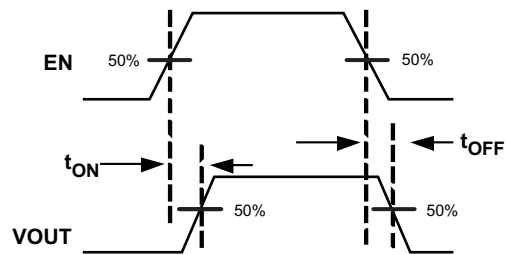


Figure 3. VOUT Enable Timing

APPLICATION INFORMATION

POWER CHANGEOVER

The TPS22933 LDO is powered by the highest level input. When input voltages change, the TPS22933 may change which input powers the LDO. During initial power up, the input that reaches the highest value first will power the LDO. Once that decision is made, changing between input sources is based on VCO. When an input source becomes VCO over the input currently supplying power to the LDO, changeover will occur and the new, higher input will power the LDO.

TPS22933A EXAMPLE:

Initial power up:

DC_IN = 0V; USB = 0V; EN = 0V

BAT is applied at 4.2V

LDO power comes from BAT

LOUT = 3.6V; CAP = 4.2V; VOUT = 0V

USB power is connected at 5.0V, BAT remains 4.2V and DC_IN remains 0V

LDO power is changed from BAT to USB in t_{CO}

LOUT = 3.6V; CAP = 5.0V; VOUT = 0V

DC_IN power is connected at 5.0V, BAT remains 4.2V and USB remains 5V

No change in LDO power

LOUT = 3.6V; CAP = 5.0V; VOUT = 0V

EN = VIH, BAT remains 4.2V, USB remains 5.0V and DC_IN remains 5V

LOUT = 3.6V, CAP = 5.0V; VOUT = 3.6V

USB power is removed, BAT remains 4.2V and DC_IN remains 5.0V

LDO power is changed from USB to DC_IN

LOUT = 3.6V; CAP = 5.0V; VOUT = 3.6V

DC_IN power is removed, BAT remains 4.2V and USB remains 0V:

LDO power is changed from DC_IN to BAT

LOUT = 3.6V; CAP = 4.2V; VOUT = 3.6V

ON/OFF CONTROL

The EN pin controls the state of the VOUT switch and VOUT pull-down switch. EN has no control over LOUT. Asserting EN enables the VOUT switch and disables the Quick Output Discharge (QOD) switch. Deasserting EN disables the VOUT switch and enables the QOD switch. EN is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin is compatible with standard GPIO Logic threshold and can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

LDO CAPACITOR (for CAP pin)

An optional capacitor on the CAP pin helps stabilize the integrated LDO. Care should be taken in capacitor sizing to reduce inrush currents. The voltage on the CAP pin will follow the highest input. Since the max input voltage is 12-V, the capacitor voltage rating must be higher than 12-V.

BOARD LAYOUT

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for BAT, USB, DC_IN, LOUT, VOUT, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

APPLICATION EXAMPLES

Below are two diagrams of typical applications for the TPS22933A. In all cases, the unused power inputs can be left floating or tied to ground. The EN pin must not be left floating.

Figure 4 shows three power inputs multiplexed to source the LDO. The LDO always on output (LOUT) is tied to an MSP430. The MSP430 then determines when to enable the switched output (VOUT) by driving the EN pin.

Figure 5 shows three power inputs multiplexed to source only through the CAP pin. In this case, the LDO outputs are not used (EN is tied low). The highest of the inputs is chosen to drive the voltage at the CAP pin.

Note that these two applications are not mutually exclusive. An application could use the CAP pin as a power output and use one or both of the LDO outputs.

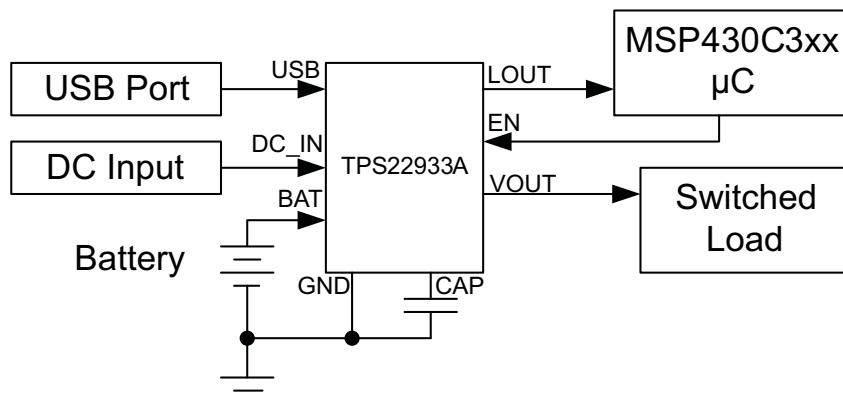


Figure 4. Application Example 1

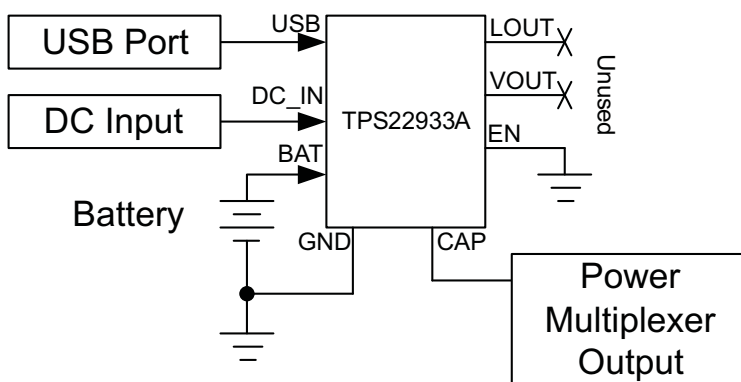
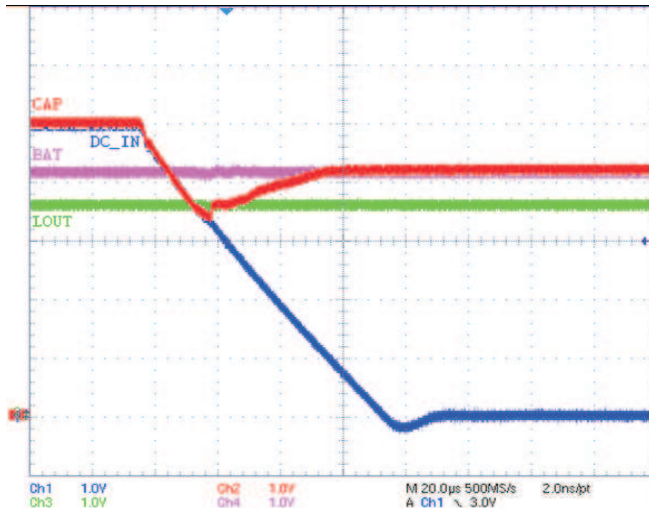


Figure 5. Application Example 2

PERFORMANCE GRAPHS

Table 1. Performance Graphs and Plots

Type	Description	Figure
Scope Plot	DC_IN to BAT switchover	Figure 6
Graph	RON versus VIN (BAT, USB, DC_IN) 25°C	Figure 7
Graph	RON versus VIN (Any input)	Figure 8
Graph	Quiescent Current versus Input Voltage (Any input)	Figure 9
Graph	Operating Current versus Input Voltage (Any Input)	Figure 10
Scope Plot	t _{OFF} (VIN = 4.2-V, C(VOUT) = 1uF, 25°C)	Figure 11
Scope Plot	t _{OFF} (VIN = 4.2-V, C(VOUT) = open, 25°C)	Figure 12
Scope Plot	t _{ON} (VIN = 4.2-V, C(VOUT) = 1uF, 25°C)	Figure 13
Scope Plot	t _{ON} (VIN = 4.2-V, C(VOUT) = open, 25°C)	Figure 14
Graph	LOUT and VOUT versus Temperature at VIN = 4.2-V	Figure 15
Graph	LOUT and VOUT versus IOU (VIN = 4.2-V, Temp = 25°C)	Figure 16
Graph	LOUT Dropout Voltage versus Temperature (VIN = 2.5-V)	Figure 17
Graph	VOUT Dropout Voltage versus Temperature (VIN = 2.5-V)	Figure 18
Graph	Output Pull-down Resistance (R _{PD}) versus Temperature (10mA into VOUT)	Figure 19



**Figure 6. DC_IN Removed, BAT Powers LDO
(LOUT = 3.6-V)**

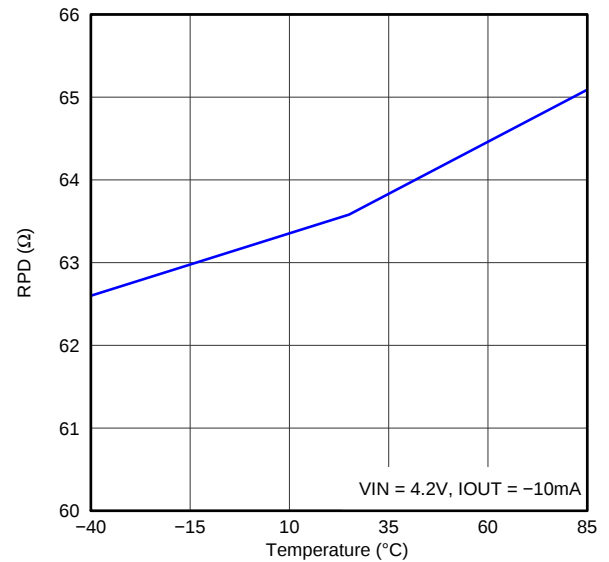
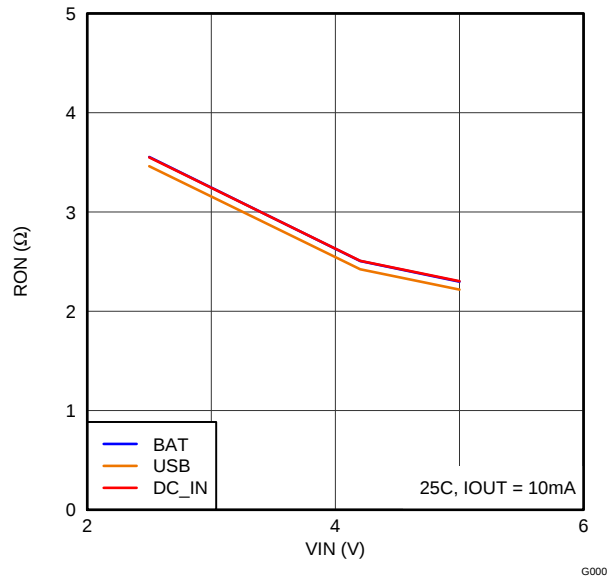
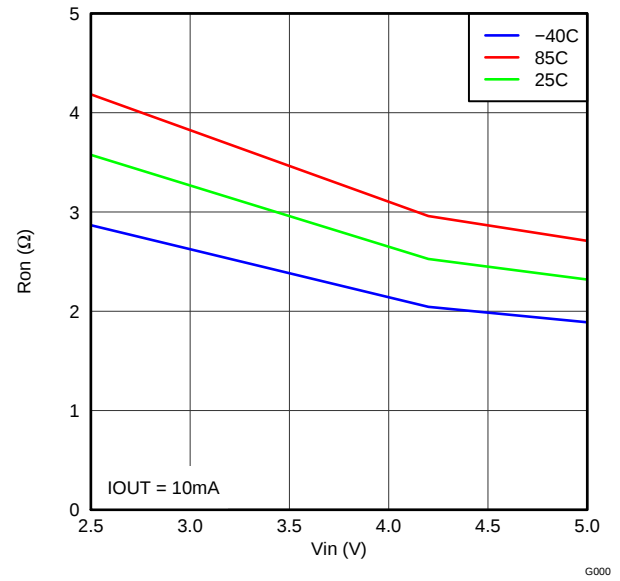
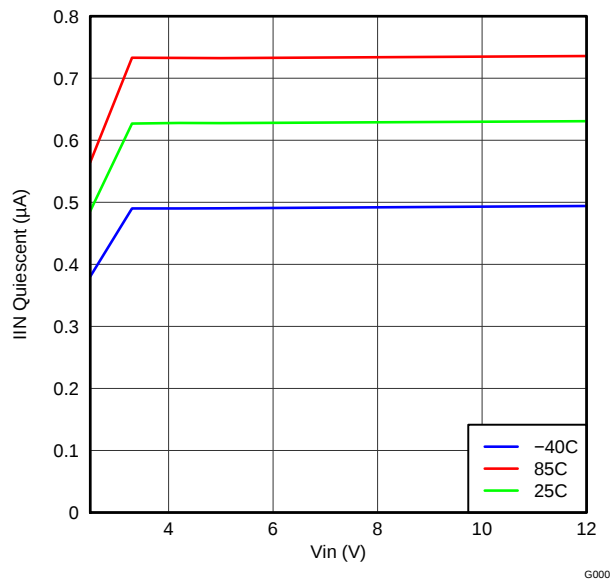
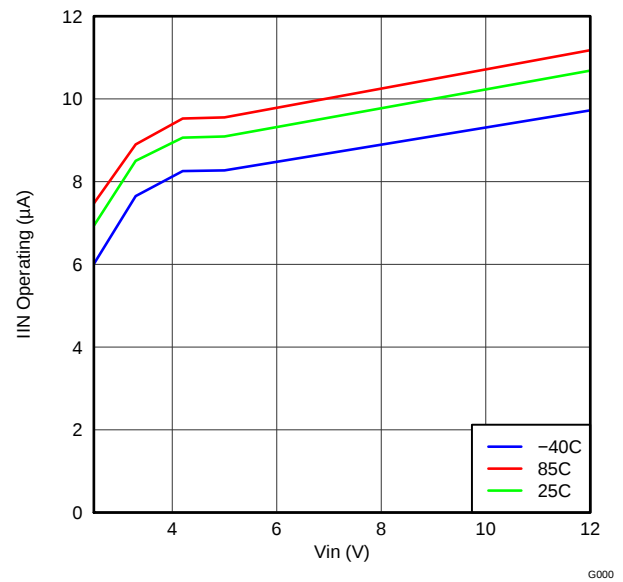


Figure 7. RPD vs Temp


Figure 8. R_{ON} vs VIN (Typical)

Figure 9. R_{ON} vs VIN

Figure 10. $I_{IN}(\text{Quiescent})$ vs VIN

Figure 11. $I_{IN}(\text{Operating})$ vs VIN

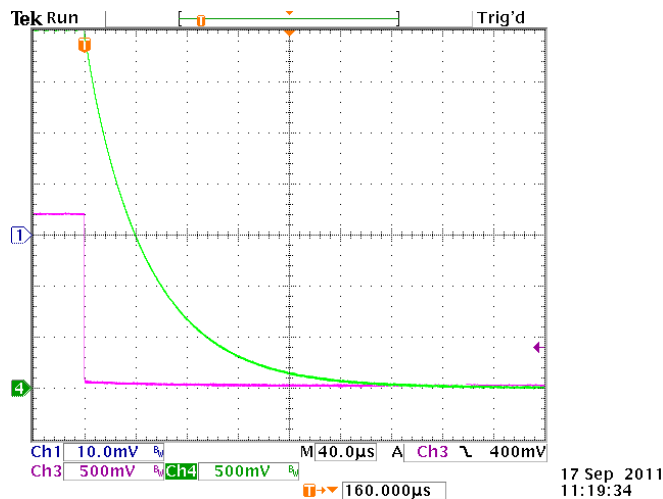


Figure 12. VOUT t_{OFF} (1µF on VOUT)

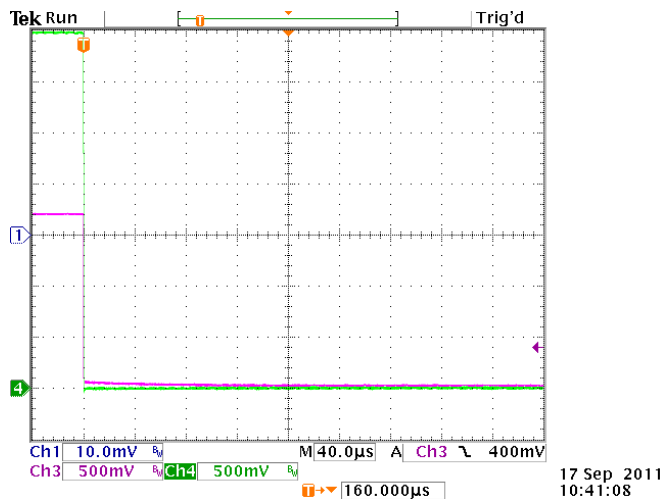


Figure 13. VOUT t_{OFF} (No Capacitor on VOUT)

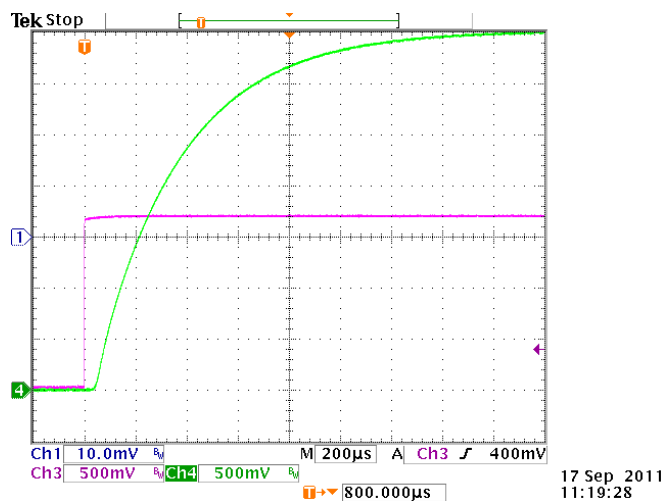


Figure 14. VOUT t_{ON} (1-µF on VOUT)

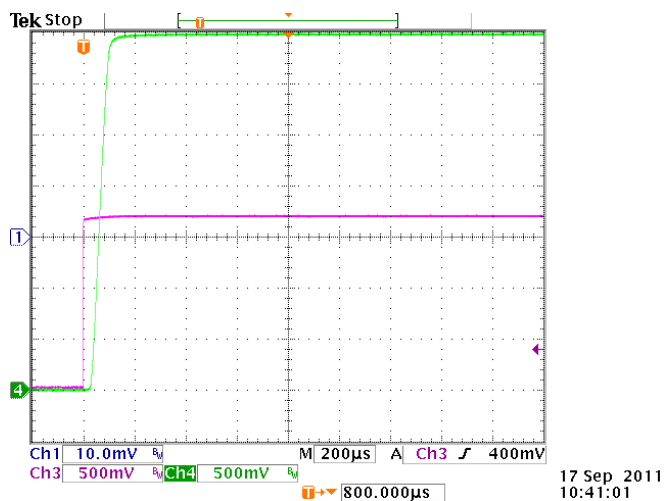


Figure 15. VOUT t_{ON} (No Capacitor on VOUT)

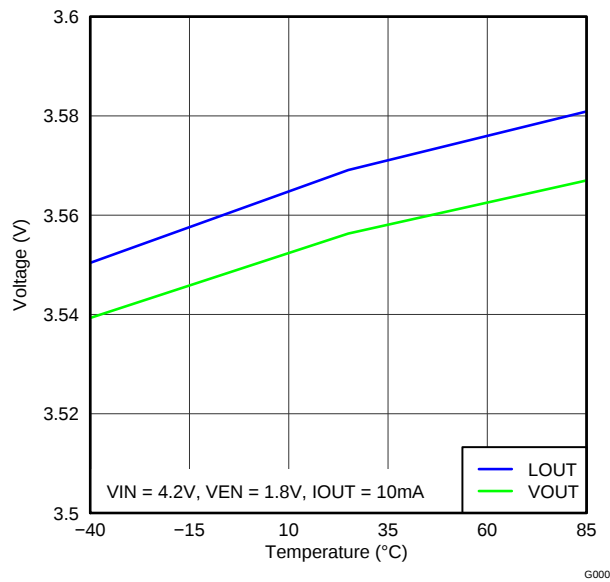


Figure 16. LOUT-VOUT vs Temp VIN 4p2V

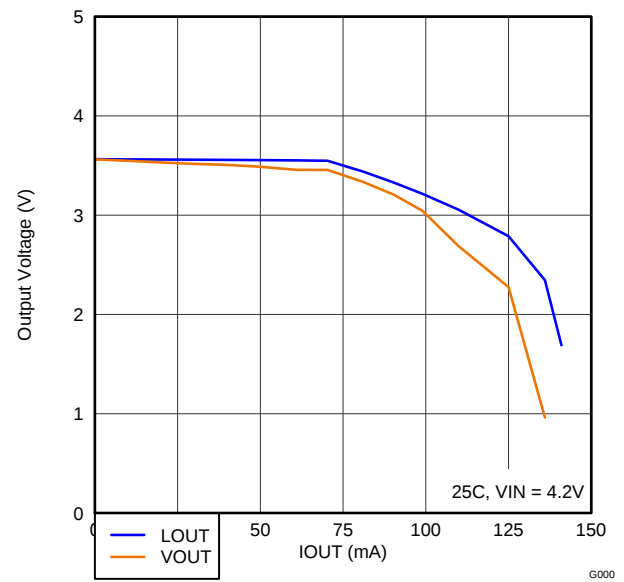


Figure 17. LOUT-VOUT vs IOUT

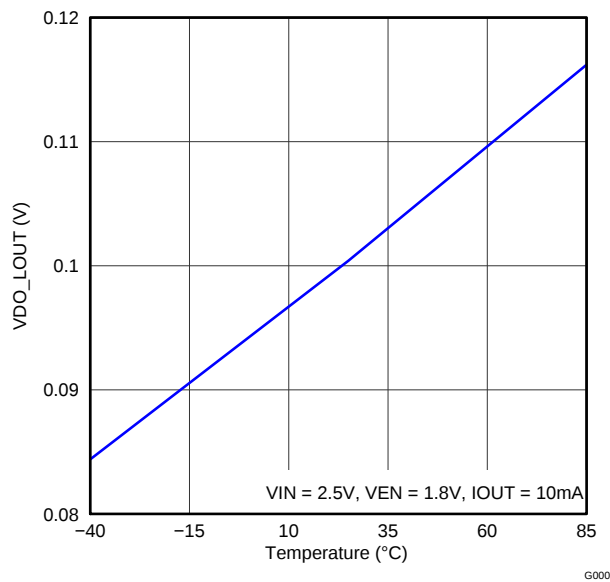


Figure 18. VDOLOUT vs Temp VIN 2p5V

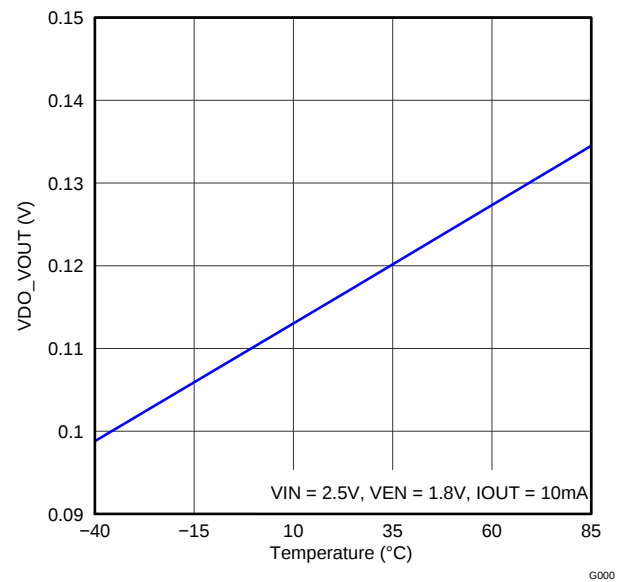


Figure 19. VDOVOUT vs Temp VIN 2p5V

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPS22933ARSER	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS22933ARSET	ACTIVE	UQFN	RSE	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22933ARSER	UQFN	RSE	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2
TPS22933ARSET	UQFN	RSE	8	250	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

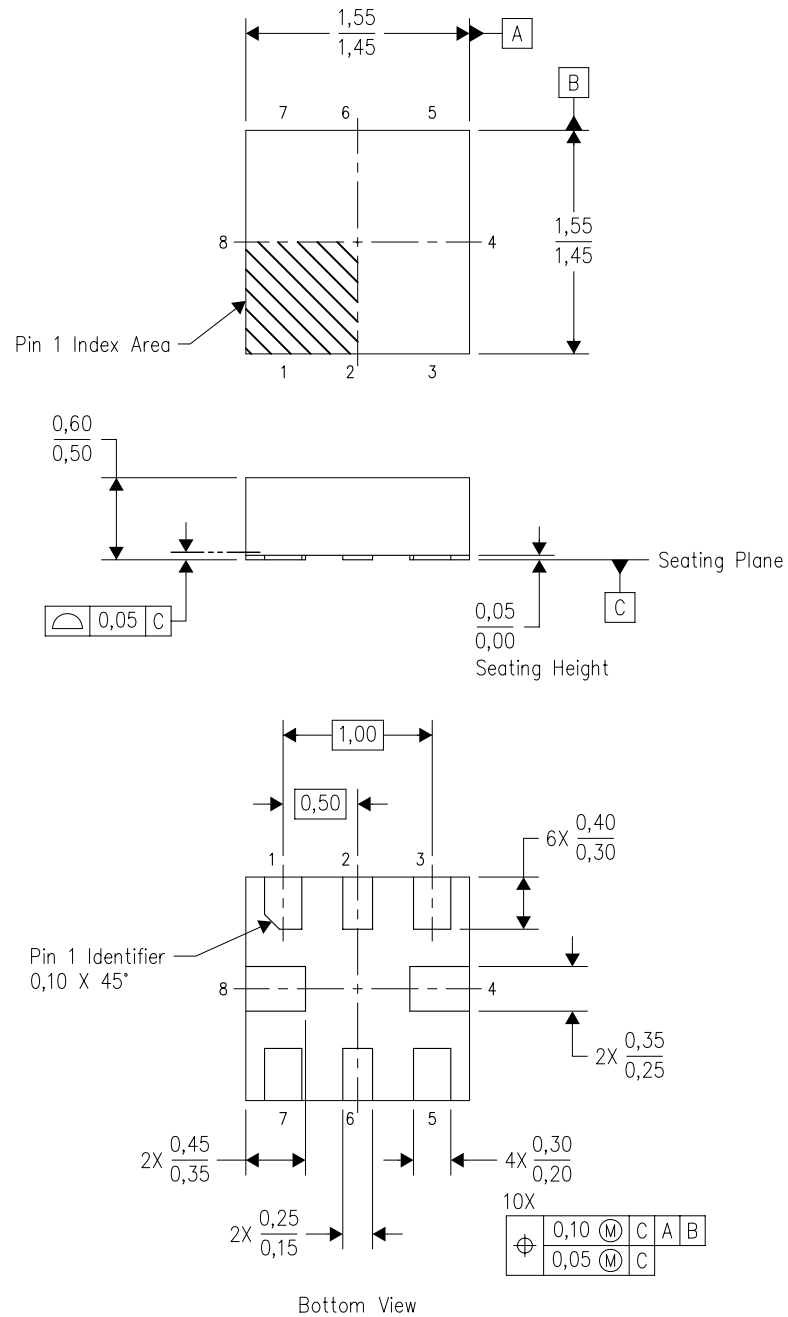


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22933ARSER	UQFN	RSE	8	3000	202.0	201.0	28.0
TPS22933ARSET	UQFN	RSE	8	250	202.0	201.0	28.0

RSE (S-PUQFN-N8)

PLASTIC QUAD FLATPACK NO-LEAD



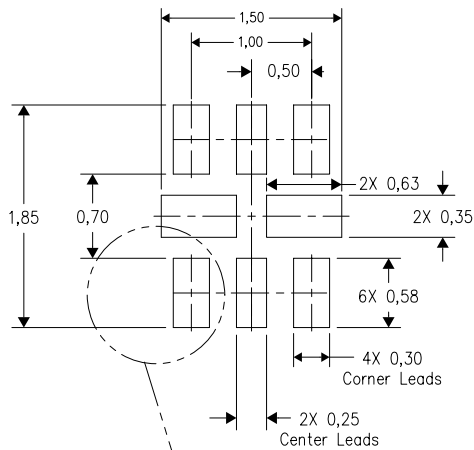
4207268-2/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation UECD.

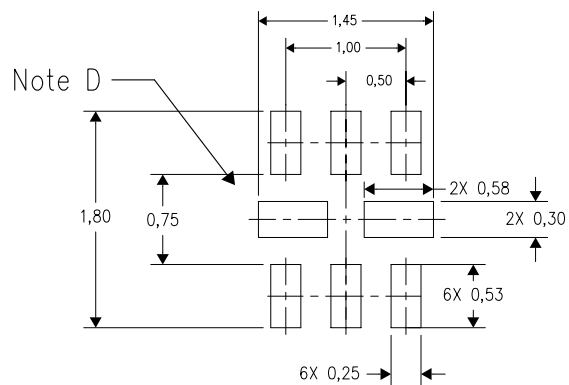
RSE (S-PUQFN-N8)

PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout



Example Stencil Design
(Note E)



4208106-2/E 01/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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