

ULTRA SMALL, LOW RESISTANCE LOAD SWITCH

Check for Samples: TPS22930

FEATURES

- Integrated Single Channel Load Switch
- Ultra Small CSP-4 Package (0.9mm x 0.9mm, 0.5mm pitch)
- Input Voltage Range: 1.4V to 5.5V
- Ultra Low R_{ON} Resistance
 - $-R_{ON} = 35m\Omega$ at $V_{IN} = 5V$
 - $-R_{ON} = 36m\Omega$ at $V_{IN} = 3.6V$
 - $-R_{ON} = 49m\Omega$ at $V_{IN} = 1.8V$
- 2A Maximum Continuous Switch Current
- Low Quiescent Current (< 3µA)
- Low Control Input Threshold Enables Use of 1.2V/1.8V/2.5V/3.3V Logic
- Controlled Slew Rate
- Under Voltage Lockout
- Reverse Current Protection When Disabled

APPLICATIONS

- Smartphone / Wireless Handsets
- Portable Industrial / Medical Equipment
- Portable Media Players
- Point of Sales Terminals
- GPS Navigation Devices
- Digital Cameras
- Portable Instrumentation

DESCRIPTION

The TPS22930 is a small, low R_{ON} load switch with controlled turn on. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.4V to 5.5V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22930 is active high enable.

The TPS22930 device provides circuit breaker functionality by disabling the body diode during reverse voltage (also known as reverse current) situations. Reverse current protection is active only when the power-switch is disabled (off). The device disengages the body diode when the output voltage (V_{OUT}) is driven higher than the input (V_{IN}) to stop the flow of current towards the input side of the switch. Additionally, under-voltage lockout (UVLO) protection turns the switch off if the input voltage is too low.

The slew rate of the device is internally controlled in order to avoid inrush current.

The TPS22930 is available in an ultra-small, space-saving 4-pin CSP package and is characterized for operation over the free-air temperature range of -40°C to 85°C.

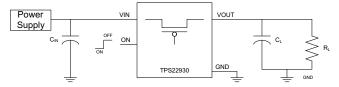


Figure 1. Typical Application

Feature List

Device	RON (typ) at 4.2V			Maximum Continuous Current	Enable
TPS22930A	35mΩ	5.4µs	No	2A	Active High

(1) This feature discharges output of the switch to GND through a resistor, preventing the output from floating when the pass FET is disabled



RUMENTS

SLVSBL3 – NOVEMBER 2012 www.ti.com



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NO.	TOP-SIDE MARKING/STATUS	
-40°C to 85°C	YZV	Tape and reel 3000 units	TPS22930AYZVR	3Q	ì

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

	-		VALUE	UNIT ⁽²⁾
V _{IN}	Input voltage range		-0.3 to 6	V
V _{OUT}	Output voltage range		-0.3 to 6	V
V _{ON}	Input voltage range		-0.3 to 6	V
I _{MAX}	Maximum continuous switch	current	2	Α
I _{PLS}	Maximum pulsed switch cur	rent, pulse ≤1ms, 25% duty cycle	2.5	Α
T _A	Operating free-air temperate	ure range ⁽³⁾	-40 to 85	°C
TJ	Maximum junction temperat	ure	150	°C
T _{STG}	Storage temperature range		–65 to 150	°C
T _{LEAD}	Maximum lead temperature	(10-s soldering time)	300	°C
FCD	Electrostatic discharge	Human-Body Model (HBM)	2000	
ESD	protection	Charged-Device Model (CDM)	1000	V

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

		TPS22930		
	THERMAL METRIC ⁽¹⁾	YZV	UNITS	
		4 PINS		
θ_{JA}	Junction-to-ambient thermal resistance	189.1		
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.9		
θ_{JB}	Junction-to-board thermal resistance	36.8	90044	
ΨЈТ	Junction-to-top characterization parameter	11.3	°C/W	
ΨЈВ	Junction-to-board characterization parameter	36.8		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a		

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

⁽³⁾ In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: TA_(max) = T_{J(max)} – (θ_{JA} × P_{D(max)})



RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.4	5.5	V
V _{ON}	ON voltage range		0	5.5	V
V _{OUT}	Output voltage range		0	V _{IN}	V
.,	High-level input voltage, ON	V _{IN} = 3.61 V to 5.5 V	1.1	5.5	
V _{IH}		V _{IN} = 1.4 V to 3.6V	1.1	5.5	V
.,	Landard Constant and Con-	V _{IN} = 3.61 V to 5.5 V	0	0.6	.,
V_{IL}	Low-level input voltage, ON	V _{IN} = 1.4 V to 3.6V	0	0.4	V
C _{IN}	Input capacitor		1(1)		μF

⁽¹⁾ Refer to Application Information section.

ELECTRICAL CHARACTERISTICS

Unless otherwise note, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_{A} \leq 85^{\circ}\text{C}$ (Full). Typical values are for $T_{A} = 25^{\circ}\text{C}$.

	PARAMETER	TEST CONDITIONS	T _A	MIN TYP	MAX	UNIT
POWER SUF	PPLIES AND CURRENTS					
		$I_{OUT} = 0$, $V_{IN} = V_{ON} = 5.25V$		2.3	10	
		$I_{OUT} = 0$, $V_{IN} = V_{ON} = 4.2V$		2.2	7	
I _{IN}	Quiescent current	$I_{OUT} = 0$, $V_{IN} = V_{ON} = 3.6V$	Full	2.1	7	μΑ
		$I_{OUT} = 0, V_{IN} = V_{ON} = 2.5V$		1.0	5	
		$I_{OUT} = 0, V_{IN} = V_{ON} = 1.5V$		0.8	5	
		V _{OUT} = Open, V _{IN} = 5.25V, V _{ON} = 0V		0.3	10	
		$V_{OUT} = Open, V_{IN} = 4.2V, V_{ON} = 0V$		0.2	7	μΑ
I _{IN(off)}	Off supply current	$V_{OUT} = Open, V_{IN} = 3.6V, V_{ON} = 0V$	Full	0.2	7	
		$V_{OUT} = Open, V_{IN} = 2.5V, V_{ON} = 0V$		0.1	5	
		$V_{OUT} = Open, V_{IN} = 1.5V, V_{ON} = 0V$		0.1	5	
		V _{OUT} = 0 V, V _{IN} = 5.25V, V _{ON} = 0V		0.8	10	
		$V_{OUT} = 0 \text{ V}, V_{IN} = 4.2 \text{V}, V_{ON} = 0 \text{V}$		0.2	7	
I _{IN(leak)}	Leakage current	$V_{OUT} = 0 \text{ V}, V_{IN} = 3.6 \text{V}, V_{ON} = 0 \text{V}$	Full	0.2	7	'
		$V_{OUT} = 0 \text{ V}, V_{IN} = 2.5 \text{V}, V_{ON} = 0 \text{V}$		0.1	5	
		$V_{OUT} = 0 \text{ V}, V_{IN} = 1.5 \text{V}, V_{ON} = 0 \text{V}$		0.1	5	
I _{ON}	ON pin input leakage current	V _{ON} = 5.5V	Full		0.5	
I _{RCP(leak)}	Reverse leakage current	$V_{IN} = V_{ON} = GND, V_{OUT} = 5V,$ measured from V_{IN}	Full		2	μA
111/10	Llador voltaga lagissis	V _{IN} increasing, VON = 3.6V, IOUT = -100mA	E. II		1.2	
UVLO	Under voltage lockout	V _{IN} decreasing, VON = 3.6V, IOUT = -100mA	Full	0.5		



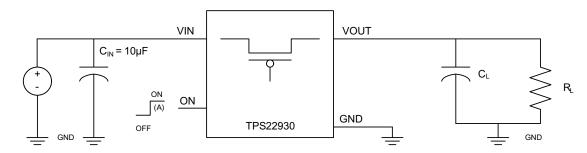
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise note, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 85^{\circ}\text{C}$ (Full). Typical values are for $\text{T}_{\text{A}} = 25^{\circ}\text{C}$.

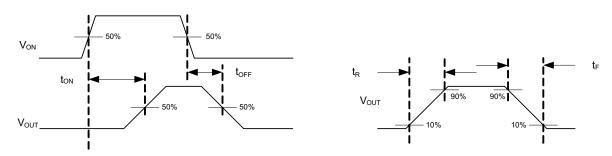
	PARAMETER	TEST CONDITIO	NS	T _A	MIN	TYP	MAX	UNIT
RESISTAN	CE CHARACTERISTICS							
			V 50V	25°C		35	44	
			$V_{IN} = 5.0 \text{ V}$	Full			50	
			V 42V	25°C		35	44	
			$V_{IN} = 4.2 \text{ V}$	Full			50	
		I _{OUT} = -200mA	V _{IN} = 3.6 V	25°C		36	44	mΩ
D	ON state resistance			Full			50	
R _{ON}	ON-state resistance		V 0.5.V	25°C		39	44	
			$V_{IN} = 2.5 \text{ V}$	Full			50	
			V 40V	25°C		49	55	
			V _{IN} = 1.8 V	Full			62	
			., , , , , , , , , , , , , , , , , , ,	25°C		59	66	
			V _{IN} = 1.5 V	Full			74	



SWITCHING CHARACTERISTIC MEASUREMENT INFORMATION



TEST CIRCUIT



ton/toff WAVEFORMS

(A) Rise and fall times of the control signal are 100ns.

Figure 2. Test Circuit and $t_{\text{ON}}/t_{\text{OFF}}$ Waveforms

SWITCHING CHARACTERISTICS

	PARAMETER	TEST CONDITION	MIN TYP MAX	UNIT
V _{IN} = 5	5.5 V, T _A = 25°C (unless oth	nerwise noted)	·	
t _{ON}	Turn-on time		4.8	
t _{OFF}	Turn-off time	D 400 C 04.15	6.3	
t _R	V _{OUT} rise time	$R_L = 10\Omega$, $C_L = 0.1\mu$ F	5.6	μs
t _F	V _{OUT} fall time		2.8	
V _{IN} = 4	1.2 V, T _A = 25°C (unless oth	nerwise noted)	·	
t _{ON}	Turn-on time		5.8	
t _{OFF}	Turn-off time	D 400 C 04.15	7.3	
t _R	V _{OUT} rise time	$R_L = 10\Omega$, $C_L = 0.1\mu$ F	5.4	μs
t_{F}	V _{OUT} fall time		2.8	
$V_{IN} = 3$	3.0 V, T _A = 25°C (unless oth	nerwise noted)	·	
t _{ON}	Turn-on time		7.4	
t _{OFF}	Turn-off time	D 400 0 0405	9.5	
t _R	V _{OUT} rise time	$R_L = 10\Omega$, $C_L = 0.1\mu$ F	6.3	μs
t _F	V _{OUT} fall time		2.9	

TEXAS INSTRUMENTS

FUNCTIONAL BLOCK DIAGRAM

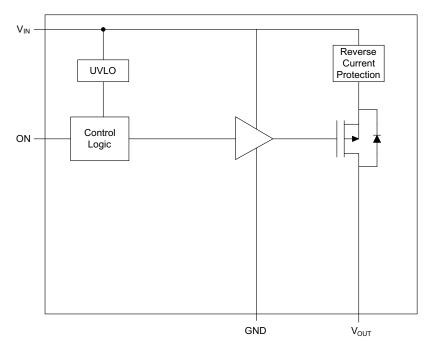


Figure 3. Functional Block Diagram

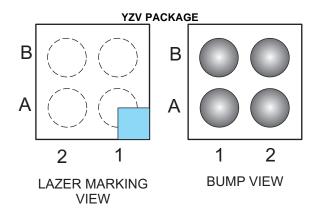


Table 1. TERMINAL ASSIGNMENTS

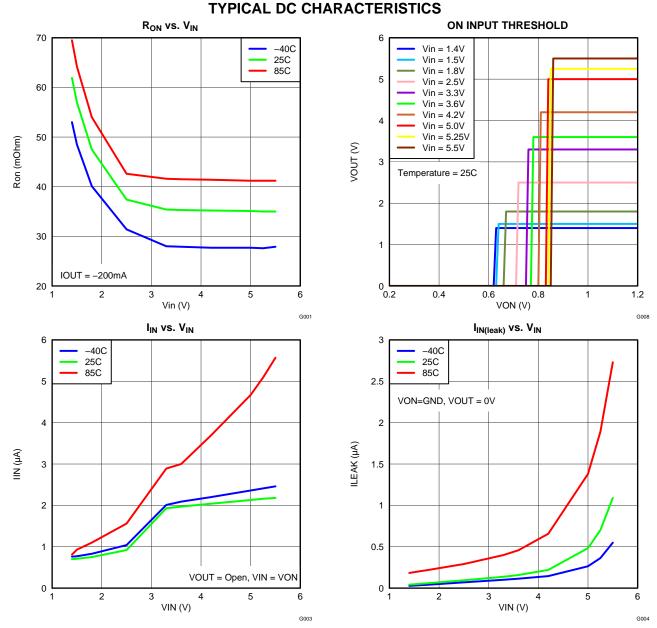
В	ON	GND
Α	VIN	VOUT
	2	1

PIN DESCRIPTIONS

TPS22930	PIN NAME	1/0	DESCRIPTION		
YZV	PIN NAME I/O		DESCRIPTION		
A1	VOUT	0	Switch output.		
A2	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V _{IN} dip during transients.		
B1	GND	_	Device ground.		
B2	ON	I	Switch control input, active high. Do no leave floating.		

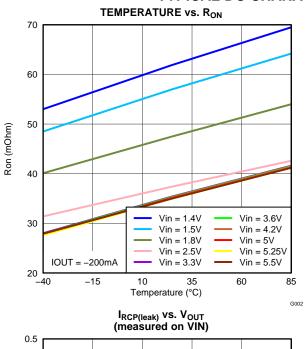


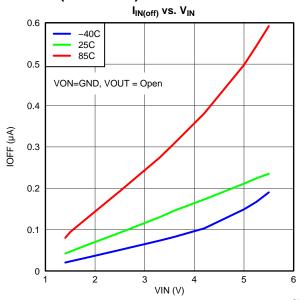
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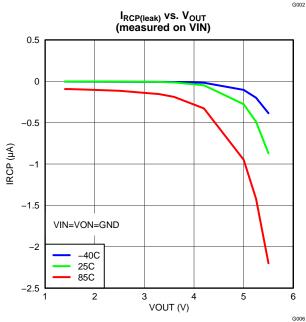


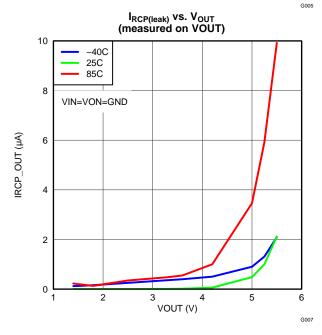




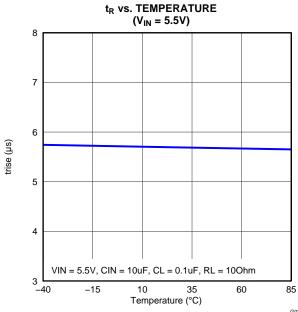


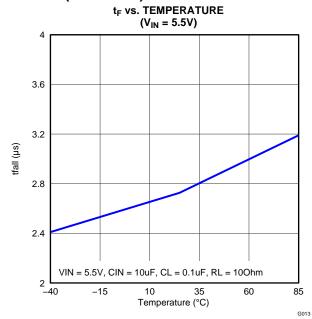


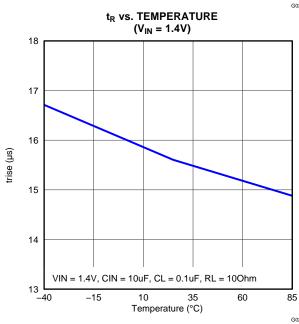


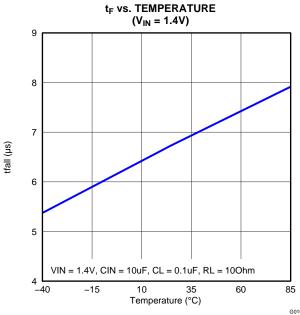




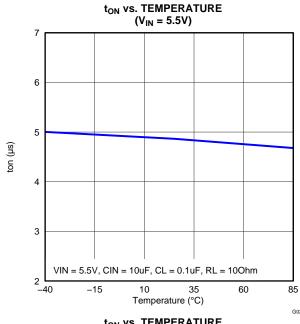


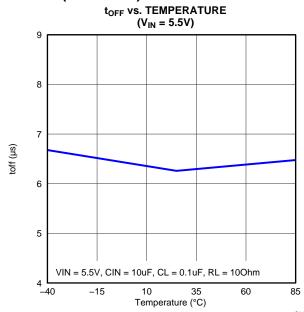


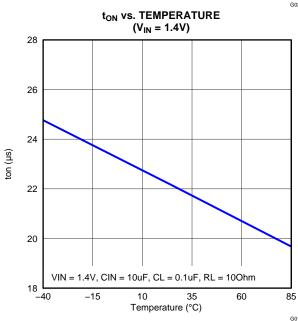


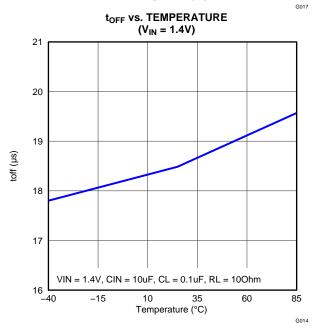


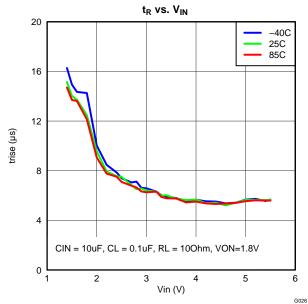


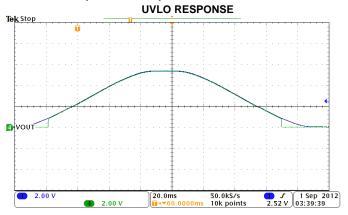


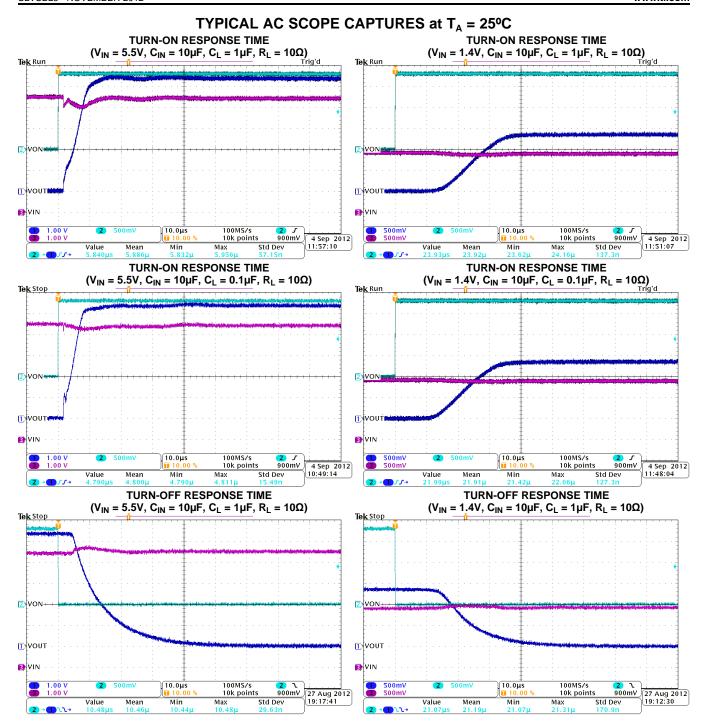






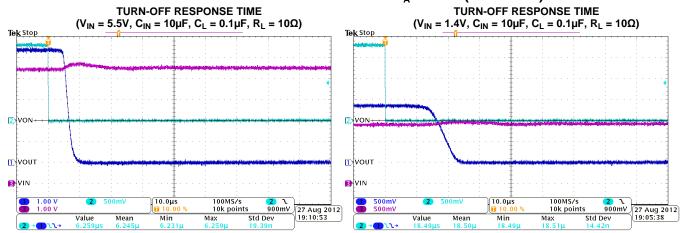








TYPICAL AC SCOPE CAPTURES at T_A = 25°C (continued)





APPLICATION INFORMATION

ON/OFF CONTROL

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

INPUT CAPACITOR (OPTIONAL)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, it is recommended that a capacitor be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 100 times higher than the output capacitor to avoid excessive voltage drop; however, a 100 to 1 ratio is not required for proper functionality of the device.

OUTPUT CAPACITOR (OPTIONAL)

Due to the integrated body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 100 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 100 to 1 ratio is not required for proper functionality of the device.

UNDER VOLTAGE LOCKOUT

Under voltage lockout protection turns off the switch if the input voltage drops below the under voltage lockout threshold. With the ON pin active, the input voltage rising above the under voltage lockout threshold will allow a controlled turn-on of the switch to limit current over-shoot.

REVERSE CURRENT PROTECTION

Reverse current protection (RCP) is only active when ON is asserted low. When ON is asserted high, current can flow from VOUT to VIN or from VIN to VOUT. This allows the device to function as a bi-directional switch when enabled.

BOARD LAYOUT AND THERMAL CONSIDERATIONS

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 125° C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_{A}}{\Theta_{JA}} \tag{1}$$

Where:

P_{D(max)} = maximum allowable power dissipation

T_{J(max)} = maximum allowable junction temperature (125°C for the TPS22930)

 T_A = ambient temperature of the device

 Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The power dissipated by the device depends on the R_{ON} of the device at a given V_{IN} . To calculate the amount of power being dissipated by the device, use the following equation:

$$P_{IR} = I^2 \times R_{ON} \tag{2}$$

Where:

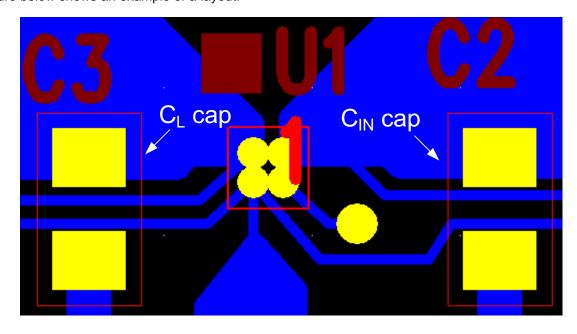
 P_{IR} = power dissipated by the device

I = load current in amperes

R_{ON} = resistance of the device in Ohms at a given V_{IN} (see Electrical Characteristics section)

The result from Equation 2 should always be less than or equal to the result from Equation 1.

The figure below shows an example of a layout.







1-Dec-2012

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Samples
	(1)		Drawing			(2)		(3)	(Requires Login)
TPS22930AYZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TPS22930AYZVT	ACTIVE	DSBGA	YZV	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22930AYZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1
TPS22930AYZVT	DSBGA	YZV	4	250	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1

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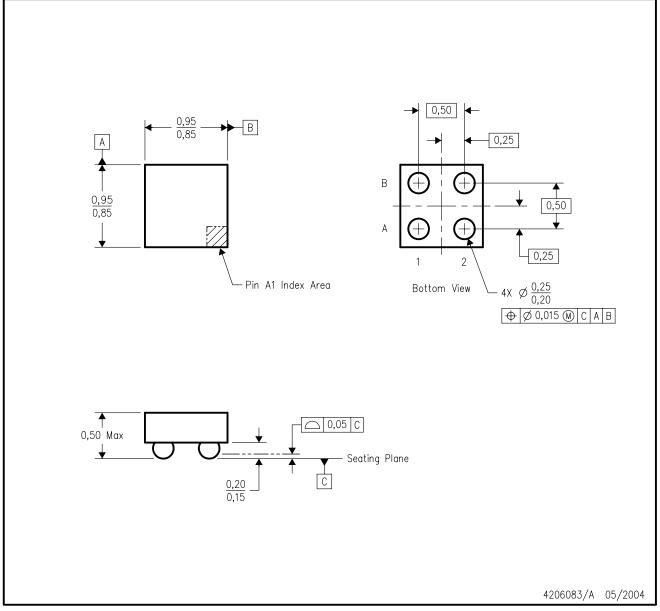


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22930AYZVR	DSBGA	YZV	4	3000	210.0	185.0	35.0
TPS22930AYZVT	DSBGA	YZV	4	250	210.0	185.0	35.0

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. NanoFree $^{\text{TM}}$ package configuration.
- D. This package contains lead—free balls. Refer to the 4 YEV package (drawing 4206082) for tin—lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.



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