

# 256-TAPS DUAL CHANNEL DIGITAL POTENTIOMETER WITH NON-VOLATILE MEMORY

Check for Samples: [TPL0102](#)

## FEATURES

- Dual Channel, 256-Position Resolution
- Non-volatile Memory Stores Wiper Settings
- 2mm x 2mm, 14-pin MicroQFN or 14-pin TSSOP Packages
- 100 k $\Omega$  End-to-End Resistance (TPL0102-100)
- Fast Power-up Response Time to Wiper Setting: <100 $\mu$ s
- $\pm 0.5$  LSB INL,  $\pm 0.25$  LSB DNL (Voltage-Divider Mode)
- 4 ppm/ $^{\circ}$ C Ratiometric Temperature Coefficient
- I<sup>2</sup>C-compatible Serial Interface
- 2.7 V to 5.5 V Single-Supply Operation
- $\pm 2.25$  V to  $\pm 2.75$  V Dual-Supply Operation
- Operating Temperature Range From -40 $^{\circ}$ C to +85 $^{\circ}$ C
- ESD Performance Tested Per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)

## APPLICATIONS

- Adjustable Gain Amplifiers and Offset Trimming
- Adjustable Power Supplies
- Precision Calibration of Set Point Thresholds
- Sensor Trimming and Calibration
- Mechanical Potentiometer Replacement

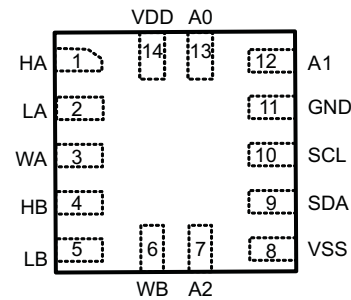
## DESCRIPTION

The TPL0102 is a two channel, linear-taper digital potentiometer with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0102-100 has an end-to-end resistance of 100k $\Omega$ .

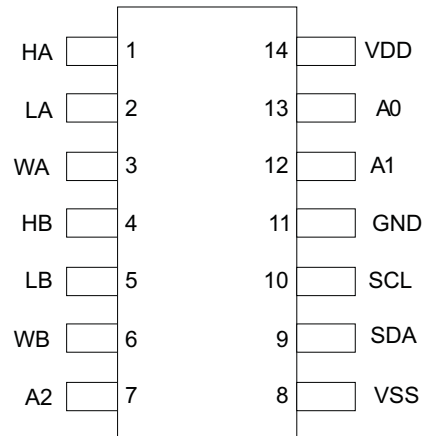
The TPL0102 has non-volatile memory (EEPROM) which can be used to store the wiper position. The internal registers of the TPL0102 can be accessed using the I<sup>2</sup>C interface.

The TPL0102 is available in a 14-pin MicroQFN and 14-pin TSSOP package with a specified temperature range of -40 $^{\circ}$ C to +85 $^{\circ}$ C.

MicroQFN - RUC PACKAGE  
(TOP VIEW)



TSSOP - PW PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup> (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tape and reel	TPL0102-100PWR	EL-100
	MicroQFN-RUC		TPL0102-100RUCR	6N

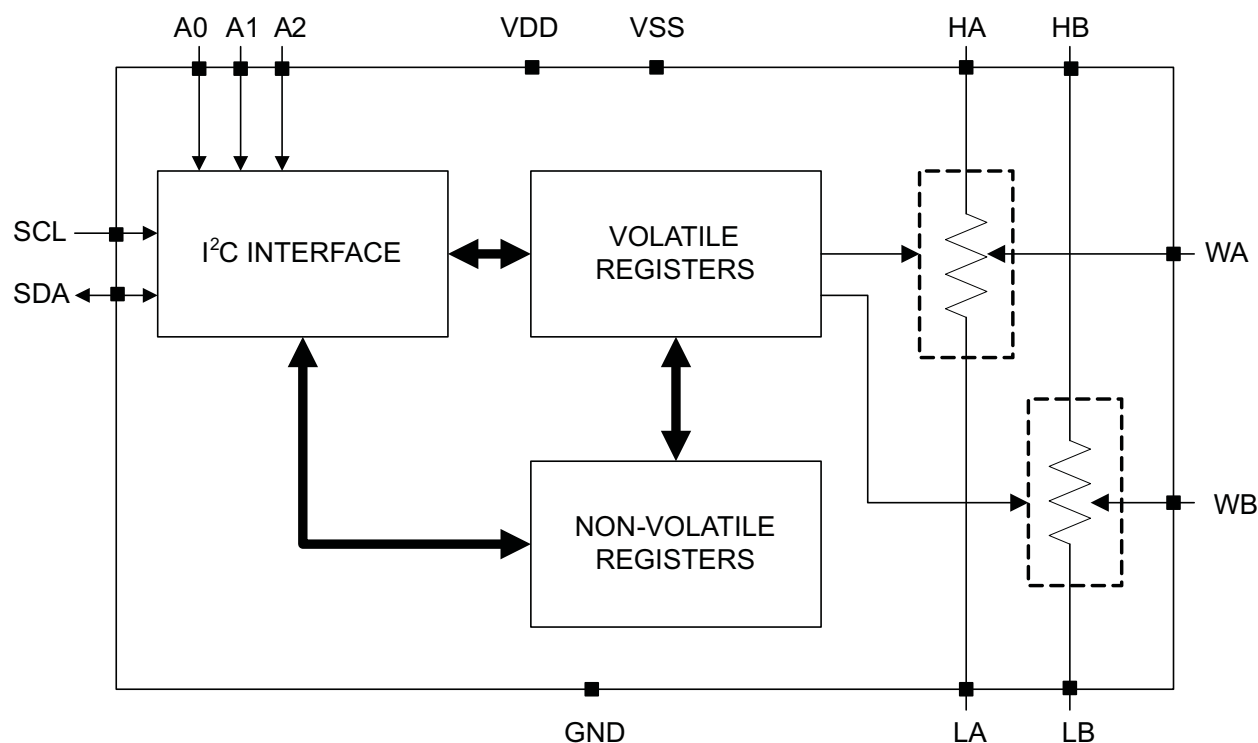
(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**Table 1. Summary of Features**

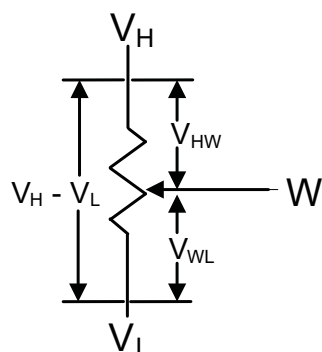
Feature	TPL0102-100
# of Potentiometers	2
Digital Interface	I <sup>2</sup> C
Steps	256
Wiper Memory	Non-Volatile
Taper	Linear
End-to-end Resistance	100kΩ
End-to-end Resistance Tolerance	20%
Wiper Resistance	25 Ω (typ)
Smallest Package Size	MicroQFN (RUC): 4 mm <sup>2</sup>

## FUNCTIONAL BLOCK DIAGRAM



## DIGITAL POTENTIOMETER CONFIGURATIONS

### VOLTAGE DIVIDER MODE

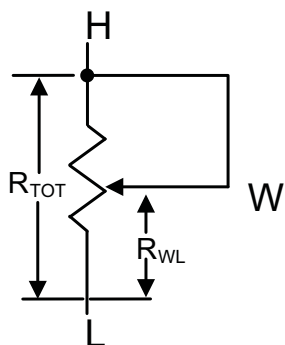


$$V_{HW} = (V_H - V_L) \times (1 - (D/256))$$

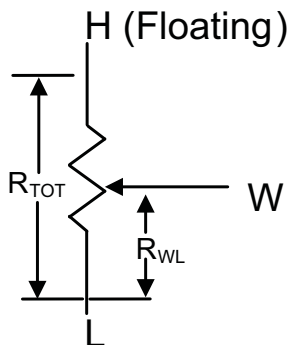
$$V_{WL} = (V_H - V_L) \times D/256$$

Where D = Decimal Value of Wiper Code

### RHEOSTAT MODE A



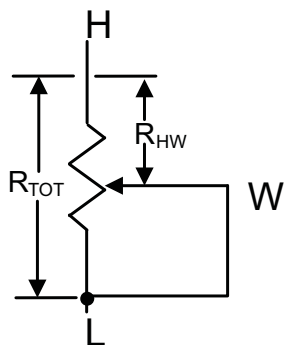
OR



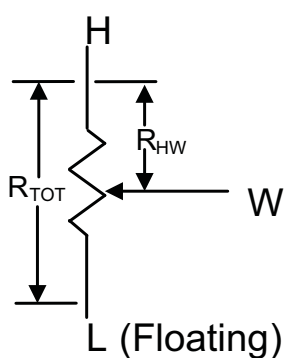
$$R_{WL} = R_{TOT} \times D/256$$

Where D = Decimal Value of Wiper Code

### RHEOSTAT MODE B



OR



$$R_{HW} = R_{TOT} \times (1 - (D/256))$$

Where D = Decimal Value of Wiper Code

**Figure 1. DPOT Configurations**

**Table 2. PIN DESCRIPTION TABLE**

14 RUC/14 PW	PIN NAME	TYPE	DESCRIPTION
1	HA	I/O	High terminal of Potentiometer A
2	LA	I/O	Low terminal of Potentiometer A
3	WA	I/O	Wiper terminal of Potentiometer A
4	HB	I/O	High terminal of Potentiometer B
5	LB	I/O	Low terminal of Potentiometer B
6	WB	I/O	Wiper terminal of Potentiometer B
7	A2	Input	Address Bit 2
8	VSS	Power	Negative or GND Power Supply Pin
9	SDA	I/O	I <sup>2</sup> C Data I/O
10	SCL	Input	I <sup>2</sup> C Clock Input
11	GND	Ground	Ground
12	A1	Input	Address Bit 1
13	A0	Input	Address Bit 0
14	VDD	Power	Positive Power Supply Pin

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{DD}, V_{SS}$	Single Supply Operation ( $V_{SS}=0V$ )	2.7	5.5	V
	Dual Supply Operation	$\pm 2.25$	$\pm 2.75$	
$V_H, V_L$	Terminal Voltage Range	$V_{SS}$	$V_{DD}$	V
$V_{IH}$	Voltage Input High (SCL, SDA, A0, A1, A2)	$0.7 \times V_{DD}$	5.5	V
$V_{IL}$	Voltage Input Low (SCL, SDA, A0, A1, A2)	0	$0.3 \times V_{DD}$	V
$I_W$	Wiper Current		$\pm 2$	mA
$T_A$	Ambient Temperature	-40	85	°C

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)(3)</sup>

		MIN	MAX	UNIT
$V_{DD}$ to GND	Supply voltage range	-0.3	7	V
$V_{SS}$ to GND		-7	0.3	V
$V_{DD}$ to $V_{SS}$			7	V
$V_H, V_L, V_W$	Voltage at resistor terminals	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
$V_I$	Digital input voltage range	-0.3	$V_{DD} + 0.3$	V
$I_H, I_L, I_W$	Pulse Current		$\pm 20$	mA
	Continuous Current		$\pm 2$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	PW package	88	°CW
		RUC package	216.7	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## ELECTRICAL CHARACTERISTICS

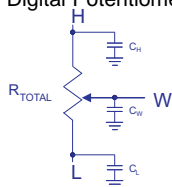
$V_{DD} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $V_H = V_{DD}$ ,  $V_L = GND$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted). Typical values are at  $V_{DD} = 5V$ ,  $T_A = 25^{\circ}C$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{TOT}$	End-to-end Resistance (Between H and L Terminals)	TPL0102-100	80	100	120	k $\Omega$
$R_H$ , $R_L$	Terminal resistance			60	200	$\Omega$
$R_W$	Wiper resistance			25	100	$\Omega$
$C_H$ , $C_L^{(1)(2)}$	Terminal capacitance			22		pF
$C_W^{(1)(2)}$	Wiper capacitance			16		pF
$I_{LKG}$	Terminal Leakage Current	$V_H = V_{SS}$ to $V_{DD}$ , $V_L =$ Floating OR $V_L = V_{SS}$ to $V_{DD}$ , $V_H =$ Floating		0.1	1	$\mu A$
$TC_R$	Resistance temperature coefficient	Input Code = 0x80h		92		ppm/ $^{\circ}C$
$R_{TOT,MATCH}$	Channel-to-channel resistance match			0.1		%
<b>Voltage Divider Mode</b>						
$INL^{(3)(4)}$	Integral non-linearity		-0.5		0.5	LSB
$DNL^{(3)(5)}$	Differential non-linearity		-0.25		0.25	LSB
$ZS_{ERROR}^{(6)(7)}$	Zero-scale error		0	0.1	2	LSB
$FS_{ERROR}^{(6)(8)}$	Full-scale error		-2	-0.1	0	LSB
$V_{MATCH}^{(6)(9)}$	Channel-to-Channel matching	Wiper at the same tap position, same voltage at all H and same voltage at all L terminals	-2		2	LSB
$TC_V$	Ratiometric temperature coefficient	Wiper set at mid-scale		4		ppm/ $^{\circ}C$
BW	Bandwidth	TPL0102-100 Wiper set at mid-scale $C_{LOAD} = 10$ pF		229		kHz
$T_{SW}$	Wiper setting time	TPL0102-100		3.6		$\mu S$
THD	Total harmonic distortion	$V_H = 1$ V <sub>RMS</sub> at 1 kHz, $V_L = (V_{DD} - V_{SS})/2$ , Measurement at W TPL0102-100		0.03		%
$X_{TALK}$	Cross talk	$f_H = 1$ kHz, $V_L = GND$ , Measurement at W		-82		dB

- (1) Terminal and Wiper Capacitance extracted from self admittance of three port network measurement

$$Y_{ii} = \frac{I_i}{V_i} \Big|_{V_k=0 \text{ for } k \neq i}$$

- (2) Digital Potentiometer Macromodel



- (3)  $LSB = (V_{MEAS}[\text{code } 255] - V_{MEAS}[\text{code } 0]) / 255$   
 (4)  $INL = ((V_{MEAS}[\text{code } x] - V_{MEAS}[\text{code } 0]) / LSB) - [\text{code } x]$   
 (5)  $DNL = ((V_{MEAS}[\text{code } x] - V_{MEAS}[\text{code } x-1]) / LSB) - 1$   
 (6)  $IDEAL\_LSB = (V_H - V_L) / 256$   
 (7)  $ZS_{ERROR} = V_{MEAS}[\text{code } 0] / IDEAL\_LSB$   
 (8)  $FS_{ERROR} = ((V_{MEAS}[\text{code } 255] - (V_H - V_L)) / IDEAL\_LSB) + 1$   
 (9)  $V_{MATCH} = (V_{MEAS\_A}[\text{code } x] - V_{MEAS\_B}[\text{code } x]) / IDEAL\_LSB$

## ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $V_H = V_{DD}$ ,  $V_L = GND$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted). Typical values are at  $V_{DD} = 5V$ ,  $T_A = 25^{\circ}C$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RHEOSTAT MODE (Measurements between W and L with H not connected, or between W and H with L not connected)							
RINL <sup>(10)(11)</sup>	Integral non-linearity			−1		1	LSB
RDNL <sup>(10)(12)</sup>	Differential non-linearity			−0.5		0.5	LSB
R <sub>OFFSET</sub> <sup>(13)(14)</sup>	Offset			0	0.2	2	LSB
R <sub>MATCH</sub> <sup>(13)(15)</sup>	Channel-to-Channel matching			−2		2	LSB
RBW	Bandwidth	Code = 0x00h, L Floating, Input applied to W, Measure at H, C <sub>LOAD</sub> = 10 pF	TPL0102-100		54		kHz

(10)  $RLSB = (R_{MEAS[code\ 255]} - R_{MEAS[code\ 0]}) / 255$

(11)  $RINL = ((R_{MEAS[code\ x]} - R_{MEAS[code\ 0]}) / RLSB) - [code\ x]$

(12)  $RDNL = ((R_{MEAS[code\ x]} - R_{MEAS[code\ x-1]}) / RLSB) - 1$

(13)  $IDEAL\_RLSB = R_{TOT} / 256$

(14)  $R_{OFFSET} = R_{MEAS[code\ 0]} / IDEAL\_RLSB$

(15)  $R_{MATCH} = (R_{MEAS\_A[code\ x]} - R_{MEAS\_B[code\ x]}) / IDEAL\_RLSB$

## OPERATING CHARACTERISTICS

$V_{DD} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $V_H = V_{DD}$ ,  $V_L = GND$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted). Typical values are at  $V_{DD} = 5V$ ,  $T_A = 25^{\circ}C$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>DD(STBY)</sub>	V <sub>DD</sub> standby current	V <sub>DD</sub> = 2.75 V, V <sub>SS</sub> = –2.75, I <sup>2</sup> C interface in standby mode			0.2	1	μA
I <sub>SS(STBY)</sub>	V <sub>SS</sub> standby current	V <sub>DD</sub> = 2.75 V, V <sub>SS</sub> = –2.75, I <sup>2</sup> C interface in standby mode	–1	–0.2			μA
I <sub>DD(SHUTDOWN)</sub>	V <sub>DD</sub> shutdown current	V <sub>DD</sub> = 2.75 V, V <sub>SS</sub> = –2.75, I <sup>2</sup> C interface in standby mode		0.2		1	μA
I <sub>SS(SHUTDOWN)</sub>	V <sub>SS</sub> shutdown current	V <sub>DD</sub> = 2.75 V, V <sub>SS</sub> = –2.75, I <sup>2</sup> C interface in standby mode	–1	–0.2			μA
I <sub>DD</sub>	V <sub>DD</sub> current during non-volatile write	V <sub>DD</sub> = 2.75 V, V <sub>SS</sub> = –2.75			200		μA
I <sub>SS</sub>	V <sub>SS</sub> current during non-volatile write	V <sub>DD</sub> = 2.75 V, V <sub>SS</sub> = –2.75	–200				μA
I <sub>LKG-DIG</sub>	Digital pins leakage current (A0, A1, A2, SDA, and SCL)		–1			1	μA
V <sub>POR</sub>	Power-on recall voltage	Minimum V <sub>DD</sub> at which memory recall occurs			2		V

### EEPROM Specification

	EEPROM endurance			100,000		Cycles
	EEPROM retention	T <sub>A</sub> = 85°C		100		Years
t <sub>WC</sub>	Non-volatile write cycle time			20		ms

### Wiper Timing Characteristics

t <sub>WRT</sub>	Wiper response time	SCL falling edge of last bit of wiper data byte to wiper new position		600		ns
t <sub>SHUTDOWNREC</sub>	Wiper position recall time from shut-down mode	SCL falling edge of last bit of ACR data byte to wiper stored position and H connection		800		ns
t <sub>D</sub>	Power-up delay	V <sub>DD</sub> above V <sub>POR</sub> , to wiper initial value register recall completed, and I <sup>2</sup> C interface in standby mode		35	100	μs
C <sub>IN</sub>	Pin capacitance	A0, A1, A2, SDA SCL pins		7		pF

## OPERATING CHARACTERISTICS (continued)

$V_{DD} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $V_H = V_{DD}$ ,  $V_L = GND$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted). Typical values are at  $V_{DD} = 5V$ ,  $T_A = 25^{\circ}C$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>I<sup>2</sup>C Interface Specifications</b>						
$V_{IH}$	Input high voltage		$0.7 \times V_{DD}$		5.5	V
$V_{IL}$	Input low voltage		0		$0.3 \times V_{DD}$	V
$V_{OL}$	Output low voltage	SDA pin, $I_{OL} = 4\text{ mA}$			0.4	V
$C_{IN}$	Pin capacitance	A0, A1, A2, SDA SCL pins		7		pF

## TIMING REQUIREMENTS

$V_{DD} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $V_H = V_{DD}$ ,  $V_L = GND$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted). Typical values are at  $V_{DD} = 5V$ ,  $T_A = 25^{\circ}C$  (unless otherwise noted).

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
<b>I<sup>2</sup>C Interface Timing Requirements</b>						
$f_{SCL}$	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
$t_{SCH}$	I <sup>2</sup> C clock high time	4		0.6		$\mu s$
$t_{SCL}$	I <sup>2</sup> C clock low time	4.7		1.3		$\mu s$
$t_{sp}$	I <sup>2</sup> C spike time	0	50	0	50	ns
$t_{SDS}$	I <sup>2</sup> C serial data setup time	250		100		ns
$t_{SDH}$	I <sup>2</sup> C serial data hold time	0		0		ns
$t_{ICR}$	I <sup>2</sup> C input rise time		1000	$20 + 0.1C_b^{(1)}$	300	ns
$t_{ICF}$	I <sup>2</sup> C input fall time		300	$20 + 0.1C_b^{(1)}$	300	ns
$t_{ICF}$	I <sup>2</sup> C output fall time, 10 pF to 400 pF bus		300	$20 + 0.1C_b^{(1)}$	300	ns
$t_{BUF}$	I <sup>2</sup> C bus free time between stop and start	4.7		1.3		$\mu s$
$t_{STS}$	I <sup>2</sup> C start or repeater start conditions setup time	4.7		1.3		$\mu s$
$t_{STH}$	I <sup>2</sup> C start or repeater start condition hold time	4		0.6		$\mu s$
$t_{SPS}$	I <sup>2</sup> C stop condition setup time	4		0.6		$\mu s$
$t_{VD(DATA)}$	Valid data time, SCL low to SDA output valid		1		1	$\mu s$
$t_{VD(DATA)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1		1	$\mu s$

(1)  $C_b$  = total capacitance of one bus line in pF



## REGISTER DESCRIPTION

### Slave Address

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
1	0	1	0	A2	A1	A0	R/W

### TPL0102 Register Map

REGISTER ADDRESS (HEX)	NON-VOLATILE	VOLATILE
0	IVRA	WRA
1	IVRB	WRB
2	General purpose	N/A
3	General purpose	N/A
4	General purpose	N/A
5	General purpose	N/A
6	General purpose	N/A
7	General purpose	N/A
8	General purpose	N/A
9	General purpose	N/A
A	General purpose	N/A
B	General purpose	N/A
C	General purpose	N/A
E	General purpose	N/A
D	General purpose	N/A
F	Reserved	
10	N/A	ACR

### IVRA (Initial Value Register for Potentiometer A)

- Register Address: 00H
- Factory Programmed Value: 80H
- Type: Non-volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION
IVRA	8	Non-volatile register to store wiper position for potentiometer A

### WRA (Wiper Resistance Register for Potentiometer A)

- Register Address: 00H
- Reset Value: Same as IVRA
- Type: Volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION
WRA	8	Volatile register to change wiper position for potentiometer A

### IVRB (Initial Value Register for Potentiometer B)

- Register Address: 01H
- Factory Programmed Value: 80H
- Type: Non-volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION
IVRB	8	Non-volatile register to store wiper position for potentiometer B

### WRB (Wiper Resistance Register for Potentiometer B)

- Register Address: 01H
- Reset Value: Same as IVRB
- Type: Volatile Write/Read

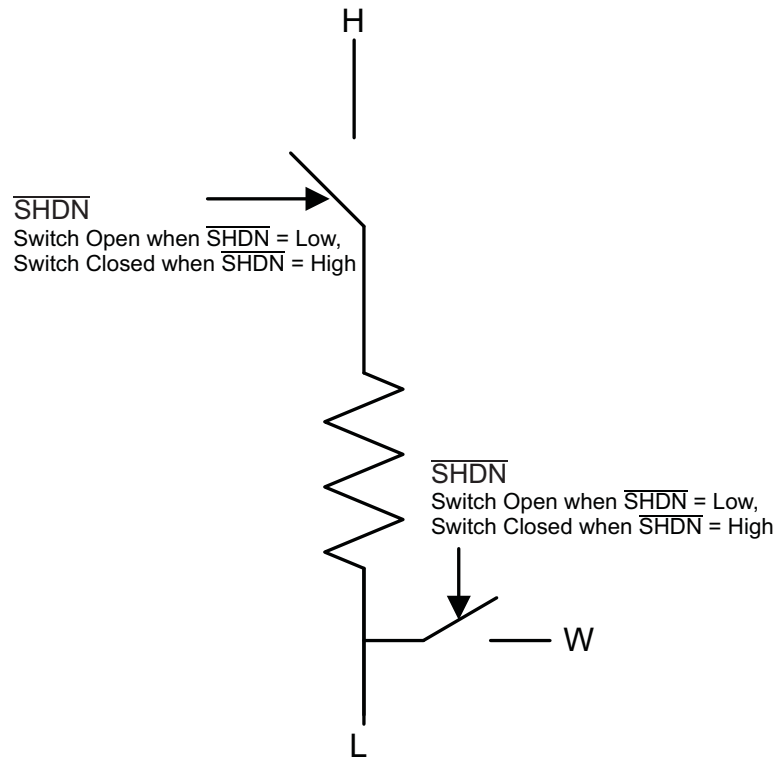
NAME	SIZE (BITS)	DESCRIPTION
WRB	8	Volatile register to change wiper position for potentiometer B

### ACR (Access Control Register)

- Register Address: 00H
- Reset Value: 40H
- Type: Non-volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION							
IVRA	8	Non-volatile register to store wiper position for potentiometer A							
ACR	8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		VOL	$\overline{\text{SHDN}}$	WIP	0	0	0	0	0
Default Value		0	1	0	0	0	0	0	0

NAME	SIZE (BITS)	DESCRIPTION
VOL	1	0: Non-volatile registers (IVRA, IVRB) are accessible. Value written to IVRi register is also written to the corresponding WRi.
		1: Only Volatile Registers (WRi) are accessible.
$\overline{\text{SHDN}}$	1	0: Shut-down mode is enabled. Potentiometers are in shut-down mode. (see <a href="#">Figure 2</a> )
		1: Shut-down mode is disabled
WIP (Read-only bit)	1	0: Non-volatile write operation is not in progress
		1: Non-volatile write operation is in progress (it is not possible to write to the WRi or ACR while WIP = 1)



**Figure 2. Potentiometer in Shut-Down Mode**

## PRINCIPLES OF OPERATION

The TPL0102 is a two channel, linear-taper digital potentiometer with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0102-100 has an end-to-end resistance of 100k $\Omega$ .

The TPL0102 has non-volatile memory (EEPROM) which can be used to store the wiper position. When the device is powered down, the last value stored in the IVR register will be maintained in the non-volatile memory. When power is restored, the contents of the IVR register are recalled and loaded into the corresponding WR register to set the wipers to the initial position. The internal registers of the TPL0102 can be accessed using the I<sup>2</sup>C interface.

The position of the wiper terminal is controlled by the value in the WR 8-bit register. When the WR contains all zeroes, the wiper terminal W is closest to its L (Low) terminal. As the value of the WR increases from all zeroes to all ones (255 decimal), the wiper moves monotonically from the position closest to L to the position closest to H. At the same time, the resistance between W and L increases monotonically, whereas the resistance between W and H decreases monotonically.

### Potentiometer Pin Description

#### HA,HB,LA,LB

The high (HA, HB) and low (LA, LB) terminals of the TPL0102 are equivalent to the fixed terminals of a mechanical potentiometer. The H and L terminals do not have any polarity restrictions, i.e. H can be at a higher voltage than L, or L can be at a higher voltage than H. The WA and WB terminals are the wipers and equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper is set using the WR register. With the WR register set to 255 decimal, the wiper is closest to the H terminal, and with the WR register set to 0, the wiper is closest to the L terminal.

#### SDA, SCL

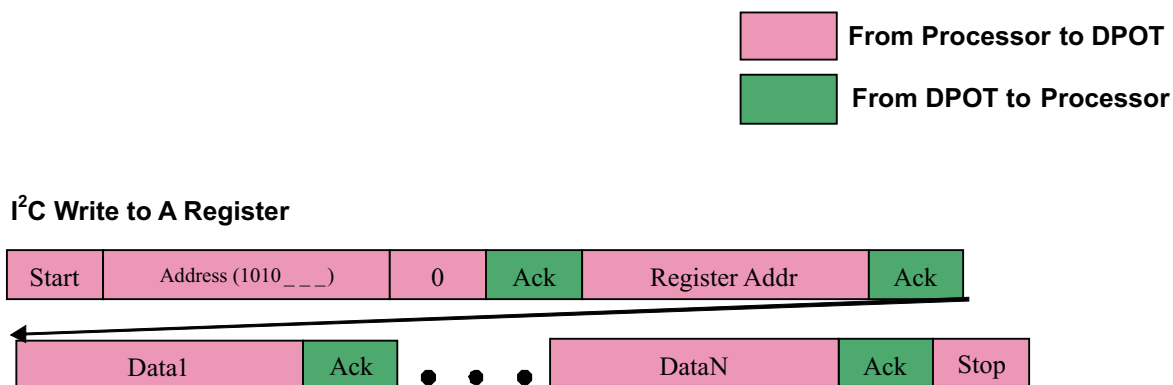
SDA is a bi-directional serial data input/output pin for I<sup>2</sup>C communication. SDA is an open drain output and requires an external pull-up resistor.

SCL is the serial clock input for I<sup>2</sup>C communication. SCL requires an external pull-up resistor.

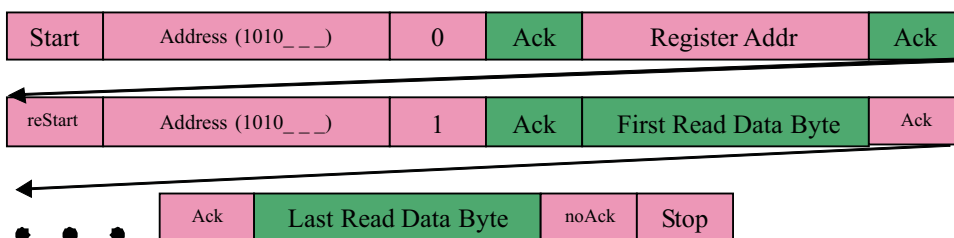
#### A0, A1, A2

These inputs are used to set the last three bits of the I<sup>2</sup>C address of the device. By using different values for A0, A1, A2, up to eight TPL0102 devices can be used on the same I<sup>2</sup>C bus.

**Figure 3. I<sup>2</sup>C Interface**

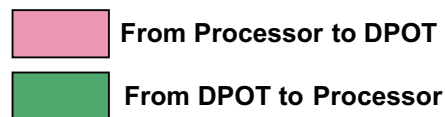


**I<sup>2</sup>C Read From A Register**

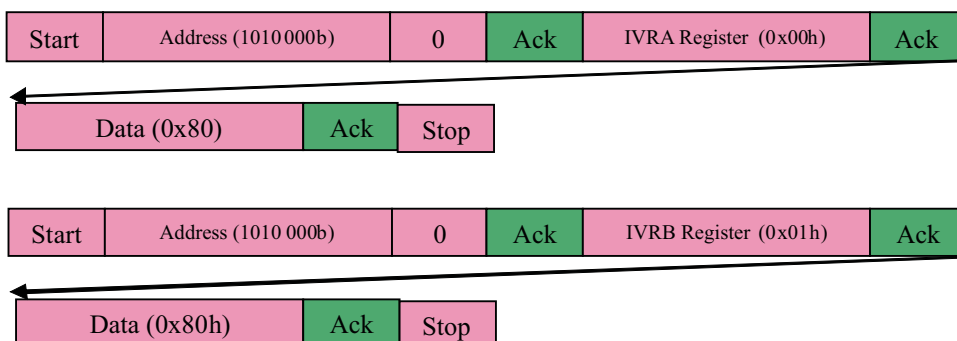


**Figure 4. I<sup>2</sup>C Interface**

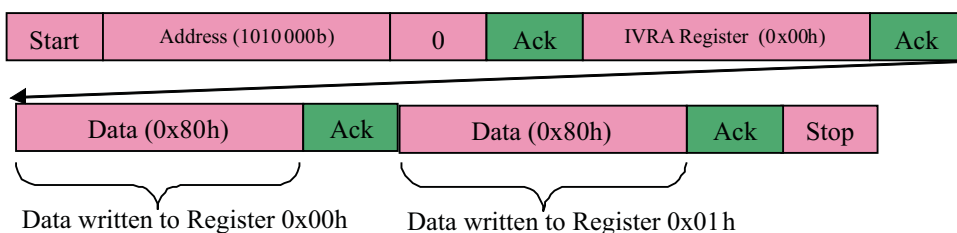
Following is a sample sequence to set wipers of both potentiometers at mid-scale. Assume A0, A1, and A2 are zero and device has just been powered up.



**Method 1: First Write 0x80 to IVRA and then write 0x80 to IVRB Register**



**Method 2: Perform a multi byte write to IVRA and IVRB Register**

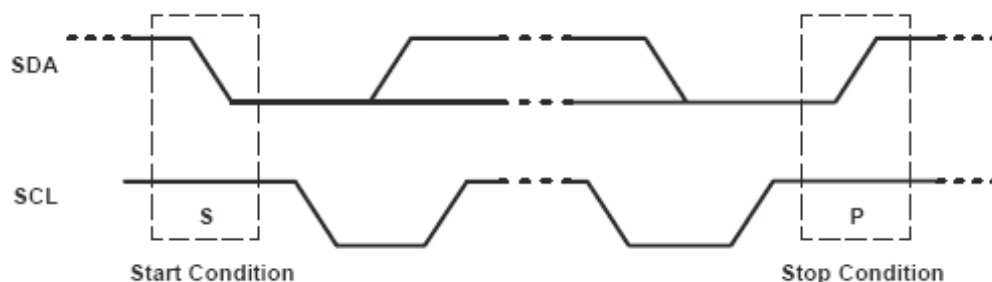


**Figure 5. I<sup>2</sup>C Interface Example**

## Standard I<sup>2</sup>C Interface Details

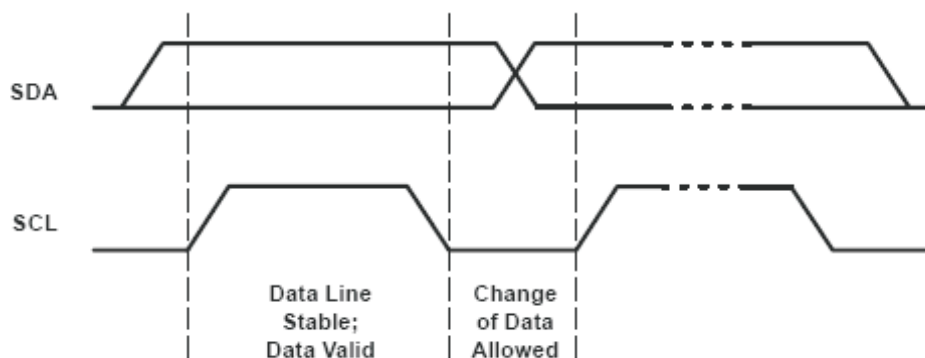
The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by the master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 6). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse



**Figure 6. Definition of Start and Stop Conditions**

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK. On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 7).

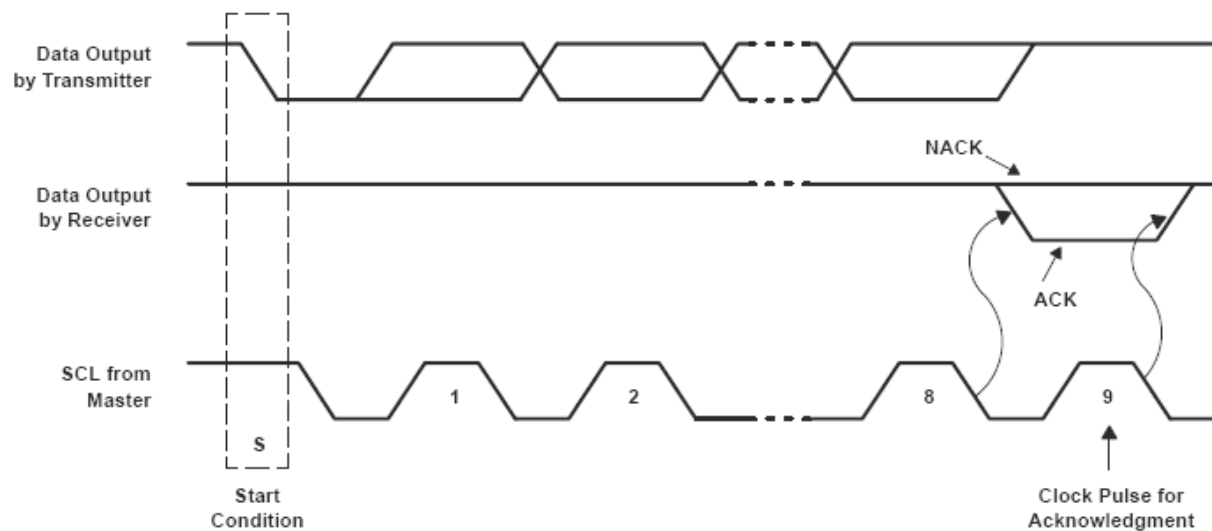


**Figure 7. Bit Transfer**

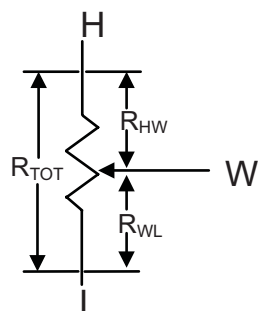
A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 6).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 8). Setup and hold times must be taken into account.

Figure 8. Acknowledgment on the I<sup>2</sup>C Bus

## IDEAL RESISTANCE VALUES



$$R_{WL} = R_{TOT} \times D/256$$

$$R_{HW} = R_{TOT} \times (1 - (D/256))$$

Where D = Decimal Value of Wiper Code

Below table shows the ideal values for DPOT with end-to-end resistance of 100kΩ. The absolute values of resistance can vary significantly but the Ratio ( $R_{HW}/R_{WL}$ ) is extremely accurate.

Step	Binary	$R_{HW}$ (kΩ)	$R_{WL}$ (kΩ)	$R_{HW}/R_{WL}$
0	0	0.00	100.00	0.00
1	1	0.39	99.61	0.00
2	10	0.78	99.22	0.01
3	11	1.17	98.83	0.01
4	100	1.56	98.44	0.02
5	101	1.95	98.05	0.02
6	110	2.34	97.66	0.02
7	111	2.73	97.27	0.03
8	1000	3.13	96.88	0.03
9	1001	3.52	96.48	0.04
10	1010	3.91	96.09	0.04
11	1011	4.30	95.70	0.04
12	1100	4.69	95.31	0.05
13	1101	5.08	94.92	0.05
14	1110	5.47	94.53	0.06
15	1111	5.86	94.14	0.06



Step	Binary	R <sub>HW</sub> (kΩ)	R <sub>WL</sub> (kΩ)	R <sub>HW</sub> /R <sub>WL</sub>
16	10000	6.25	93.75	0.07
17	10001	6.64	93.36	0.07
18	10010	7.03	92.97	0.08
19	10011	7.42	92.58	0.08
20	10100	7.81	92.19	0.08
21	10101	8.20	91.80	0.09
22	10110	8.59	91.41	0.09
23	10111	8.98	91.02	0.10
24	11000	9.38	90.63	0.10
25	11001	9.77	90.23	0.11
26	11010	10.16	89.84	0.11
27	11011	10.55	89.45	0.12
28	11100	10.94	89.06	0.12
29	11101	11.33	88.67	0.13
30	11110	11.72	88.28	0.13
31	11111	12.11	87.89	0.14
32	100000	12.50	87.50	0.14
33	100001	12.89	87.11	0.15
34	100010	13.28	86.72	0.15
35	100011	13.67	86.33	0.16
36	100100	14.06	85.94	0.16
37	100101	14.45	85.55	0.17
38	100110	14.84	85.16	0.17
39	100111	15.23	84.77	0.18
40	101000	15.63	84.38	0.19
41	101001	16.02	83.98	0.19
42	101010	16.41	83.59	0.20
43	101011	16.80	83.20	0.20
44	101100	17.19	82.81	0.21
45	101101	17.58	82.42	0.21
46	101110	17.97	82.03	0.22
47	101111	18.36	81.64	0.22
48	110000	18.75	81.25	0.23
49	110001	19.14	80.86	0.24
50	110010	19.53	80.47	0.24
51	110011	19.92	80.08	0.25
52	110100	20.31	79.69	0.25
53	110101	20.70	79.30	0.26
54	110110	21.09	78.91	0.27
55	110111	21.48	78.52	0.27
56	111000	21.88	78.13	0.28
57	111001	22.27	77.73	0.29
58	111010	22.66	77.34	0.29
59	111011	23.05	76.95	0.30
60	111100	23.44	76.56	0.31
61	111101	23.83	76.17	0.31
62	111110	24.22	75.78	0.32
63	111111	24.61	75.39	0.33
64	1000000	25.00	75.00	0.33

Step	Binary	R <sub>HW</sub> (kΩ)	R <sub>WL</sub> (kΩ)	R <sub>HW</sub> /R <sub>WL</sub>
65	1000001	25.39	74.61	0.34
66	1000010	25.78	74.22	0.35
67	1000011	26.17	73.83	0.35
68	1000100	26.56	73.44	0.36
69	1000101	26.95	73.05	0.37
70	1000110	27.34	72.66	0.38
71	1000111	27.73	72.27	0.38
72	1001000	28.13	71.88	0.39
73	1001001	28.52	71.48	0.40
74	1001010	28.91	71.09	0.41
75	1001011	29.30	70.70	0.41
76	1001100	29.69	70.31	0.42
77	1001101	30.08	69.92	0.43
78	1001110	30.47	69.53	0.44
79	1001111	30.86	69.14	0.45
80	1010000	31.25	68.75	0.45
81	1010001	31.64	68.36	0.46
82	1010010	32.03	67.97	0.47
83	1010011	32.42	67.58	0.48
84	1010100	32.81	67.19	0.49
85	1010101	33.20	66.80	0.50
86	1010110	33.59	66.41	0.51
87	1010111	33.98	66.02	0.51
88	1011000	34.38	65.63	0.52
89	1011001	34.77	65.23	0.53
90	1011010	35.16	64.84	0.54
91	1011011	35.55	64.45	0.55
92	1011100	35.94	64.06	0.56
93	1011101	36.33	63.67	0.57
94	1011110	36.72	63.28	0.58
95	1011111	37.11	62.89	0.59
96	1100000	37.50	62.50	0.60
97	1100001	37.89	62.11	0.61
98	1100010	38.28	61.72	0.62
99	1100011	38.67	61.33	0.63
100	1100100	39.06	60.94	0.64
101	1100101	39.45	60.55	0.65
102	1100110	39.84	60.16	0.66
103	1100111	40.23	59.77	0.67
104	1101000	40.63	59.38	0.68
105	1101001	41.02	58.98	0.70
106	1101010	41.41	58.59	0.71
107	1101011	41.80	58.20	0.72
108	1101100	42.19	57.81	0.73
109	1101101	42.58	57.42	0.74
110	1101110	42.97	57.03	0.75
111	1101111	43.36	56.64	0.77
112	1110000	43.75	56.25	0.78
113	1110001	44.14	55.86	0.79

Step	Binary	R <sub>HW</sub> (kΩ)	R <sub>WL</sub> (kΩ)	R <sub>HW</sub> /R <sub>WL</sub>
114	1110010	44.53	55.47	0.80
115	1110011	44.92	55.08	0.82
116	1110100	45.31	54.69	0.83
117	1110101	45.70	54.30	0.84
118	1110110	46.09	53.91	0.86
119	1110111	46.48	53.52	0.87
120	1111000	46.88	53.13	0.88
121	1111001	47.27	52.73	0.90
122	1111010	47.66	52.34	0.91
123	1111011	48.05	51.95	0.92
124	1111100	48.44	51.56	0.94
125	1111101	48.83	51.17	0.95
126	1111110	49.22	50.78	0.97
127	1111111	49.61	50.39	0.98
128	10000000	50.00	50.00	1.00
129	10000001	50.39	49.61	1.02
130	10000010	50.78	49.22	1.03
131	10000011	51.17	48.83	1.05
132	10000100	51.56	48.44	1.06
133	10000101	51.95	48.05	1.08
134	10000110	52.34	47.66	1.10
135	10000111	52.73	47.27	1.12
136	10001000	53.13	46.88	1.13
137	10001001	53.52	46.48	1.15
138	10001010	53.91	46.09	1.17
139	10001011	54.30	45.70	1.19
140	10001100	54.69	45.31	1.21
141	10001101	55.08	44.92	1.23
142	10001110	55.47	44.53	1.25
143	10001111	55.86	44.14	1.27
144	10010000	56.25	43.75	1.29
145	10010001	56.64	43.36	1.31
146	10010010	57.03	42.97	1.33
147	10010011	57.42	42.58	1.35
148	10010100	57.81	42.19	1.37
149	10010101	58.20	41.80	1.39
150	10010110	58.59	41.41	1.42
151	10010111	58.98	41.02	1.44
152	10011000	59.38	40.63	1.46
153	10011001	59.77	40.23	1.49
154	10011010	60.16	39.84	1.51
155	10011011	60.55	39.45	1.53
156	10011100	60.94	39.06	1.56
157	10011101	61.33	38.67	1.59
158	10011110	61.72	38.28	1.61
159	10011111	62.11	37.89	1.64
160	10100000	62.50	37.50	1.67
161	10100001	62.89	37.11	1.69
162	10100010	63.28	36.72	1.72

Step	Binary	R <sub>HW</sub> (kΩ)	R <sub>WL</sub> (kΩ)	R <sub>HW</sub> /R <sub>WL</sub>
163	10100011	63.67	36.33	1.75
164	10100100	64.06	35.94	1.78
165	10100101	64.45	35.55	1.81
166	10100110	64.84	35.16	1.84
167	10100111	65.23	34.77	1.88
168	10101000	65.63	34.38	1.91
169	10101001	66.02	33.98	1.94
170	10101010	66.41	33.59	1.98
171	10101011	66.80	33.20	2.01
172	10101100	67.19	32.81	2.05
173	10101101	67.58	32.42	2.08
174	10101110	67.97	32.03	2.12
175	10101111	68.36	31.64	2.16
176	10110000	68.75	31.25	2.20
177	10110001	69.14	30.86	2.24
178	10110010	69.53	30.47	2.28
179	10110011	69.92	30.08	2.32
180	10110100	70.31	29.69	2.37
181	10110101	70.70	29.30	2.41
182	10110110	71.09	28.91	2.46
183	10110111	71.48	28.52	2.51
184	10111000	71.88	28.13	2.56
185	10111001	72.27	27.73	2.61
186	10111010	72.66	27.34	2.66
187	10111011	73.05	26.95	2.71
188	10111100	73.44	26.56	2.76
189	10111101	73.83	26.17	2.82
190	10111110	74.22	25.78	2.88
191	10111111	74.61	25.39	2.94
192	11000000	75.00	25.00	3.00
193	11000001	75.39	24.61	3.06
194	11000010	75.78	24.22	3.13
195	11000011	76.17	23.83	3.20
196	11000100	76.56	23.44	3.27
197	11000101	76.95	23.05	3.34
198	11000110	77.34	22.66	3.41
199	11000111	77.73	22.27	3.49
200	11001000	78.13	21.88	3.57
201	11001001	78.52	21.48	3.65
202	11001010	78.91	21.09	3.74
203	11001011	79.30	20.70	3.83
204	11001100	79.69	20.31	3.92
205	11001101	80.08	19.92	4.02
206	11001110	80.47	19.53	4.12
207	11001111	80.86	19.14	4.22
208	11010000	81.25	18.75	4.33
209	11010001	81.64	18.36	4.45
210	11010010	82.03	17.97	4.57
211	11010011	82.42	17.58	4.69

Step	Binary	R <sub>HW</sub> (kΩ)	R <sub>WL</sub> (kΩ)	R <sub>HW</sub> /R <sub>WL</sub>
212	11010100	82.81	17.19	4.82
213	11010101	83.20	16.80	4.95
214	11010110	83.59	16.41	5.10
215	11010111	83.98	16.02	5.24
216	11011000	84.38	15.63	5.40
217	11011001	84.77	15.23	5.56
218	11011010	85.16	14.84	5.74
219	11011011	85.55	14.45	5.92
220	11011100	85.94	14.06	6.11
221	11011101	86.33	13.67	6.31
222	11011110	86.72	13.28	6.53
223	11011111	87.11	12.89	6.76
224	11100000	87.50	12.50	7.00
225	11100001	87.89	12.11	7.26
226	11100010	88.28	11.72	7.53
227	11100011	88.67	11.33	7.83
228	11100100	89.06	10.94	8.14
229	11100101	89.45	10.55	8.48
230	11100110	89.84	10.16	8.85
231	11100111	90.23	9.77	9.24
232	11101000	90.63	9.38	9.67
233	11101001	91.02	8.98	10.13
234	11101010	91.41	8.59	10.64
235	11101011	91.80	8.20	11.19
236	11101100	92.19	7.81	11.80
237	11101101	92.58	7.42	12.47
238	11101110	92.97	7.03	13.22
239	11101111	93.36	6.64	14.06
240	11110000	93.75	6.25	15.00
241	11110001	94.14	5.86	16.07
242	11110010	94.53	5.47	17.29
243	11110011	94.92	5.08	18.69
244	11110100	95.31	4.69	20.33
245	11110101	95.70	4.30	22.27
246	11110110	96.09	3.91	24.60
247	11110111	96.48	3.52	27.44
248	11111000	96.88	3.13	31.00
249	11111001	97.27	2.73	35.57
250	11111010	97.66	2.34	41.67
251	11111011	98.05	1.95	50.20
252	11111100	98.44	1.56	63.00
253	11111101	98.83	1.17	84.33
254	11111110	99.22	0.78	127.00
255	11111111	99.61	0.3	255.00

## REVISION HISTORY

Changes from Revision A (March 2011) to Revision B	Page
• Added RECOMMENDED OPERATING CONDITONS table. ....	5
• Added IDEAL RESISTANCE VALUES section. ....	16

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPL0102-100PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPL0102-100RUCR	ACTIVE	QFN	RUC	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL0102-100PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPL0102-100RUCR	QFN	RUC	14	3000	180.0	8.4	2.3	2.3	0.55	4.0	8.0	Q2



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL0102-100PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TPL0102-100RUCR	QFN	RUC	14	3000	202.0	201.0	28.0

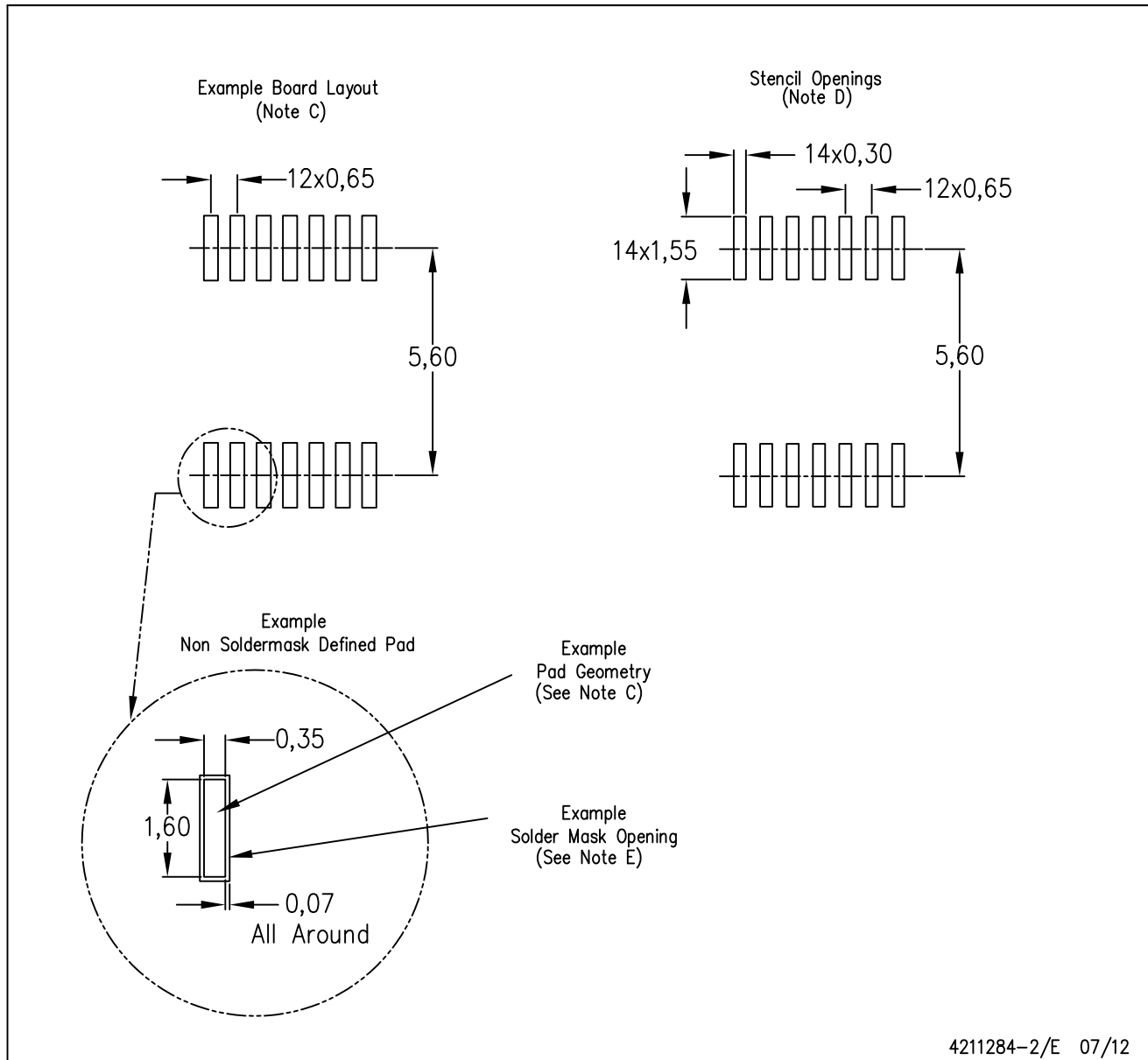
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

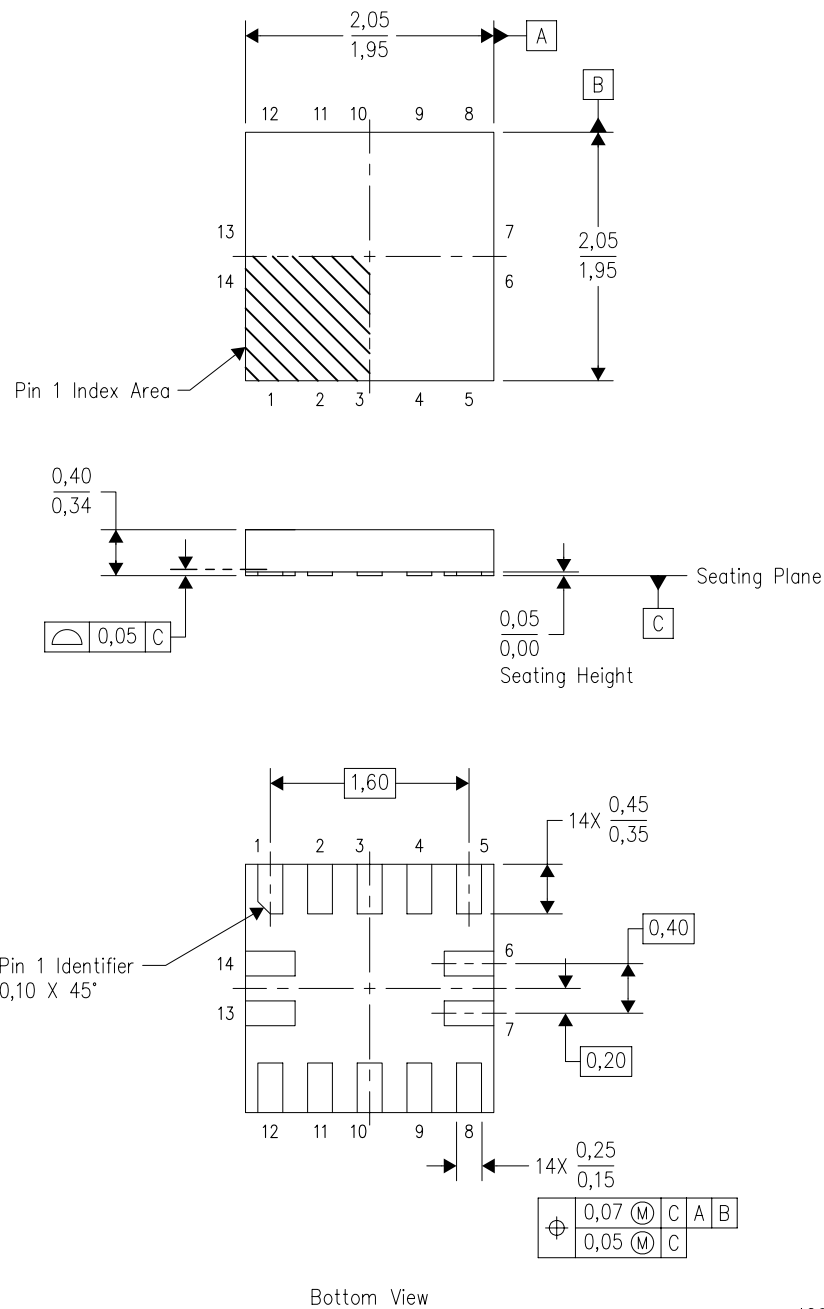
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUC (S-PX2QFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



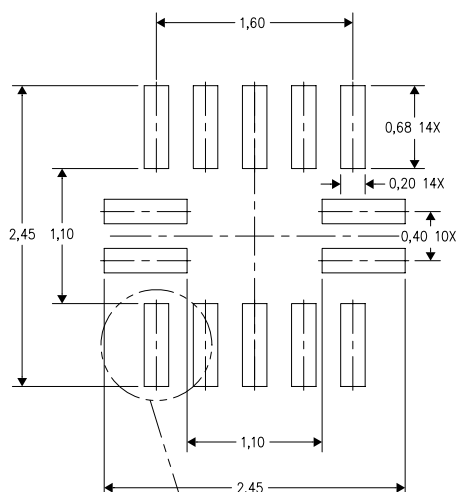
4208447/C 08/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-lead) package configuration.
  - D. This package complies to JEDEC MO-288 variation X2GFE.

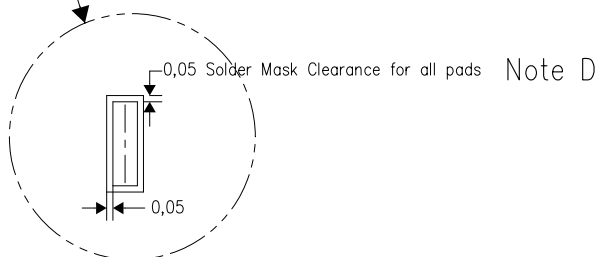
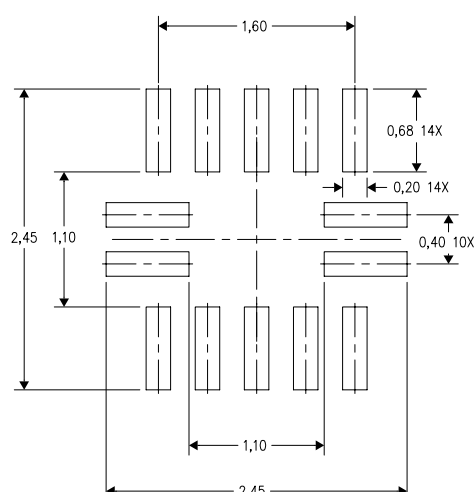
RUC (S-PX2QFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout



Example Stencil Design  
(Note E)



4211124/A 06/10

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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