Quad Channel High Speed ESD Protection Device

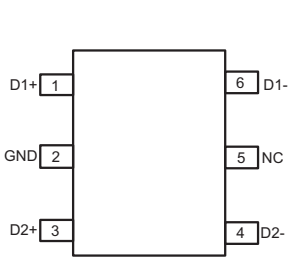
Check for Samples: TPD4E1U06

FEATURES

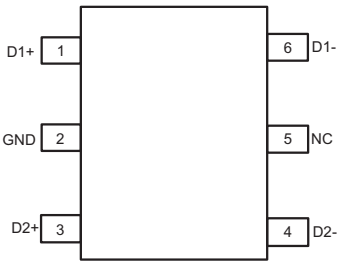
- **Provides System Level ESD Protection for Low-Voltage IO Interface**
- **IEC 61000-4-2 Level 4**
  - **±15kV (Contact discharge)**
  - **±15kV (Air-gap discharge)**
- **IO Capacitance 0.8pF (Typ)**
- **DC Breakdown Voltage 6.5V (Min)**
- **Ultra low Leakage Current 10nA (Max)**
- **Low ESD Clamping Voltage**
- **Industrial Temperature Range: –40°C to 125°C**
- **Small, Easy-to-Route DCK, DBV, and DGS Package**

APPLICATIONS

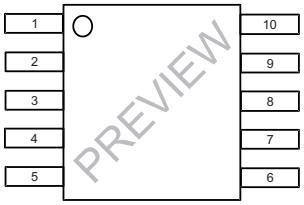
- **USB2.0**
- **Ethernet**
- **HDMI Control Lines**
- **MIPI Bus**
- **LVDS**
- **SATA**



DCK
2 mm x 2.1 mm x 0.95 mm
(0.65-mm pitch)



DBV
2.9 mm x 2.8 x 1.45 mm
(0.95-mm pitch)



DGS
3 mm x 4.9 mm x 1.1mm
(0.5-mm pitch)

DESCRIPTION

The TPD4E1U06 is a quad channel ultra low cap ESD protection device. It offers ±15KV IEC air-gap and ±15KV contact ESD protection. Its 0.8pF line capacitance makes it suitable for a wide range of applications. Typical application areas are HDMI, USB2.0, MHL, and DisplayPort.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	3000	Tape and reel	TPD4E1U06DCKR	BPI
–40°C to 125°C	3000	Tape and reel	TPD4E1U06DBVR	NG4I
–40°C to 125°C	3000	Tape and reel	TPD4E1U06DGSR	TBD

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM

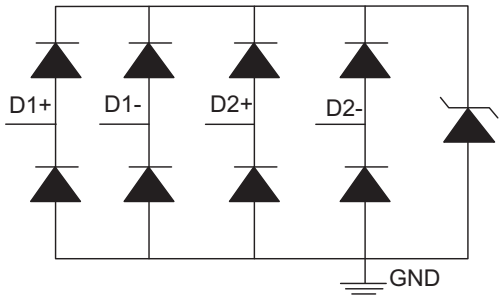


Figure 1. Circuit Schematic Diagram

TERMINAL FUNCTIONS DCK/DBV

PIN				DESCRIPTION	USAGE
NAME	DBV/DCK	DGS	TYPE		
D1+	1	1	I/O	ESD protected channel	Connect to data line as close to the connector as possible
D1–	6	9	I/O		
D2–	4	4	I/O		
D2+	3	6	I/O		
NC	5	2, 5, 7, 10	I/O	No connect	Can be left floating, grounded, or connected to VCC
GND	2	3, 8	GND	Ground	Connect to ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating temperature range	–40	125	°C
Storage temperature	–65	155	°C
IEC 61000-4-2 contact ESD		±15	kV
IEC 61000-4-2 air-gap ESD		±15	kV
I_{PP}, peak pulse current (tp = 8/20 µs)		3	A
P_{PP}, peak pulse power (tp = 8/20 µs)		45	W

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} = 10 µA				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, tp = 8/20 µSec, from I/O to GND(1)			11		V
		I_{PP} = 3A, tp = 8/20 µSec, from I/O to GND(1)			15		V
R_{DYN}	Dynamic resistance	Pin x to GND Pin(2)			1.0		Ω
		GND to Pin x			0.6		
C_L	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V, 25 °C			0.8	1	pF
C_{CROSS}	Channel to channel input capacitance	Pin 2 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins	DCK package		0.006	0.015	pF
			DBV package		0.01	0.025	
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of channel input capacitance	Pin 2 = 0V , f = 1 MHz, V_{BIAS} = 2.5 V, channel_x pin to gnd – channel_y pin to gnd			0.025	0.07	pF
V_{BR}	Break-down voltage, IO to GND	I_{IO} = 1 mA		6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V			1	10	nA

(1) Non-repetitive current pulse 8/20 us exponentially decaying waveform according to IEC61000-4-5
(2) Extraction of RDYN using least squares fit of TLP characteristics between I=10A and I=20A

TYPICAL CHARACTERISTICS

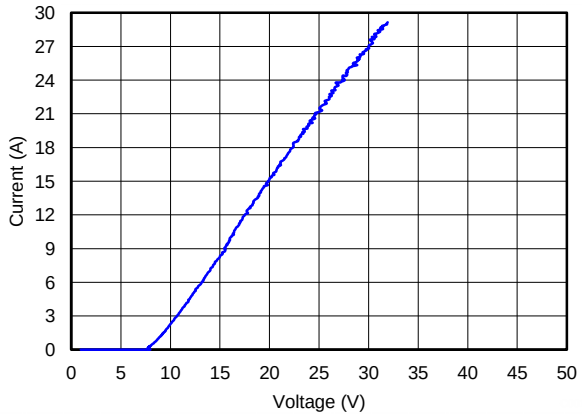


Figure 2. TLP, Data to GND

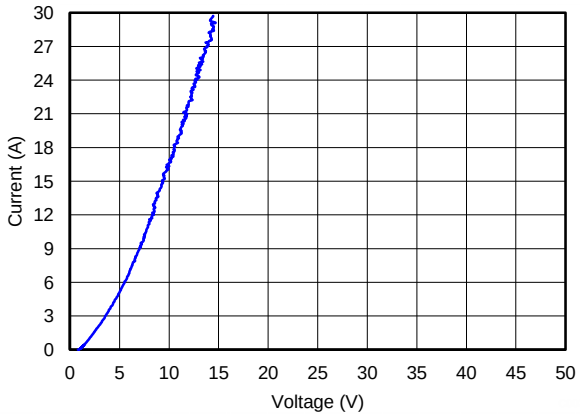


Figure 3. TLP, GND to Data

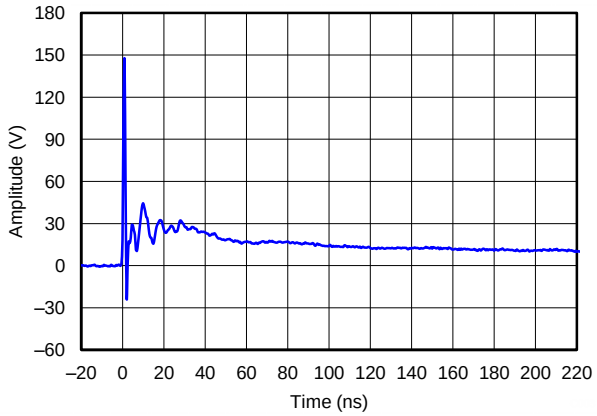


Figure 4. IEC 61000-4-2 Clamping Voltage, +8kV Contact

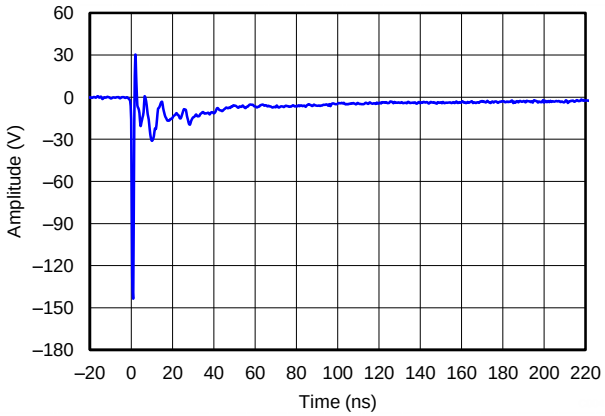


Figure 5. IEC 61000-4-2 Clamping Voltage, –8kV Contact

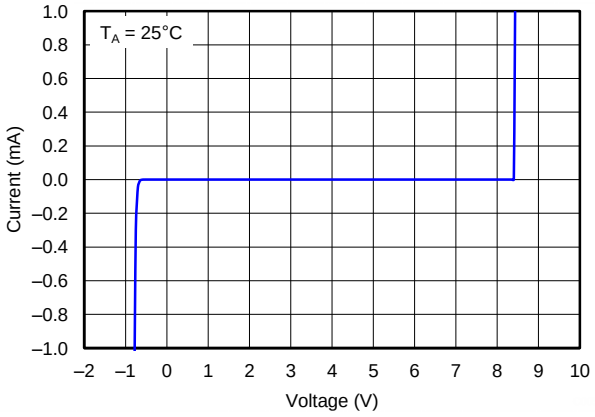


Figure 6. Diode Curve, T_A = 25°C

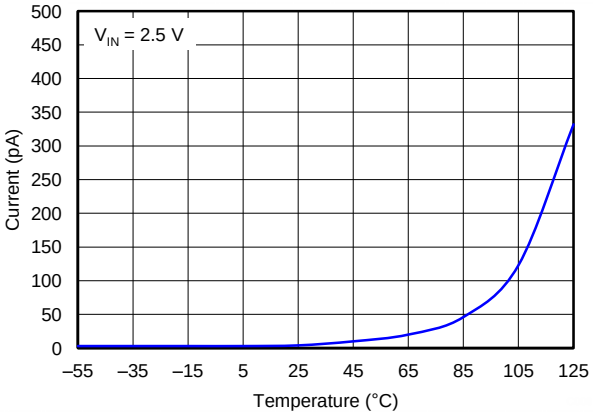


Figure 7. I_{LEAK} vs. Temperature, V_{IN} = 2.5 V

TYPICAL CHARACTERISTICS (continued)

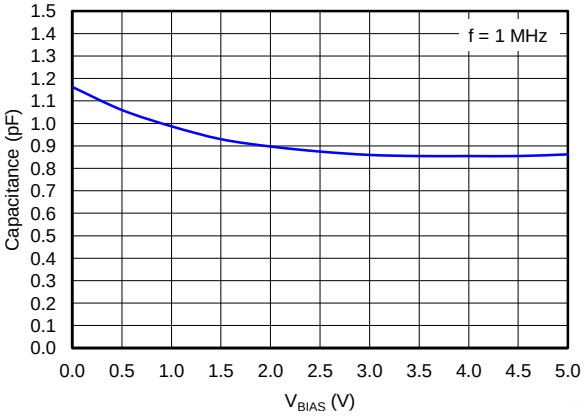


Figure 8. Capacitance Across V_{BIAS}, f = 1 MHz

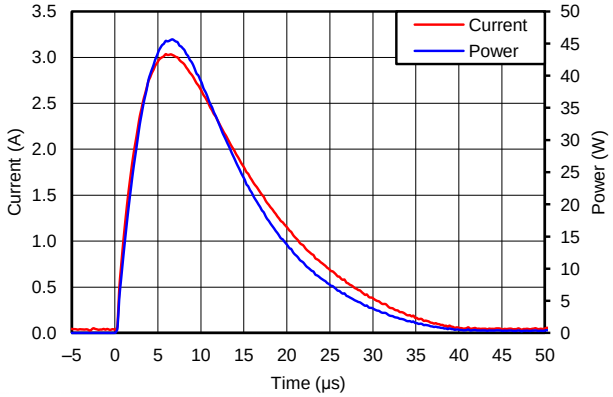


Figure 9. Surge Curve (tp = 8/20 µs), Pin IO to GND

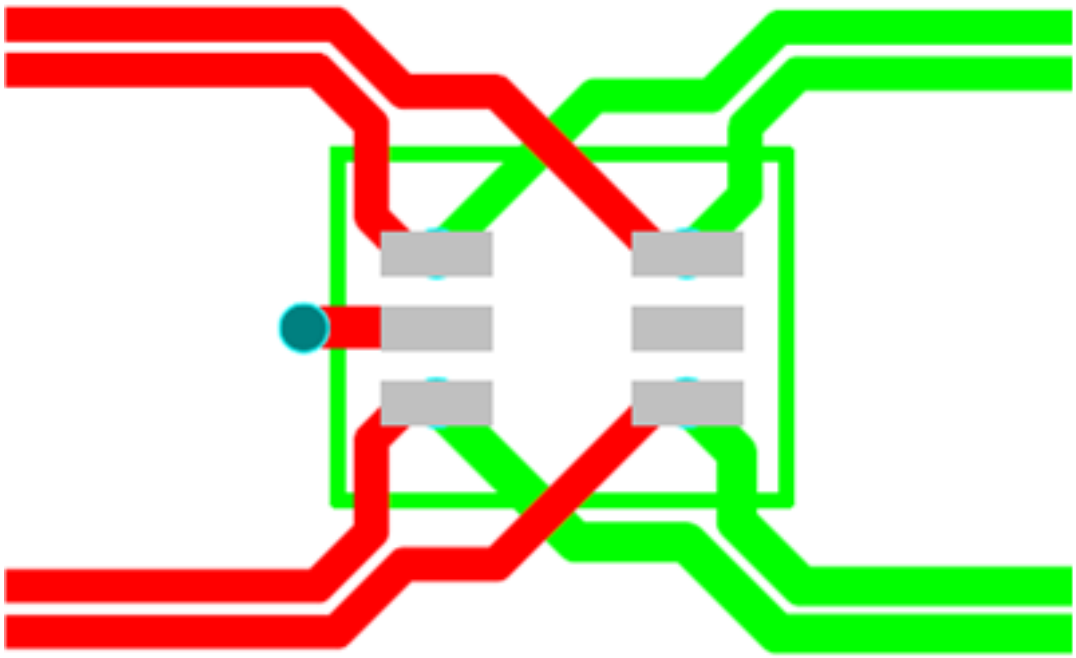


Figure 10. PCB Layout Recommendation

REVISION HISTORY

Changes from Revision A (December 2012) to Revision B	Page
• Added C_{CROSS} data for DBV package	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD4E1U06DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NG4I	Samples
TPD4E1U06DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BP6, BPI)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

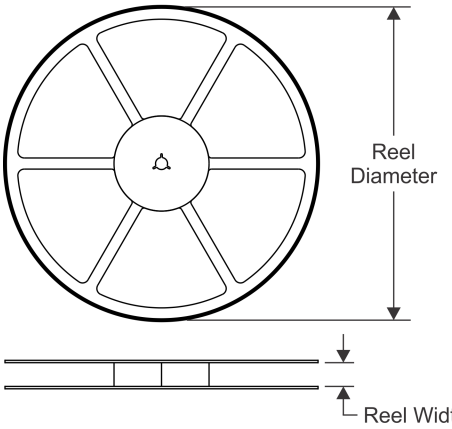
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

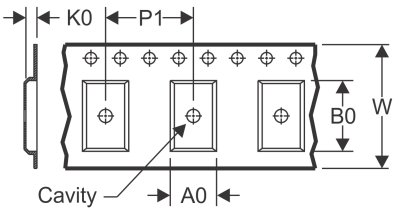
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

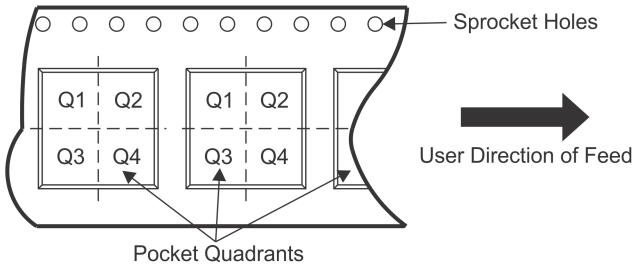


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

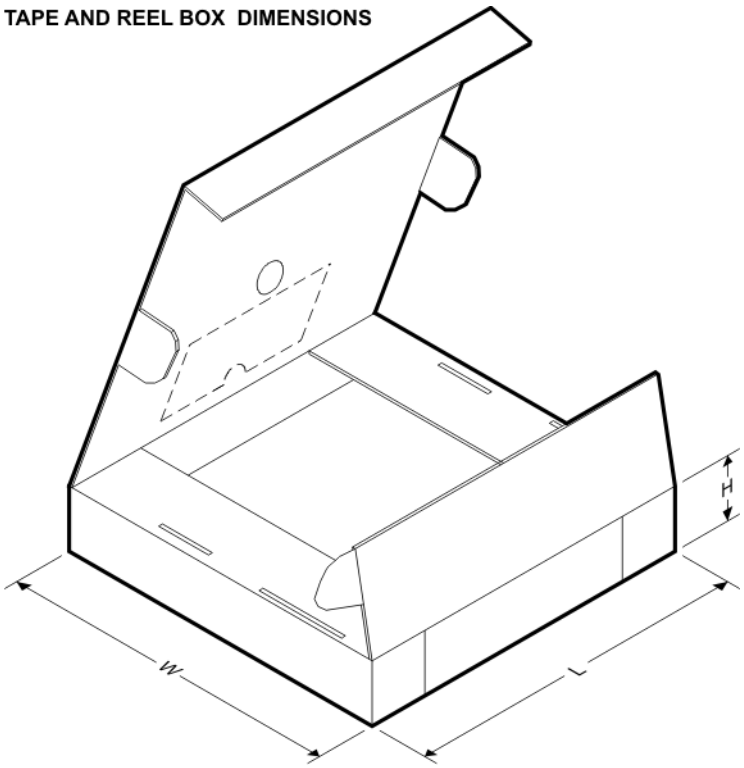
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E1U06DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPD4E1U06DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPD4E1U06DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

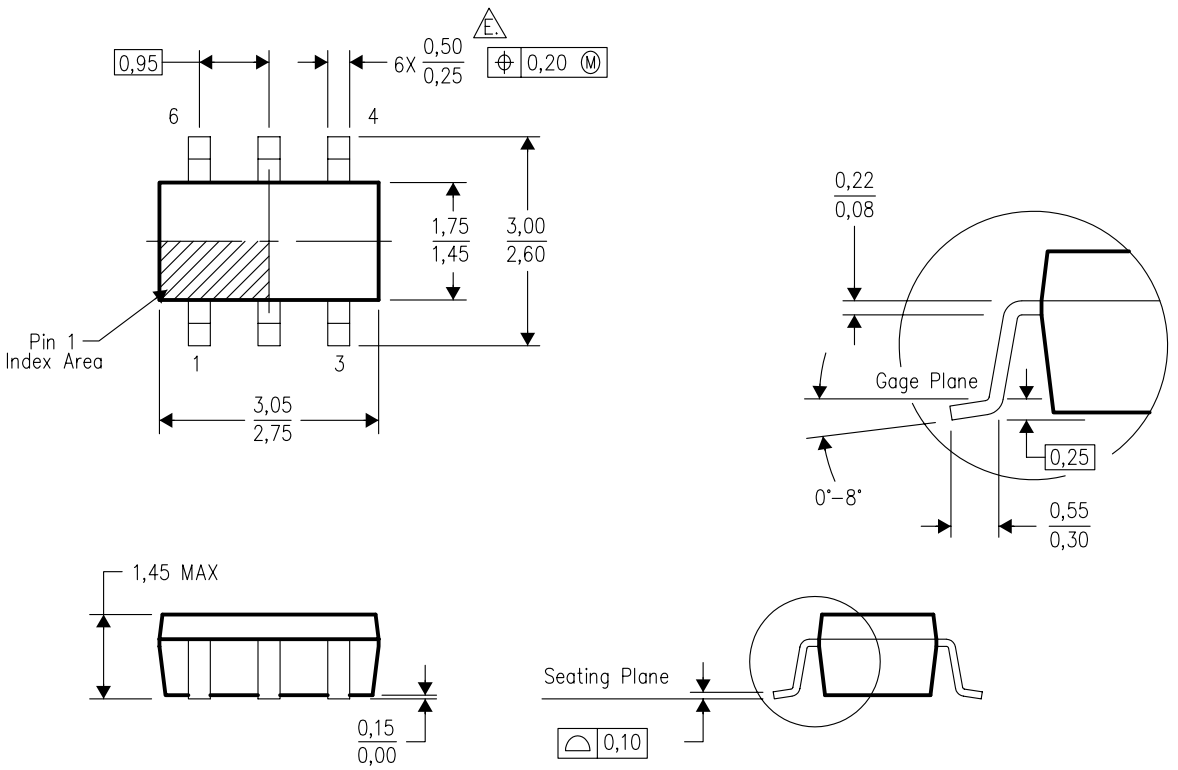
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E1U06DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPD4E1U06DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TPD4E1U06DCKR	SC70	DCK	6	3000	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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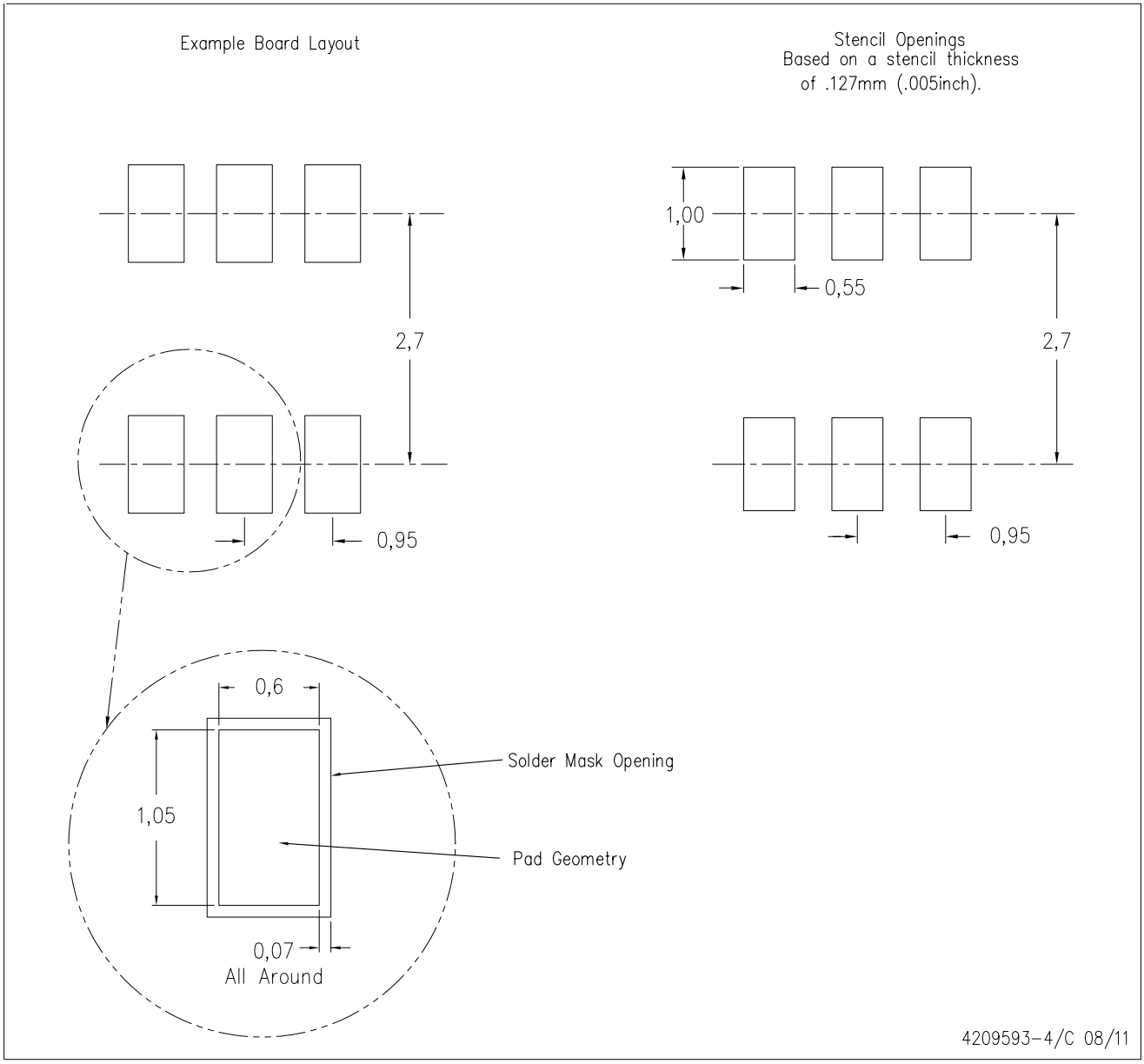
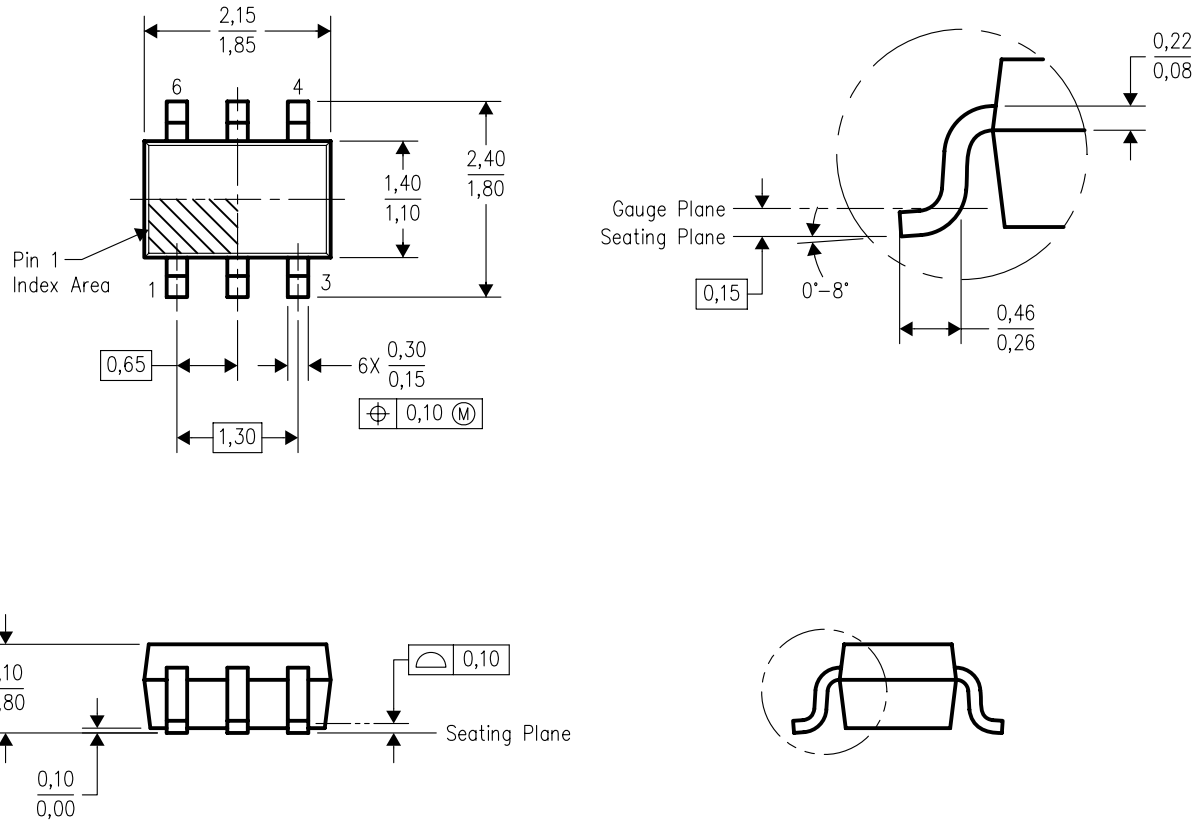
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

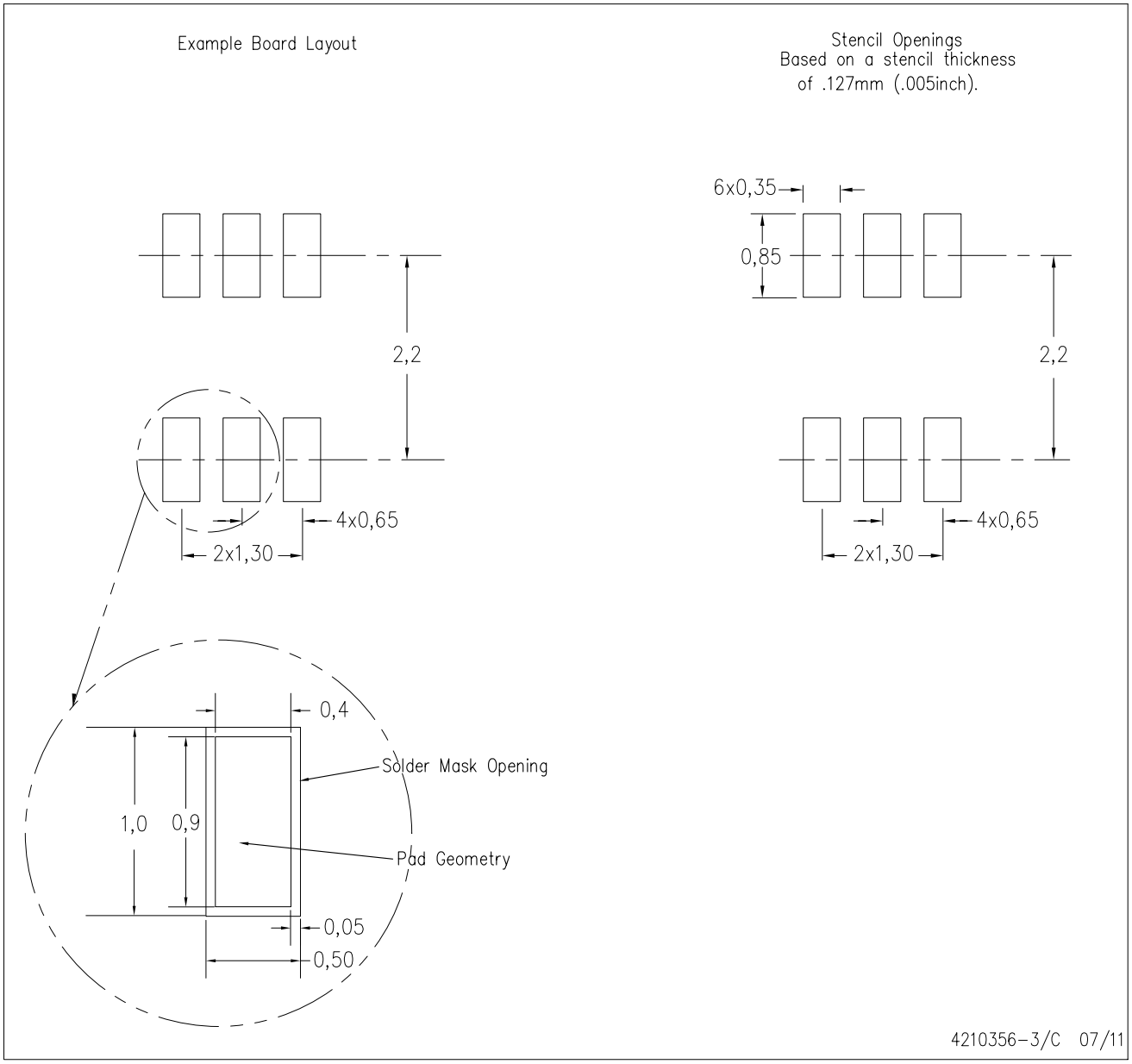
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



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