

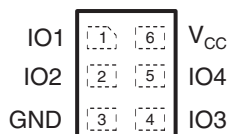
## FEATURES

- ESD Protection Exceeds JESD
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 8$ -kV IEC 61000-4-2 Contact Discharge
  - $\pm 12$ -kV IEC 61000-4-2 Air-Gap Discharge
- Low 1.6-pF Input Capacitance
- 0.9-V to 5.5-V Supply Voltage Range
- 4-Channel Device
- Space-Saving SON (DRY) Package

## APPLICATIONS

- USB
- Ethernet
- FireWire
- Video
- Cell Phones
- SVGA Video Connections
- Glucose Meters

DRY PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The TPD4E004 is a low-capacitance  $\pm 15$ -kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steers ESD current pulses to  $V_{CC}$  or GND. The TPD4E004 protects against ESD pulses up to  $\pm 15$ -kV Human-Body Model (HBM),  $\pm 8$ -kV Contact Discharge, and  $\pm 12$ -kV Air-Gap Discharge, as specified in IEC 61000-4-2. This device has a 1.6-pF capacitance per channel, making it ideal for use in high-speed data IO interfaces.

The TPD4E004 is a quad-ESD structure designed for USB, ethernet, and other high-speed applications.

The TPD4E004 is available in the DRY package and is specified for  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  operation.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	SON – DRY (1.0 mm $\times$ 1.45 mm, Pitch = 0.5 mm, Height = 0.55 mm)	Reel of 5000	TPD4E004DRYR	2P

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



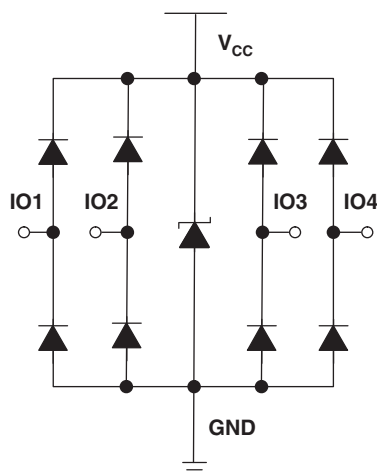
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# TPD4E004

## 4-CHANNEL ESD-PROTECTION ARRAY FOR HIGH-SPEED DATA INTERFACES

SLVS729A—FEBRUARY 2008—REVISED FEBRUARY 2008



### PIN DESCRIPTION

TERMINAL		DESCRIPTION
NAME	NO.	
GND	3	Ground
IOx	1,2,4,5	ESD-protected channel
V <sub>CC</sub>	6	Power-supply input

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	−0.3	5.5	V
V <sub>IO</sub>	Input/output voltage range	−0.3	V <sub>CC</sub> + 0.3	V
T <sub>stg</sub>	Storage temperature range	−65	150	°C
T <sub>J</sub>	Junction temperature		150	°C
Bump temperature (soldering)	Infrared (15 s)		220	°C
	Vapor phase (60 s)		215	
Lead temperature (soldering, 10 s)			300	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 0.9\text{ V}$  to  $5.5\text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise noted)

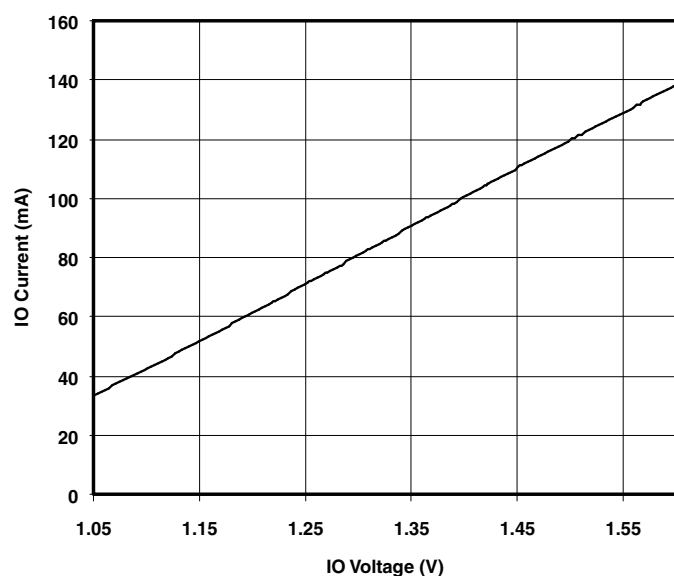
PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{CC}$ Supply voltage		0.9		5.5	V
$I_{CC}$ Supply current				500	nA
$V_F$ Diode forward voltage	$I_F = 1\text{ mA}$		0.8		V
$I_l$ Channel leakage current			$\pm 1$		nA
$V_{BR}$ Break-down voltage	$I_l = 10\text{ }\mu\text{A}$	6		8	V
$C_{I/O}$ Channel input capacitance	$V_{CC} = 5\text{ V}$ , Bias of $V_{CC}/2$ , $f = 10\text{ MHz}$		1.6	2	pF

(1) Typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

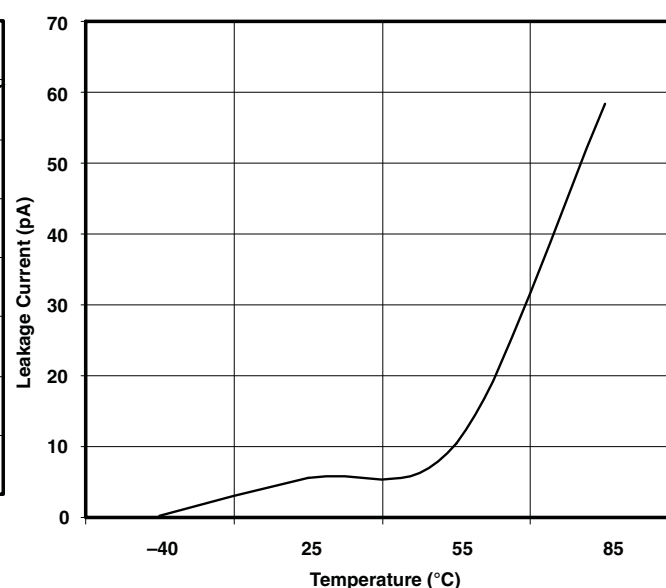
## ESD Protection

PARAMETER	TYP	UNIT
HBM	$\pm 15$	kV
IEC 61000-4-2 Contact Discharge	$\pm 8$	kV
IEC 61000-4-2 Air-Gap Discharge	$\pm 12$	kV

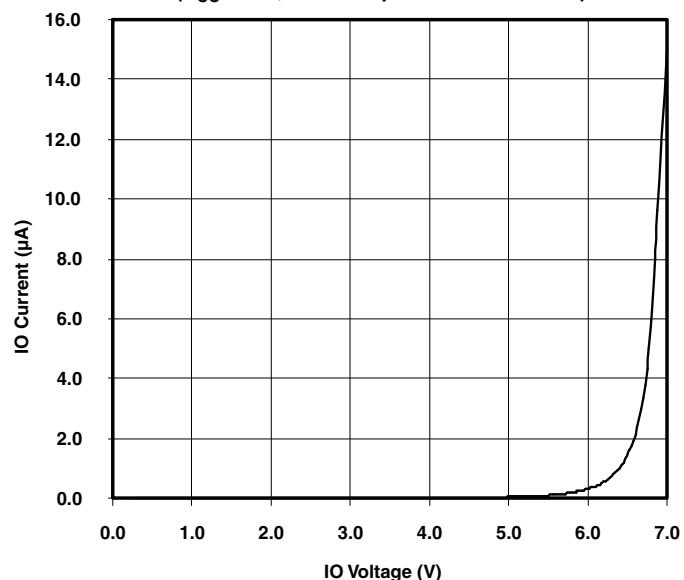
## TYPICAL OPERATING CHARACTERISTICS



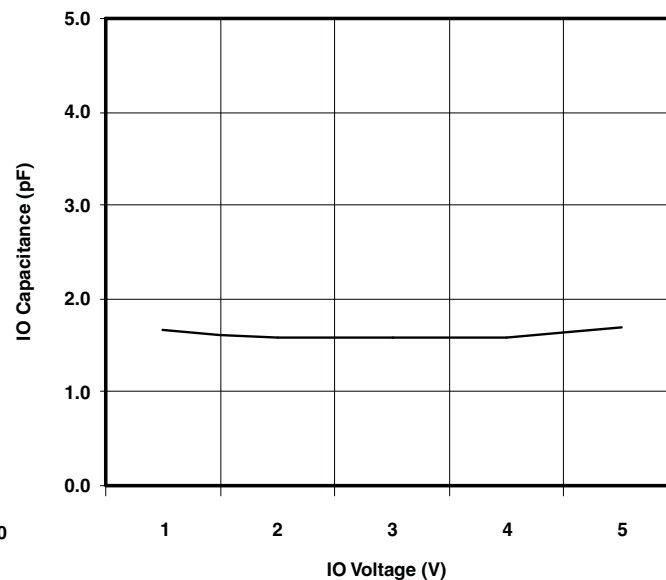
**Figure 1. Forward Diode Voltage (Upper Clamp Diode)**  
( $V_{CC} = 0$  V, DC Sweep Across the IO Pin)



**Figure 2. Leakage Current vs Temperature ( $V_{IO} = 2.5$  V)**



**Figure 3. Reverse Diode Curve Current IO to GND**  
( $V_{CC} = \text{Open}$ )



**Figure 4. IO Capacitance vs Input Voltage**  
( $V_{CC} = 5$  V)

### TYPICAL OPERATING CHARACTERISTICS (continued)

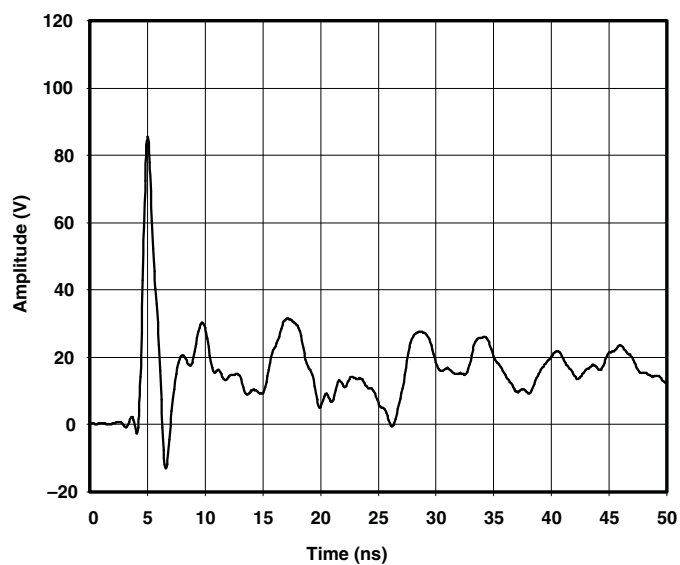
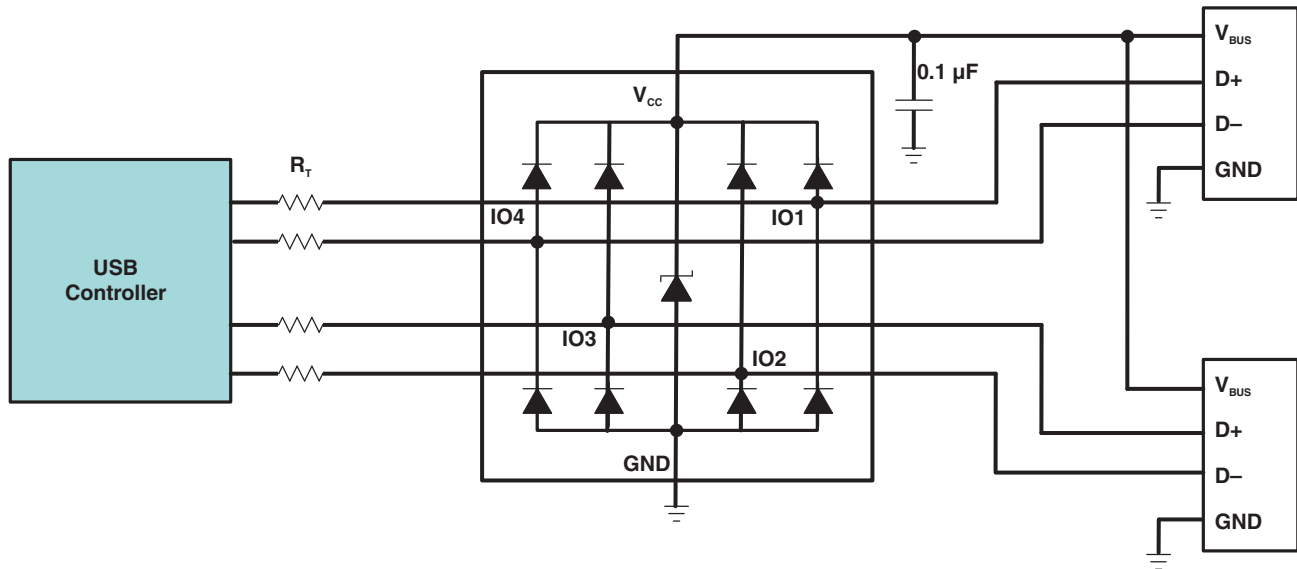


Figure 5. IEC ESD Clamping Waveforms +8-kV Contact

## APPLICATION INFORMATION



### Detailed Description

When placed near the connector, the TPD4E004 ESD solution offers little or no signal distortion during normal operation due to low I/O capacitance and ultra-low leakage current specifications. The TPD4E004 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/design guidelines should be followed:

1. Place the TPD4E004 solution close to the connector. This allows the TPD4E004 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a  $0.1\text{-}\mu F$  capacitor very close to the  $V_{CC}$  pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Make sure that there is enough metallization for the  $V_{CC}$  and GND loop. During normal operation, the TPD4E004 consumes nA leakage current. But during the ESD event,  $V_{CC}$  and GND may see  $15 \mu A$  to  $30 \mu A$  of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating.
5. The  $V_{CC}$  pin can be connected in two different ways:
  - a. If the  $V_{CC}$  pin is connected to the system power supply (a  $0.1\text{-}\mu F$  capacitor at  $V_{CC}$  is recommended for ESD bypass), the TPD4E004 works as a transient voltage suppressor for any signal swing above  $V_{CC} + V_d$ .
  - b. If the  $V_{CC}$  pin is not connected to system power supply (a  $0.1\text{-}\mu F$  capacitor is still recommended at the  $V_{CC}$  pin for ESD bypass), the TPD4E004 can tolerate higher signal swing in the range up to  $V_{BR}$ . Note that initially the bypass capacitor is charged by the signals through clamp diode.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD4E004DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P	<a href="#">Samples</a>
TPD4E004DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E004DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1



## TAPE AND REEL BOX DIMENSIONS

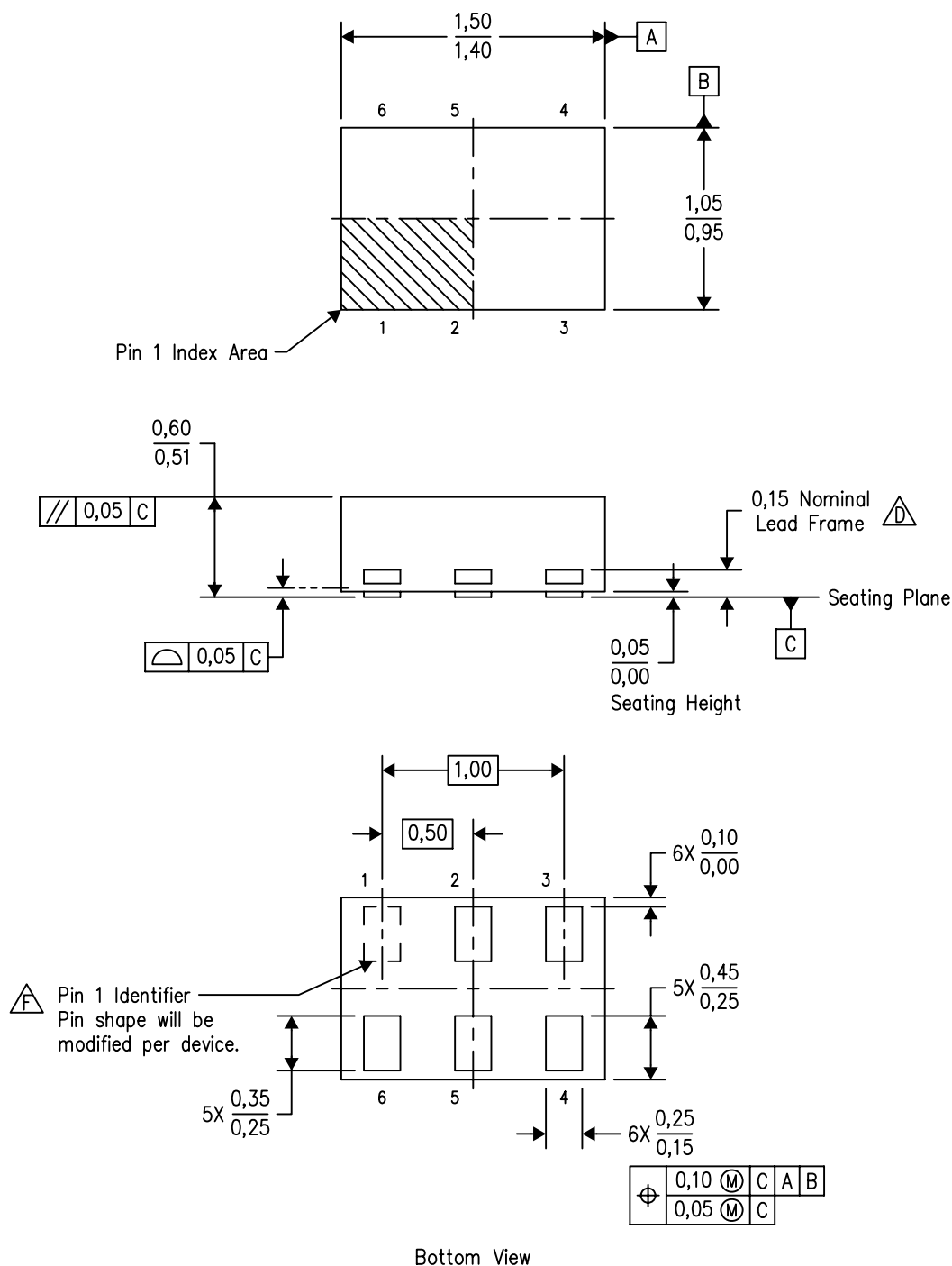


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E004DRYR	SON	DRY	6	5000	203.0	203.0	35.0

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

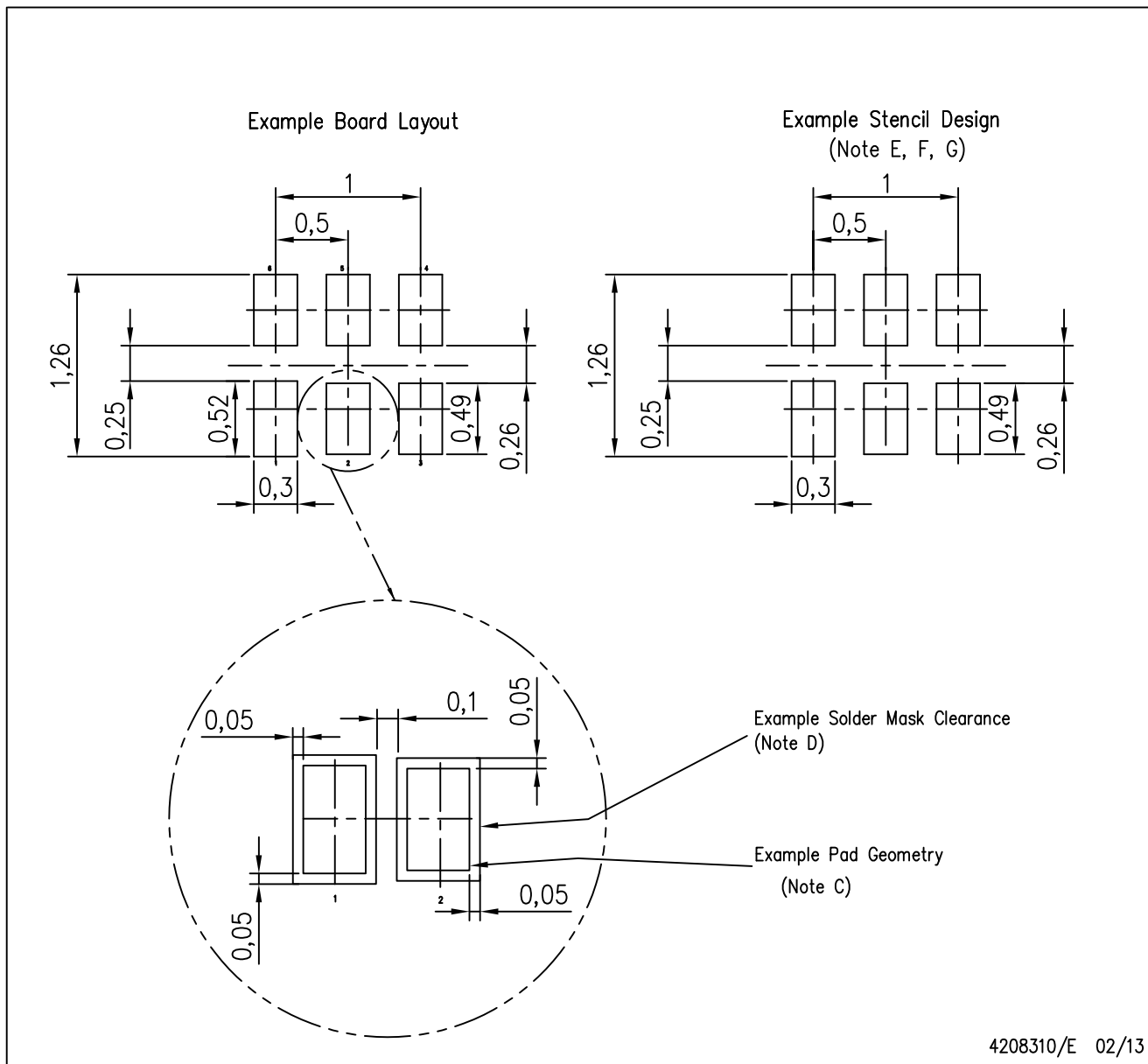


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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
  - E. This package complies to JEDEC MO-287 variation UFAD.
  - F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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