



PRELIMINARY

## TP3401, TP3402, TP3403 DASL Digital Adapter for Subscriber Loops

### General Description

The TP3401, TP3402 and TP3403 are complete monolithic transceivers for data transmission on twisted pair subscriber loops. They are built on National's double poly microCMOS process, and require only a single +5 Volt supply. Alternate Mark Inversion (AMI) line coding, in which binary '1's are alternately transmitted as a positive pulse then a negative pulse, is used to ensure low error rates in the presence of noise with lower emi radiation than other codes such as Bi-phase (Manchester).

Full-duplex transmission at 144 kb/s is achieved on a single twisted wire pair using a burst-mode technique (Time Compression Multiplexed). Thus the device operates as an ISDN 'U' Interface for short loop applications, typically in a PBX environment, providing transmission for 2 B channels and 1 D channel. On #24 cable, the range is at least 1.8 km (6k ft).

System timing is based on a Master/Slave configuration, with the line card end being the Master which controls loop timing and synchronisation. All timing sequences necessary for loop activation and de-activation are generated on-chip. Selection of Master and Slave mode operation is programmed via the Microwire Control Interface.

A 2.048 MHz clock, which may be synchronized to the system clock, controls all transmission-related timing functions.

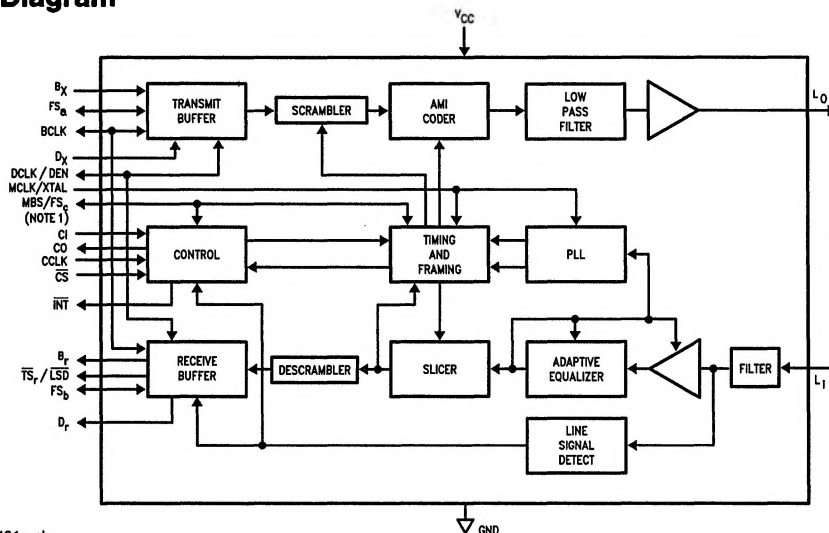
For the TP3401, this clock must be provided from an external source; the TP3402 includes an oscillator circuit requiring an external crystal. The TP3403 includes the functions of both the TP3401 and the TP3402.

### Features

Complete ISDN PBX 2-Wire Data Transceiver including:

- 2 B plus D channel interface for PBX U' Interface
- 144 kb/s full-duplex on 1 twisted pair using Burst Mode
- Loop range up to 6 kft (#24AWG)
- Alternate Mark Inversion coding with transmit filter and scrambler for low emi radiation
- Adaptive line equalizer
- On-chip timing recovery, no external components
- Standard TDM interface for B channels
- Separate interface for D channel
- 2.048 MHz master clock
- Driver for line transformer
- 4 loop-back test modes
- Single +5V supply
- MICROWIRE™ compatible serial control interface
- Applications in:
  - PBX Line Cards
  - Terminals
  - Regenerators
- Available in both 20-pin DIP and 28-pin PLCC

### Block Diagram

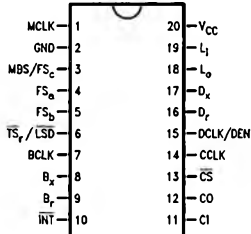


Note 1: TP3401 only.

TL/H/9264-1

## Connection Diagram

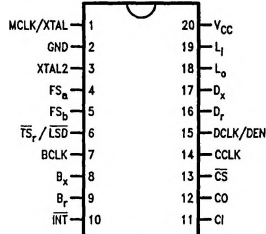
TP3401 DASL



TL/H/9264-2

Order Number TP3401J  
See NS Package Number J20A

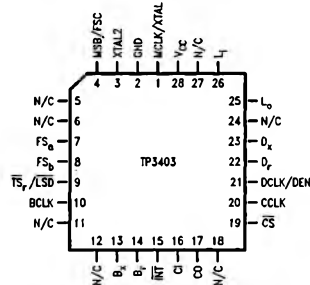
TP3402 DASL



TL/H/9264-15

Order Number TP3402J  
See NS Package Number J20A

TP3403 Package Information



TL/H/9264-16

Order Number TP3403V  
See NS Package Number V28A

## Pin Descriptions

| Name  | Description   |
|---|---|
| GND   | Negative power supply pin, normally 0V. All analog and digital signals are referred to this pin.  |
| V <sub>CC</sub>                                 | Positive power supply input, which must be +5V ± 5%.  |
| MCLK<br>(TP3401 only)                           | The 2.048 MHz Master Clock input, which requires a CMOS logic level clock input from a stable source. Must be synchronous with BCLK.  |
| MCLK/XTAL<br>(TP3402/3403 only)                 | This pin is the 2.048 MHz Master Clock input, which requires either a crystal to be connected between this pin and XTAL2 or a CMOS logic level clock from a stable source, which must be synchronous with BCLK.   |
| XTAL2<br>(TP3402 and TP3403 only)               | This pin is the output side of the oscillator amplifier.  |
| MBS/FS <sub>C</sub><br>(TP3401 and TP3403 only) | In Master Mode, this pin is the Master Burst Sync input, which may be clocked at 4 kHz to synchronize Transmit bursts from a number of devices at the Master end only. The 4 kHz should be nominally a square wave signal. In Slave mode, this pin is a short Frame Sync output, suitable for driving another DASL in Master Mode to provide a regenerator (i.e. range-extender) capability.                                    |
| BCLK  | Bit Clock logic signal which determines the data shift rate for B channel data on the digital interface side of the device. In Master mode this pin is an input which may be any multiple of 8 kHz from 256 kHz to 2.048 MHz, but must be synchronous with MCLK. In Slave mode this pin is an output at 2.048 MHz.  |
| FS <sub>a</sub>                                 | In Master mode only, this pin is the Transmit Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time for transmit B channel data into B <sub>x</sub> ; FS <sub>a</sub> must be synchronous with BCLK and MCLK. In Slave mode only, this pin is a digital output pulse which indicates the 8-bit periods of the B1 channel data transfer at both B <sub>x</sub> and B <sub>r</sub> . |

| Name                 | Description   |
|----------------------|---|
| FS <sub>b</sub>      | In Master mode only, this pin is the Receive Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time of the device for receive B channel data out from B <sub>r</sub> ; FS <sub>b</sub> must be synchronous with BCLK and MCLK. In Slave mode only, this pin is a digital output pulse which indicates the 8-bit periods of the B2 channel data transfer at both B <sub>x</sub> and B <sub>r</sub> . |
| B <sub>x</sub>       | Digital input for B1 and B2 channel data to be transmitted to the line; must be synchronous with BCLK.  |
| B <sub>r</sub>       | Digital output for B1 and B2 channel data received from the line.   |
| TS <sub>r</sub> /LSD | In Master mode only, this pin is an open-drain output which is normally high impedance but pulls low during both B channel active receive time slots. In Slave mode only, this pin is an output which is normally high impedance and pulls low when a valid line signal is received.  |
| D <sub>x</sub>       | Digital input for D channel data to be transmitted to the line; must be synchronous with DCLK.  |
| D <sub>r</sub>       | Digital output for D channel data received from the line.   |
| DCLK/DEN             | In Master mode this pin is an input for the 16 kHz serial shift clock for D channel data on D <sub>x</sub> and D <sub>r</sub> , which should be synchronous with BCLK. It may also be re-configured via the Control Register to act as an enable input for clocking the D channel interface synchronized to BCLK. In Slave mode this is a 16 kHz clock output for D channel data.   |

\*Crystal specifications: 2.048 MHz parallel resonant, R<sub>S</sub> ≤ 100Ω with a 20 pF load. Crystal tolerance should be ±75 ppm for aging and temperature.

## Pin Descriptions (Continued)

| Name             | Description   |
|------------------|---|
| CI               | MICROWIRE control channel serial data input.  |
| CO               | MICROWIRE control channel serial data output.   |
| CCLK             | Clock input for the MICROWIRE control channel.  |
| $\overline{CS}$  | Chip Select input which enables the MICROWIRE control channel data to be shifted in and out when pulled low. When high, this pin inhibits the MICROWIRE interface.  |
| $\overline{INT}$ | Interrupt output, a latched output signal which is normally high-impedance and goes low to indicate a change of status of the loop transmission system. This latch is cleared when the Status Register is read by the microprocessor. |
| $L_o$            | Transmit AMI signal output to the line transformer. This pin is capable of driving a load impedance $\geq 60\Omega$ .   |
| $L_i$            | Receive AMI signal input from the line transformer. This is a high impedance input which requires an external line termination impedance.   |

## Functional Description

### POWER-UP/POWER-DOWN CONTROL

Following the initial application of power, the DASL enters the power-down (de-activated) state, in which all the internal circuits are inactive and in a low power state except for the line-signal detect circuit and the necessary bias circuit; the line output  $L_o$  is in a low impedance state and all digital outputs are inactive. All bits in the Control Register power-up initially set to '0', so that the device always initializes as the Master end. Thus, at the Slave end, a control word must be written through the MICROWIRE port to select Slave mode. While powered-down, the Line-Signal Detect circuits in both Master and Slave devices continually monitor the line, to enable loop transmission to be initiated from either end.

To power-up the device and initiate activation, bit C6 in the Control Register must be set high. Setting C6 low de-activates the loop and power-down the device, see Table I.

TABLE I. Power-Up/Power-Down Control (TP3401 Only)

| MBS/FS <sub>c</sub><br>Pin I/P<br>at Master | C6<br>State | Action   |
|---|-------------|--|
| 4 kHz or 1                                  | 0           | Powered-down, Line-Signal Detect active  |
| 1   | 1           | Powered-up, sending bursts synchronized to FS <sub>a</sub> at Master, or received burst at Slave |
| 4 kHz                                       | 1           | Powered-up, sending bursts synchronized to MBS at Master, or received burst at Slave             |

## LINE TRANSMIT SECTION

Alternate Mark Inversion (AMI) line coding is used on the DASL because of its spectral efficiency and null dc energy content. All transmitted bits, excluding the start bit, are scrambled by a 9-bit scrambler to provide good spectral spreading with a strong timing content. The scrambler feedback polynomial is:

$$x^9 + x^5 + 1.$$

Pulse shaping is obtained by means of a raised cosine switched-capacitor filter, in order to limit rf energy and crosstalk while minimizing inter-symbol interference (isi). Figure 3 shows the pulse shape at the  $L_o$  output, while a template for the typical power spectrum transmitted to the line with random data is shown in Figure 4.

The line-driver output,  $L_o$ , is designed to drive a transformer through a capacitor and termination resistor. A 1:1 transformer, terminated in  $100\Omega$ , results in a signal amplitude of typically 1.3V pk-pk on the line. Over-voltage protection must be included in the interface circuit.

## LINE RECEIVE SECTION

The front-end of the receive section consists of a continuous anti-alias filter followed by a switched-capacitor low-pass filter designed to limit the noise bandwidth with minimum intersymbol interference. To correct pulse attenuation and distortion caused by the transmission line an AGC circuit and first-order equalizer adapt to the received pulse shape, thus restoring a "flat" channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

From the equalized output a DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 2.048 MHz. At the Master end of the loop this reference is the network clock (BCLK), which controls all transmit functions; the DPLL clock is used only for received data sampling. At the Slave end, however, a 2.048 MHz crystal is required to generate a stable local oscillator which is used as a reference by the DPLL to run both the receive and transmit sides of the DASL device.

Following detection of the recovered symbols, the received data is de-scrambled by the same  $x^9 + x^5 + 1$  polynomial and presented to the digital system interface circuit.

When the device is de-activated, a Line-Signal Detect circuit remains powered-up to detect the presence of incoming bursts if the far-end starts to activate the loop. From a "cold" start, acquisition of bit timing and equalizer convergence with random scrambled data takes approximately 25 ms at each end of the loop. Full loop burst synchronization is achieved approximately 50 ms after the "activate" command at the originating end.

# Functional Description (Continued)

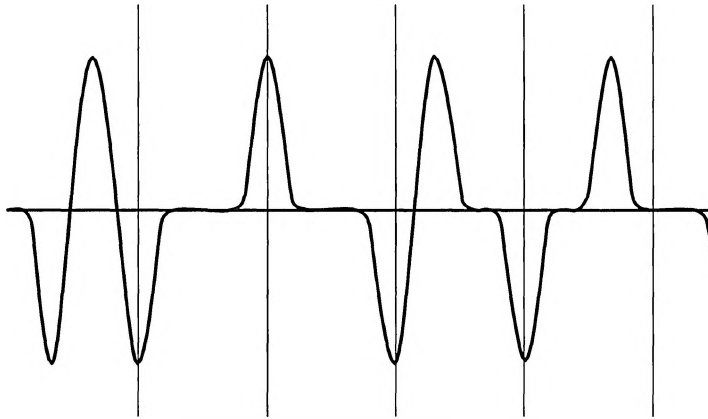


FIGURE 3. Typical AMI Waveform at  $L_o$

TL/H/9264-3

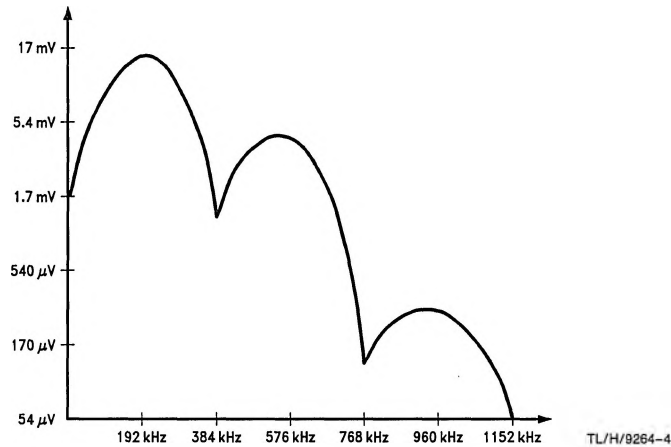


FIGURE 4. Typical AMI Transmit Spectrum Measured at LO Output (With RBW = 100 Hz).

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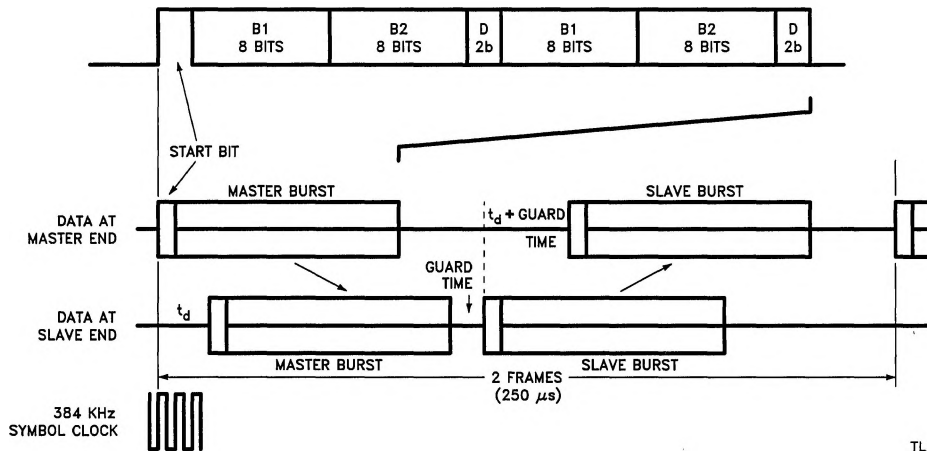


FIGURE 5. Burst Mode Timing on the Line

TL/H/9264-5

## Functional Description (Continued)

### BURST MODE OPERATION

For full-duplex operation over a single twisted-pair, burst mode timing is used, with the line-card (exchange) end of the link acting as the timing Master.

Each burst from the Master consists of the B1, B2 and D channel data from 2 consecutive frames combined in the format shown in *Figure 5*. During transmit bursts the Master's receiver input is inhibited to avoid disturbing the adaptive circuits. The Slave's receiver is enabled at this time and it synchronizes to the start bit of the burst, which is always an unscrambled '1' (of the opposite polarity to the last '1' sent in the previous burst). When the Slave detects that 36 bits following the start bit have been received, it disables the receiver input, waits 6 line symbol periods to match the other end settling guard time, and then begins to transmit its burst back towards the Master, which by this time has enabled its receiver input. The burst repetition rate is thus 4 kHz, which can either free-run or be locked to a synchronizing signal at the Master end by means of the MBS input (TP3401 only), (See *Figure 10*). In the latter case, with all Master-end transmitters in a system synchronized together, near-end crosstalk between pairs in the same cable binder may be eliminated, with a consequent increase in signal-to-noise ratio (SNR).

### ACTIVATION AND LOOP SYNCHRONIZATION

Activation (i.e. power-up and loop synchronization) may be initiated from either end of the loop. If the Master is activating the loop, it sends normal bursts of scrambled '1's, which are detected by the Slave's line-signal detect circuit, causing it to set  $C0 = 1$  in the Status Register, and pull the  $\overline{INT}$  pin low. Pin 6, the  $\overline{LSD}$  pin, also pulls low. To proceed with Activation, the device must be powered up by writing to the Control Register with  $C6 = 1$ . The Slave then replies with bursts of scrambled '1's synchronized to received bursts, and the flywheel circuit at each end searches for 4 consecutive correctly formatted receive bursts to acquire full loop synchronization. Each receiver indicates when it is correctly in sync with received bursts by setting the  $C1$  bit in the Status Register high and pulling  $\overline{INT}$  low.

To activate the loop from the Slave end, bit  $C6$  in the Control Register must be set high, which will power-up the device and begin transmission of alternate bursts i.e., the burst repetition rate is 2 kHz, not 4 kHz. At this point the Slave is running from its local oscillator and is not receiving any sync information from the Master. When the Master's line-signal detect circuit recognizes this "wake-up" signal, the Master is activated and begins to transmit bursts, synchronized, as normal, to the MBS or  $FS_a$  input with a 4 kHz repetition rate. This enables the Slave's receiver to correctly identify burst timing from the Master and to re-synchronize its own burst transmissions to those it receives. The flywheel circuits then acquire full loop sync as described earlier.

Loop synchronization is considered to be lost if the flywheel finds 4 consecutive receive burst "windows" (i.e. where a receive burst should have arrived based on timing from previous bursts) do not contain valid bursts. At this point bit  $C1$  in the Status Register is set low, the  $\overline{INT}$  output is set low and the receiver searches to re-acquire loop sync.

### DIGITAL SYSTEM INTERFACE

The digital system interface on the DASL separates B and D channel information onto different pins to provide maximum flexibility. On the B channel interface, phase skew between

transmit and receive directions may be accommodated at the Master end since separate frame sync inputs,  $FS_a$  and  $FS_b$ , are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface; since the counters are edge-synchronized the duration of the  $FS$  input signals may vary from a single-bit pulse to a square-wave. The serial shift rate is determined by the BCLK input, and may be any frequency from 128 kHz to 2.048 MHz, as shown in *Figure 6*.

At the Slave end, both  $FS_a$  and  $FS_b$  are outputs.  $FS_a$  goes high for 8 cycles of BCLK coincident with the 8 bits of the B1 channel in both Transmit and Receive directions.  $FS_b$  goes high for the next 8 cycles of BCLK, which are coincident with the 8 bits of the B2 channel in both Transmit and Receive directions. BCLK is also an output at 2.048 MHz, the serial data shift rate, as shown in *Figure 7*. Data may be exchanged between the B1 and B2 channels as it passes through the device, by setting Control bit  $C0 = 1$ . An additional Frame Sync output,  $FS_c$ , is provided to enable a regenerator to be built by connecting a DASL in Slave Mode to a DASL in Master Mode. The  $FS_c$  output from the Slave directly drives the  $FS_a$  and  $FS_b$  inputs on the Master.

D channel information, being packet-mode, requires no synchronizing input. This interface consists of the transmit data input,  $D_x$ , receive data output,  $D_r$ , and 16 kHz serial shift clock DCLK, which is an input at the Master end and an output at the Slave end. Data shifts into  $D_x$  on falling edges of DCLK and out from  $D_r$  on rising edges, as shown in *Figure 11*. DCLK should be Synchronous with BCLK.

An alternative function of the DCLK/DEN pin allows  $D_x$  and  $D_r$  to be clocked at the same rate as BCLK at the Master end only. By setting bit  $C1$  in the Control Register to a 1, DCLK/DEN becomes an input for an enabling pulse to gate 2 cycles of BCLK for shifting the 2 D bits per frame. Thus, at the Master end, the D channel bits can be interfaced to a TDM bus and assigned to a time-slot (the same time-slot for both transmit and receive), as shown in *Figure 12*.

### CONTROL INTERFACE

A serial interface, which can be clocked independently from the B and D channel system interfaces, is provided for microprocessor control of various functions on the DASL device. All data transfers consist of a single byte shifted into the Control Register via  $CI$  simultaneous with a single byte shifted out from the Status Register via  $CO$ , see *Figure 13*. Data shifts in to  $CI$  on rising edges of CCLK and out from  $CO$  on falling edges when  $\overline{CS}$  is pulled low for 8 cycles of CCLK. An Interrupt output,  $\overline{INT}$  goes low to alert the microprocessor whenever a change in one of the status bits,  $C1$  and/or  $C0$  has occurred. This latched output is cleared high following the first CCLK pulse when  $\overline{CS}$  is low. No interrupt is generated when status bit  $C2$  (bipolar violation) goes high, however. This bit is set whenever 1 or more violations of the AMI coding rule is received, and cleared everytime the  $\overline{CS}$  is pulsed. Statistics on the line bit error rate can be accumulated by regularly polling this bit.

When reading the  $CO$  pin, data is always clocked into the Control Register; therefore the  $CI$  data word should repeat the previous instruction if no change to the device mode is intended.

*Figure 13* shows the timing for this interface, and Table II lists the control functions and status indicators.

TABLE II. Control and Status Register Functions

| Bit | State | Control Register Function                | Status Register Function                   |
|-----|-------|--|--|
| C7  | 0     | Master Mode                              | Read Back C7 from Control Register         |
|     | 1     | Slave Mode                               | Read Back C7 from Control Register         |
| C6  | 0     | Deactivate and Power Down                | Read Back C6 from Control Register         |
|     | 1     | Power Up and Activate                    | Read Back C6 from Control Register         |
| C5  | 0     | Normal Through Connection                | Read Back C5 from Control Register         |
|     | 1     | Loopback to Digital Interface            | Read Back C5 from Control Register         |
| C4  | 0     | Normal Through Connection                | Read Back C4 from Control Register         |
|     | 1     | Loopback B1 + B2 + D to Line (Note 1)    | Read Back C4 from Control Register         |
| C3  | 0     | Normal Through Connection                | Read Back C3 from Control Register         |
|     | 1     | Loopback B1 Only to Line (Note 1)        | Read Back C3 from Control Register         |
| C2  | 0     | Normal Through Connection                | No Error                                   |
|     | 1     | Loopback B2 Only to Line (Note 1)        | Bipolar Violation Since Last READ (Note 2) |
| C1  | 0     | DCLK/DEN pin = 16 kHz Clock              | Out-Of-Sync                                |
|     | 1     | DCLK/DEN pin = D Channel Enable (Note 3) | Loop In-Sync and Activation Complete       |
| C0  | 0     | B1/B2 Channels Direct                    | No Line Signal at Receiver Input           |
|     | 1     | B1/B2 Channels Exchanged                 | Line Signal Present at Receiver Input      |

Note 1: Receive data active.

Note 2: After the device is in sync.

Note 3: In Master mode only.

Note 4: C7 is the first bit clocked in and out of the device.

## Timing Diagrams

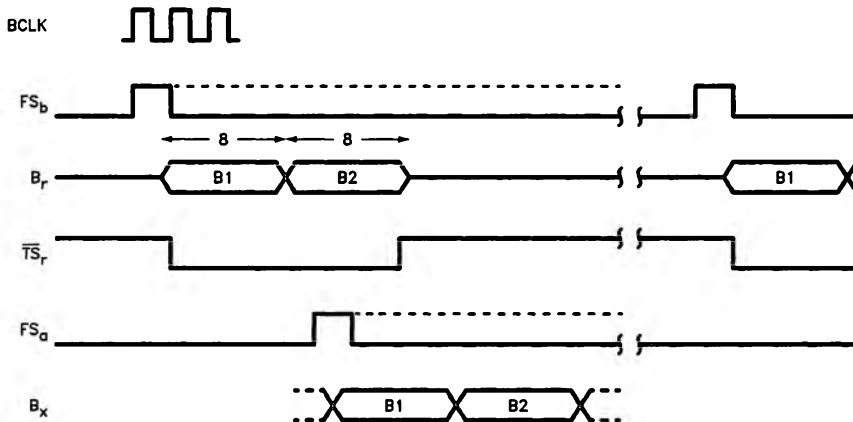


FIGURE 6. B Channel Interface Timing: Master Mode

TL/H/9264-6

## Timing Diagrams (Continued)

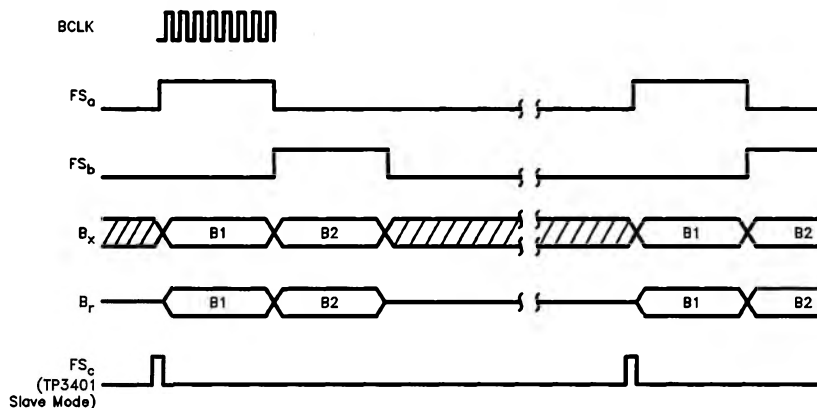


FIGURE 7. B Channel Interface Timing: Slave Mode

TL/H/9264-13

## Typical Applications

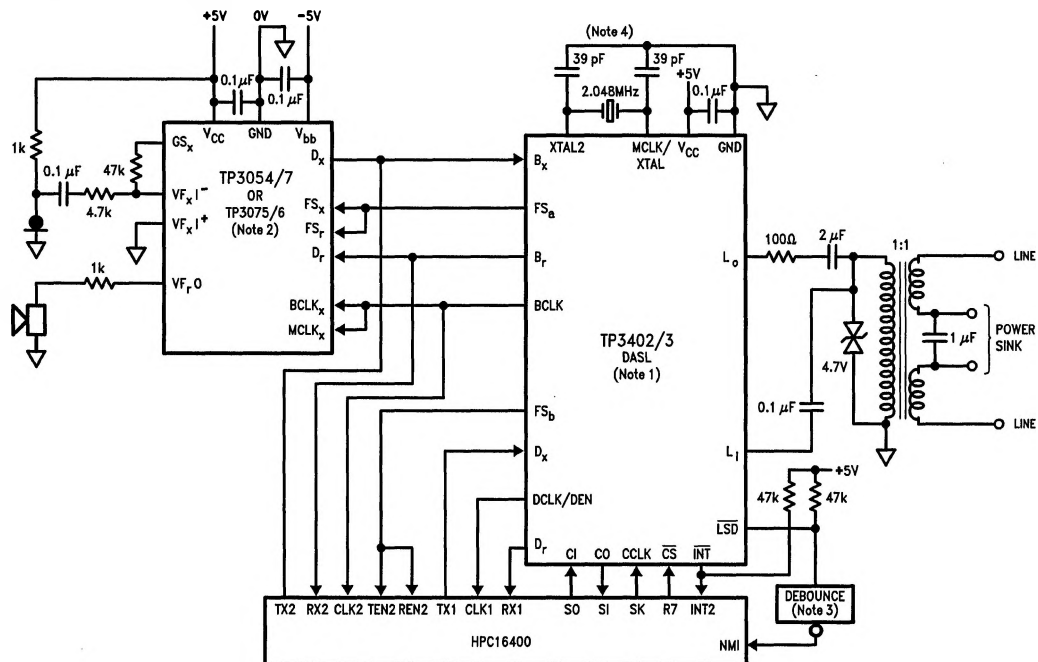


FIGURE 8. Typical Application for Slave End

TL/H/9264-11

**Note 1:** The TP3401 may also be used in this configuration with an external MCLK source.

**Note 2:** The TP3075/6 Programmable Combos also must be connected to the MICROWIRE interface.

**Note 3:** Only necessary if a mechanical Hookswitch is connected to the NMI input of the HPC.

**Note 4:** Crystal load capacitors include board and trace capacitance. Oscillator frequency can be checked by measuring the BCLK output frequency when slave mode part is in digital loopback.





## Timing Diagrams (Continued)

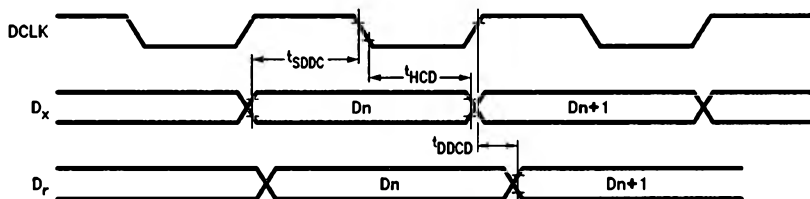
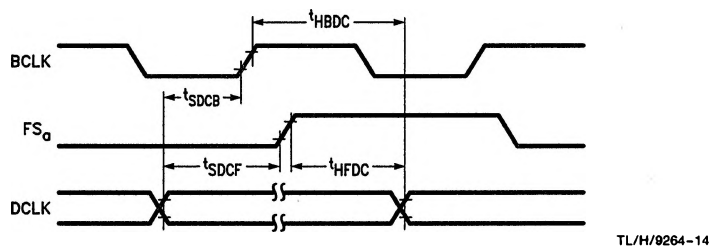


FIGURE 11. D Channel Interface Timing (Master and Slave Modes, C1 = 0)

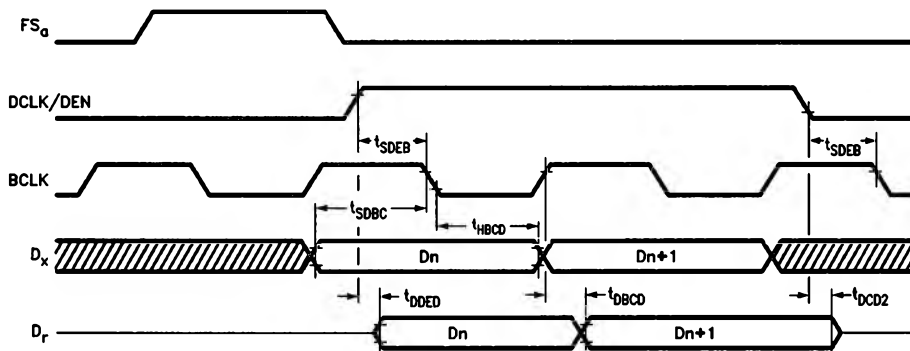
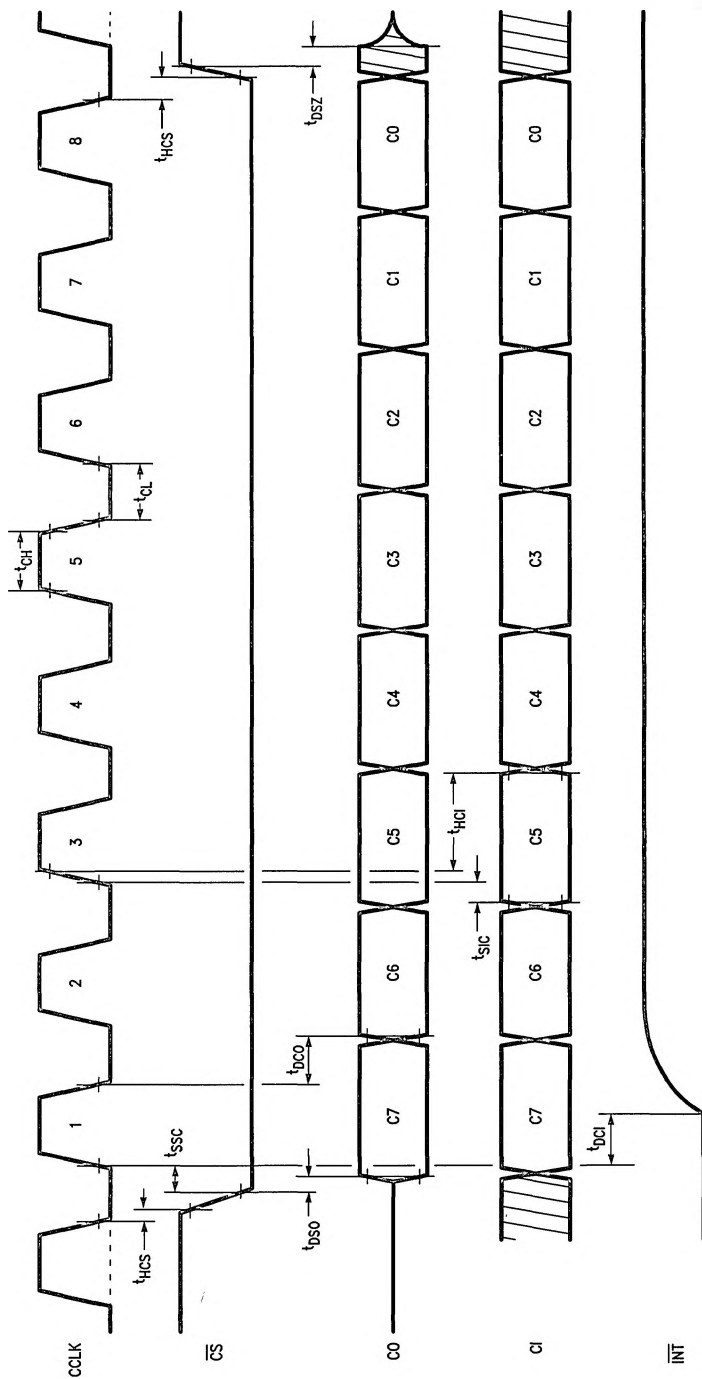


FIGURE 12. D Channel Interface Timing (Master Mode only, C1 = 1)

01-9826/H/TL

# Timing Diagrams (Continued)

FIGURE 13. Control Interface Timing



## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                              |                                |
|------------------------------|--------------------------------|
| $V_{CC}$ to GND              | 7V                             |
| Voltage at $L_i$ , $L_o$     | $V_{CC} + 1V$ to $V_{SS} - 1V$ |
| Voltage at any Digital Input | $V_{CC} + 1V$ to $V_{SS} - 1V$ |

|                                       |   |
|---------------------------------------|---|
| Storage Temperature Range             | $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ |
| Current at $L_o$                      | $\pm 100\text{ mA}$                             |
| Current at any Digital Output         | $\pm 50\text{ mA}$                              |
| Lead Temperature (Soldering, 10 sec.) | $300^{\circ}\text{C}$                           |
| ESD rating is to be determined.       |   |

**Electrical Characteristics** Unless otherwise noted, limits printed in **bold** characters are electrical testing limits at  $V_{CC} = 5.0V$  and  $T_A = 25^{\circ}\text{C}$ . All other limits are design goals for  $V_{CC} = 5.0V \pm 5\%$  and  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

| Symbol                          | Parameter   | Conditions   | Min       | Typ       | Max | Units         |
|---------------------------------|---|--|-----------|-----------|-----|---------------|
| <b>DIGITAL INTERFACES</b>       |   |  |           |           |     |               |
| $V_{IL}$                        | Input Low Voltage                                   | All Digital Inputs (not MCLK)  |           |           | 0.7 | V             |
| $V_{IH}$                        | Input High Voltage                                  | All Digital Inputs (not MCLK)  | 2.2       |           |     | V             |
| $V_{OL}$                        | Output Low Voltage                                  | $I_L = 1\text{ mA}$  |           |           | 0.4 | V             |
| $V_{OH}$                        | Output High Voltage                                 | $I_L = -1\text{ mA}$   | 2.4       |           |     | V             |
| $I_{IM}$                        | Input Current at MBS/FS <sub>c</sub>                | $GND < V_{IN} < V_{CC}$  | -600      |           | 10  | $\mu\text{A}$ |
| $I_I$                           | Input Current                                       | Any Other Digital Input, $GND < V_{IN} < V_{CC}$                                 | -10       |           | 10  | $\mu\text{A}$ |
| $I_{OZ}$                        | Output Current in High Impedance State (TRI-STATE®) | $B_r, \overline{INT}, \overline{TS_r}, CO$<br>$GND < V_{OUT} < V_{CC}$           | -10       |           | 10  | $\mu\text{A}$ |
| <b>LINE INTERFACES</b>          |   |  |           |           |     |               |
| $R_{Li}$                        | Input Resistance                                    | $0V < L_i < 5.0V$  | 200       |           |     | k $\Omega$    |
| $CL_{Lo}$                       | Load Capacitance                                    | $CL_{Lo}$ from $L_o$ to GND.   |           |           | 100 | pF            |
| $R_O$                           | Output Resistance at $L_o$                          | Load = 60 $\Omega$ in Series with 2 $\mu\text{F}$ to GND                         |           |           | 3.0 | $\Omega$      |
| $V_{DC}$                        | Mean d.c. Voltage at $L_o$                          | Load = 60 $\Omega$ in Series with 2 $\mu\text{F}$ to GND                         |           | 2.0       |     | V             |
| <b>POWER DISSIPATION</b>        |   |  |           |           |     |               |
| $I_{CC0}$                       | Power Down Current                                  |  |           | 1.3       | 2   | mA            |
| $I_{CC1}$                       | Power Up Current (Activated)                        | Load at $L_o = 200\Omega$ in Series with 2 $\mu\text{F}$ to GND (in Master Mode) |           |           | 18  | mA            |
| <b>TRANSMISSION PERFORMANCE</b> |   |  |           |           |     |               |
|                                 | Transmit Pulse Amplitude at $L_o$                   | $R_L = 200\Omega$ in Series with 2 $\mu\text{F}$ to GND                          | $\pm 0.9$ | $\pm 1.1$ |     | Vpk           |
|                                 | Input Pulse Amplitude at $L_i$                      |  | $\pm 60$  |           |     | mVpk          |
|                                 | Timing Recovery Jitter                              | BCLK at Slave Relative to MCLK at Master   |           | 100       |     | ns pk-pk      |
|                                 | Activation Time                                     | Complete Loop from Cold Start  |           | 50        |     | ms            |

## Timing Characteristics

Unless otherwise noted:  $V_{CC} = +5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ . Typical characteristics are specified at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ . All signals are referenced to GND.

| Symbol                                   | Parameter                              | Conditions  | Min  | Typ   | Max  | Units    |
|--|--|---|------|-------|------|----------|
| <b>MASTER CLOCK INPUT SPECIFICATIONS</b> |  |   |      |       |      |          |
| $F_{MCK}$                                | Master Clock Frequency                 |   |      | 2.048 |      | MHz      |
|  | Master Clock Tolerance                 | Measured Relative to the Slave MCLK                   | -100 |       | +100 | ppm      |
|  | Master Clock Input Jitter              | 2.048 MHz Input, $18\text{ kHz} < f < 200\text{ kHz}$ |      |       | 200  | ns pk-pk |
| $t_{WMH}$ ,<br>$t_{WML}$                 | Clock Pulse Width<br>Hi & Low for MCLK | $V_{IH} = V_{CC} - 0.5V$<br>$V_{IL} = 0.5V$           | 190  |       |      | ns       |
| $t_{MR}$ ,<br>$t_{MF}$                   | Rise and Fall Time<br>of MCLK          | Used as a Logic Input                                 |      |       | 15   | ns       |

### B CHANNEL INTERFACE (Figure 10)

|                          |  |   |     |       |     |         |
|--------------------------|--|---|-----|-------|-----|---------|
| $F_{BCK}$                | Bit Clock Frequency  | Master Mode Only                                    |     | 2.048 |     | MHz     |
| $t_{WBH}$ ,<br>$t_{WBL}$ | Clock Pulse Width<br>Hi & Low for BCLK                             | $V_{IH} = 2.2V$<br>$V_{IL} = 0.7V$                  | 190 |       |     | ns      |
| $t_{BR}$ ,<br>$t_{BF}$   | Rise and Fall Time<br>of BCLK                                      | Master Mode requirement for BCLK<br>Source          |     |       | 15  | ns      |
| $t_{SFB}$                | Set-Up Time, $FS_a$ and<br>$FS_b$ to BCLK Low                      | Master Mode Only                                    | 20  |       |     | ns      |
| $t_{HCFL}$               | Hold Time, BCLK Low to<br>$FS_a$ and $FS_b$ Low                    | Master Mode Only                                    | 100 |       |     | ns      |
| $t_{WBH}$ ,<br>$t_{WBL}$ | Output Pulse Width<br>High and Low for BCLK                        | Slave Mode Only<br>Load = 2 LSTTL Inputs Plus 50 pF | 195 |       |     | ns      |
| $t_{DCF}$                | Delay Time, BCLK High to<br>$FS_a$ , $FS_b$ and $FS_c$ Transitions | Slave Mode Only<br>Load = 2 LSTTL Inputs Plus 50 pF |     |       | 115 | ns      |
| $t_{SBC}$                | Set Up Time, $B_x$ Valid<br>to BCLK Low                            |   | 30  |       |     | ns      |
| $t_{HCB}$                | Hold Time, BCLK Low to<br>$B_x$ Invalid                            |   | 50  |       |     | ns      |
| $t_{DCB}$                | Delay Time, BCLK High<br>to $B_r$ Valid                            | Load = 2 LSTTL Inputs Plus 100 pF                   |     |       | 170 | ns      |
| $t_{DCBZ}$               | Delay Time, BCLK Low to<br>$B_r$ High-Impedance                    | Slave Mode Only                                     | 60  |       | 220 | ns      |
| $t_{DCT}$                | Delay Time, BCLK High<br>to $\overline{TS_r}$ Low                  | Load = 2 LSTTL Inputs Plus 100 pF                   |     |       | 150 | ns      |
| $t_{DCTZ}$               | Delay Time, BCLK Low to<br>$\overline{TS_r}$ High-Impedance        |   | 60  |       | 185 | ns      |
| $t_{SMBC}$               | Set-Up Time, MBS<br>to BCLK Low (Note 1)                           | Master Mode Only<br>(TP3401 and TP3403 only)        | 60  |       |     | ns      |
| $t_{WMBH}$               | Width of MBS Input<br>High   | Master Mode Only<br>(TP3401 and TP3403 only)        |     | 125   |     | $\mu s$ |

**Note 1:** MBS transitions may occur anywhere in the Frame, and require no specific relationship to  $FS_a$  or  $FS_b$ .

**Timing Characteristics** (Continued)

Unless otherwise noted:  $V_{CC} = +5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ . Typical characteristics are specified at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ . All signals are referenced to GND.

| Symbol  | Parameter   | Conditions                     | Min | Max | Units |
|---|---|--------------------------------|-----|-----|-------|
| <b>D CHANNEL INTERFACE (Figure 11 &amp; 12)</b> |   |                                |     |     |       |
| $t_{SDDC}$                                      | Set Up Time, $D_X$ Valid to DCLK Low                          |                                | 100 |     | ns    |
| $t_{HCD}$                                       | Hold Time, DCLK Low to $D_X$ Invalid                          |                                | 100 |     | ns    |
| $t_{DDCD}$                                      | Delay Time, DCLK High to $D_r$ Data Valid                     | Load = 100 pF + 2 LSTTL Inputs |     | 220 | ns    |
| $t_{SDCB}$                                      | Set-Up Time, DCLK Transitions to BCLK High                    | Master Mode Only               | 50  |     | ns    |
| $t_{HBDC}$                                      | Hold Time, BCLK High to DCLK Transitions                      | Master Mode Only               | 50  |     | ns    |
| $t_{SDCF}$                                      | Set-Up Time, DCLK Transitions to $FS_a$ High                  | Master Mode Only               | 100 |     | ns    |
| $t_{HFDC}$                                      | Hold Time, $FS_a$ High to DCLK Transition                     | Master Mode Only. Load = 50 pF | 50  |     | ns    |
| $t_{DDED}$                                      | Delay Time, DEN High to $D_r$ Valid                           | Load = 100 pF + 2 LSTTL Inputs |     | 200 | ns    |
| $t_{SDEB}$                                      | Set-Up Time, DEN to BCLK Low                                  |                                | 100 |     | ns    |
| $t_{SDBC}$                                      | Set-Up Time, $D_X$ to BCLK Low                                |                                | 30  |     | ns    |
| $t_{HBCD}$                                      | Hold Time, BCLK Low to $D_X$ Invalid                          |                                | 50  |     | ns    |
| $t_{DBCD}$                                      | Delay Time, BCLK High to $D_r$ Valid                          | Load = 100 pF + 2 LSSTL Inputs |     | 190 | ns    |
| $t_{DCDZ}$                                      | Delay Time, DEN Low to $D_r$ High Impedance                   |                                |     | 140 | ns    |
| <b>CONTROL INTERFACE (Figure 13)</b>            |   |                                |     |     |       |
| $t_{CH}$  | CCLK High Duration  |                                | 250 |     | ns    |
| $t_{CL}$  | CCLK Low Duration   |                                | 250 |     | ns    |
| $t_{SIC}$                                       | Setup Time, CI Valid to CCLK High                             |                                | 100 |     | ns    |
| $t_{HCI}$                                       | Hold Time, CCLK High to CI Invalid                            |                                | 0   |     | ns    |
| $t_{SSC}$                                       | Setup Time from $\overline{CS}$ Low to CCLK High              |                                | 200 |     | ns    |
| $t_{HCS}$                                       | Hold Time from CCLK Low to $\overline{CS}$                    |                                | 10  |     | ns    |
| $t_{DCO}$                                       | Delay Time from CCLK Low to $C0$ Data Valid                   | Load = 100 pF + 2 LSTTL Inputs |     | 150 | ns    |
| $t_{DSO}$                                       | Delay Time from $\overline{CS}$ Low to $CO$ Valid             | 1st Bit Only                   |     | 100 | ns    |
| $t_{DSZ}$                                       | Delay Time from $\overline{CS}$ High to $CO$ High Impedance   |                                |     | 100 | ns    |
| $t_{DCI}$                                       | Delay Time from CCLK1 High to $\overline{INT}$ High Impedance |                                |     | 120 | ns    |