

TP3052, TP3053, TP3054 TP3054-1, TP3057, TP3057-1 “Ruggedized” Serial Interface CODEC/Filter COMBO® Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ -law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (micro-CMOS).

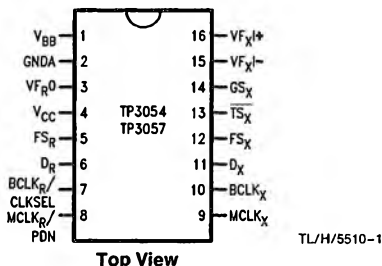
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ -law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ -law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
 - Transmit high-pass and low-pass filtering
 - Receive low-pass filter with sin x/x correction
 - Active RC noise filters
 - μ -law or A-law compatible Coder and DECoder
 - Internal precision voltage reference
 - Serial I/O interface
 - Internal auto-zero circuitry
- μ -law with signaling, TP3020 or TP5116A timing—TP3052
- μ -law with signaling, TP5116A family timing—TP3053
- μ -law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- $\pm 5V$ operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Dual-In-Line or PCC surface mount packages

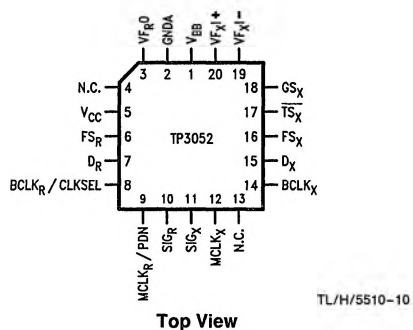
Connection Diagrams

Dual-In-Line Package



Order Number TP3054J, TP3054J-1,
 TP3057J or TP3057J-1
 See NS Package Number J16A

Plastic Chip Carriers



Order Number TP3052V*
 See NS Package Number V20A

*Available mid 1990

Block Diagram

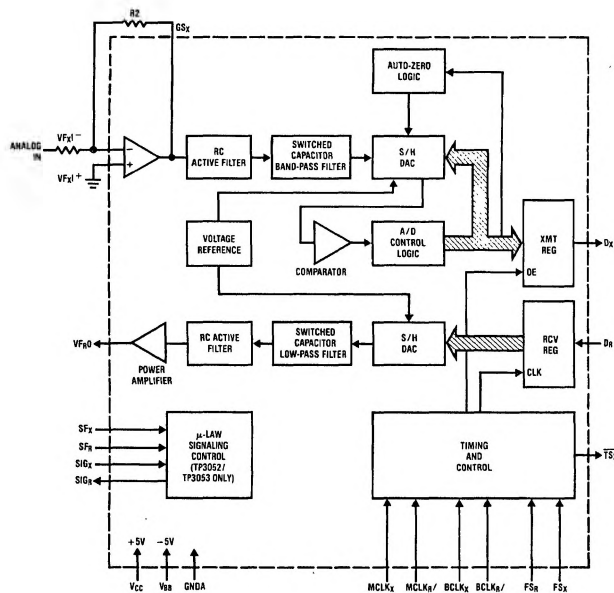


FIGURE 1

TL/H/5510-2

Pin Description

Symbol	Function	Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.	SF_R	When high during FS_R , this input indicates a receive signal frame.
GNDA	Analog ground. All signals are referenced to this pin.	SIG_R	The eighth bit of the PCM data appears at this output after each receive signalling frame.
VF_{RO}	Analog output of the receive power amplifier.	SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.	SF_X	When high during FS_X , this input indicates a transmit signaling frame.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R . FS_R is an 8 kHz pulse train. See <i>Figures 2</i> and <i>3</i> for timing details.	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X . FS_X is an 8 kHz pulse train, see <i>Figures 2</i> and <i>3</i> for timing details.
$BCLK_R/CLKSEL$	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).	$BCLK_X$	The bit clock which shifts out the PCM data on D_X . May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
$MCLK_R/PDN$	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.	D_X	The TRI-STATE® PCM data output which is enabled by FS_X .
		$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
		GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
		$VF_X ^-$	Inverting input of the transmit input amplifier.
		$VF_X +$	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the D_X and V_{FRO} outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R/PDN$ pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R/PDN$ pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X , will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R/PDN$ pin can be used as a power-down control. A low level on $MCLK_R/PDN$ powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R/CLKSEL$ can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R/CLKSEL$ pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R/CLKSEL$. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_X/R$.

TABLE 1. Selection of Master Clock Frequencies

BCLK _R /CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3053 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048

MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 53, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R/PDN$ pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R , must be one bit clock period long, with timing relationships specified in Figure 2. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the TP5116A/56A long frame mode, both the frame sync pulses, FS_X and FS_R , must be three or more bit clock periods long, with timing relationships specified in Figure 3. Based on the transmit frame sync, FS_X , the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R , will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 and TP3053 μ -law COMBOs contain circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications, and the TP3053 for long frame sync applications, although the TP3053 may also be used in short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Functional Description (Continued)

Signaling for the TP3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as " $\frac{1}{2}$ " to minimize noise and distortion. This short frame signaling may also be implemented using the TP3053, providing SF_R and SF_X are left open circuit or tied low. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the TP3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the TP3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R , which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the " $\frac{1}{2}$ " step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC

active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ -law (TP3052, TP3053, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μ s (due to the transmit filter) plus 125 μ s (due to encoding delay), which totals 290 μ s. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ -law (TP3052, TP3053, TP3054) and the 5th order low pass filter corrects for the $\sin x/x$ attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R , the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μ s later the decoder DAC output is updated. The total decoder delay is $\sim 10 \mu$ s (decoder update) plus 110 μ s (filter delay) plus 62.5 μ s ($\frac{1}{2}$ frame), which gives approximately 180 μ s.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
V_{BB} to GND	-7V
Voltage at any Analog Input or Output	$V_{CC} + 0.3V$ to $V_{BB} - 0.3V$

Voltage at any Digital Input or Output	$V_{CC} + 0.3V$ to $GND - 0.3V$
Operating Temperature Range	-25°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD (Human Body Model)	2000V
Latch-Up Immunity	= 100 mA on any Pin

Electrical Characteristics Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$ by correlation with 100% electrical testing at $T_A = 25^\circ C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	$D_X, I_L = 3.2 \text{ mA}$ $SIG_R, I_L = 1.0 \text{ mA}$ $TS_X, I_L = 3.2 \text{ mA}$, Open Drain			0.4 0.4 0.4	V V V
V_{OH}	Output High Voltage	$D_X, I_H = -3.2 \text{ mA}$ $SIG_R, I_H = -1.0 \text{ mA}$	2.4 2.4			V V
I_{IL}	Input Low Current	$GND \leq V_{IN} \leq V_{IL}$, All Digital Inputs	-10		10	μA
I_{IH}	Input High Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	-10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	$D_X, GND \leq V_O \leq V_{CC}$	-10		10	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_{LXA}	Input Leakage Current	$-2.5V \leq V \leq +2.5V$, $V_{FX}I^+$ or $V_{FX}I^-$	-200		200	nA
R_{IXA}	Input Resistance	$-2.5V \leq V \leq +2.5V$, $V_{FX}I^+$ or $V_{FX}I^-$	10			M Ω
R_{OXA}	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_{LXA}	Load Resistance	GS_X	10			k Ω
C_{LXA}	Load Capacitance	GS_X			50	pF
V_{OXA}	Output Dynamic Range	$GS_X, R_L \geq 10 \text{ k}\Omega$	-2.8		2.8	V
A_{VXA}	Voltage Gain	$V_{FX}I^+$ to GS_X	5000			V/V
F_{UXA}	Unity Gain Bandwidth		1	2		MHz
V_{OSXA}	Offset Voltage		-20		20	mV
V_{CMXA}	Common-Mode Voltage	$CMRR_X > 60 \text{ dB}$	-2.5		2.5	V
$CMRR_X$	Common-Mode Rejection Ratio	DC Test	60			dB
$PSRR_X$	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_{ORF}	Output Resistance	Pin $V_{FR}O$		1	3	Ω
R_{LRF}	Load Resistance	$V_{FR}O = \pm 2.5V$	600			Ω
C_{LRF}	Load Capacitance				500	pF
V_{OSRO}	Output DC Offset Voltage		-200		200	mV
POWER DISSIPATION (ALL DEVICES)						
I_{CC0}	Power-Down Current	No Load (Note)		0.5	1.5	mA
I_{BB0}	Power-Down Current	No Load (Note)		0.05	0.3	mA
I_{CC1}	Power-Up Active Current	No Load		6.0	9.0	mA
I_{BB1}	Power-Up Active Current	No Load		6.0	9.0	mA

Note: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Timing Specifications

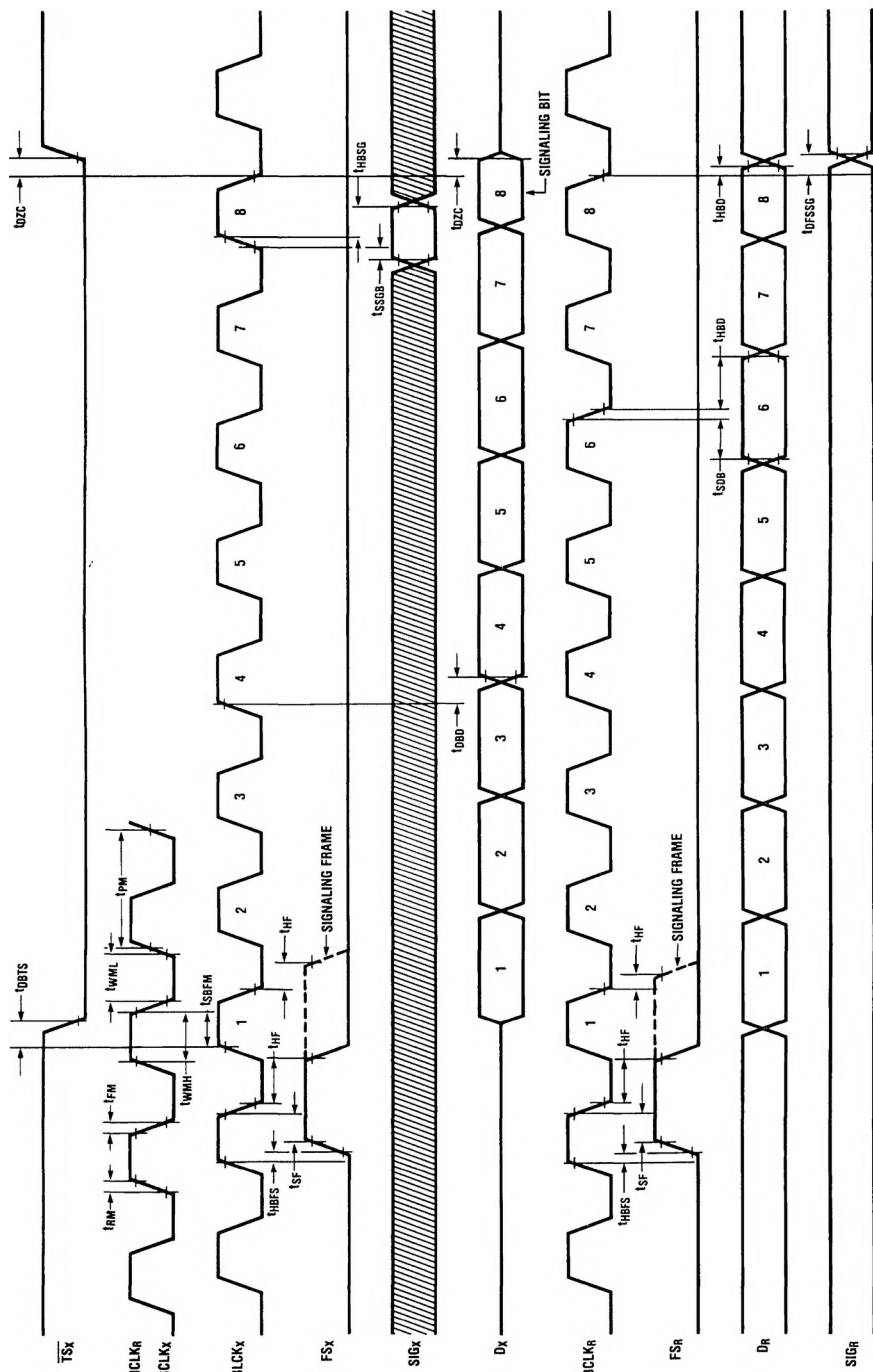
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Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the BCLK _R /CLKSEL Pin. MCLK _X and MCLK _R		1.536 1.544 2.048		MHz MHz MHz
t_{RM}	Rise Time of Master Clock	MCLK _X and MCLK _R			50	ns
t_{FM}	Fall Time of Master Clock	MCLK _X and MCLK _R			50	ns
t_{PB}	Period of Bit Clock		485	488	15725	ns
t_{RB}	Rise Time of Bit Clock	BCLK _X and BCLK _R			50	ns
t_{FB}	Fall Time of Bit Clock	BCLK _X and BCLK _R			50	ns
t_{WMH}	Width of Master Clock High	MCLK _X and MCLK _R	160			ns
t_{WML}	Width of Master Clock Low	MCLK _X and MCLK _R	160			ns
t_{SBFM}	Set-Up Time from BCLK _X High to MCLK _X Falling Edge	First Bit Clock after the Leading Edge of FS _X	100			ns
t_{SFFM}	Set-Up Time from FS _X High to MCLK _X Falling Edge	Long Frame Only	100			ns
t_{WBH}	Width of Bit Clock High	$V_{IH} = 2.2V$	160			ns
t_{WBL}	Width of Bit Clock Low	$V_{IL} = 0.6V$	160			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from BCLK _X High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		140	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from BCLK _X Low to Data Output Disabled	$C_L = 0$ pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS _X or BCLK _X , Whichever Comes Later	$C_L = 0$ pF to 150 pF	20		165	ns
t_{SSFF}	Set-Up Time from SF _{X/R} High to FS _{X/R}	TP3053 Only	60			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to BCLK _{X/R} Clock	TP3053 Only	60			ns
t_{SSGB}	Set-Up Time from SIG _X to BCLK _X	TP3052 and TP3053	100			ns
t_{HBSG}	Hold Time from BCLK _X High to SIG _X	TP3052 and TP3053	50			ns
t_{SDB}	Set-Up Time from D _R Valid to BCLK _{R/X} Low		50			ns
t_{HBD}	Hold Time from BCLK _{R/X} Low to D _R Invalid		50			ns
t_{HBSF}	Hold Time from BCLK _{X/R} Low to Signaling Frame Sync	TP3053 Only	100			ns
t_{SF}	Set-Up Time from FS _{X/R} to BCLK _{X/R} Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	50			ns
t_{HF}	Hold Time from BCLK _{X/R} Low to FS _{X/R} Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS _X or FS _R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

Timing Diagrams

TL/H/5510-3

FIGURE 2. Short Frame Sync Timing



Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$ by correlation with 100% electrical testing at $T_A = 25^\circ C$. All other limits are assured by correlation with other production tests and/or product design and characterization. $G_{NDA} = 0V$, $f = 1.02$ kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity gain non-inverting. Typical values specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600 Ω) 0 dBm0		1.2276		V _{rms}
t _{MAX}		Max Overload Level TP3052, TP3053, TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		2.501 2.492		V _{PK} V _{PK}
G _{XA}	Transmit Gain, Absolute	T _A = 25°C, V _{CC} = 5V, V _{BB} = -5V Input at G _{SX} = 0 dBm0 at 1020 Hz TP3052/53/54/57 TP3054-1/57-1	-0.15 -0.20		0.15 0.20	dB dB
G _{XR}	Transmit Gain, Relative to G _{XA}	f = 16 Hz f = 50 Hz f = 60 Hz (TP3054-1/57-1) f = 60 Hz (TP3054/57) f = 200 Hz f = 300 Hz - 3000 Hz f = 3300 Hz f = 3400 Hz (TP3052/53/54/57) f = 3400 Hz (TP3054-1/57-1) f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	-1.8 -0.15 -0.35 -0.7 -0.95		-40 -30 -22 -26 -0.1 0.15 0.05 0 0.05 -14 -32	dB dB dB dB dB dB dB dB dB dB
G _{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G _{XA}	-0.1		0.1	dB
G _{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G _{XA}	-0.05		0.05	dB
G _{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = -10 dBm0 V _{F_{XI}} + = -40 dBm0 to +3 dBm0 V _{F_{XI}} + = -50 dBm0 to -40 dBm0 V _{F_{XI}} + = -55 dBm0 to -50 dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB dB dB
G _{RA}	Receive Gain, Absolute	T _A = 25°C, V _{CC} = 5V, V _{BB} = -5V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz TP3052/53/54/57 TP3054-1/57-1	-0.15 -0.20		0.15 0.20	dB dB
G _{RR}	Receive Gain, Relative to G _{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	-0.15 -0.35 -0.7		0.15 0.05 0 -14	dB dB dB dB
G _{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G _{RA}	-0.1		0.1	dB
G _{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G _{RA}	-0.05		0.05	dB
G _{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level = -40 dBm0 to +3 dBm0 = -40 dBm0 to +3 dBm0 (TP3054-1/57-1 only) = -50 dBm0 to -40 dBm0 = -55 dBm0 to -50 dBm0	-0.2 -0.25 -0.4 -1.2		0.2 0.25 0.4 1.2	dB dB dB dB
V _{RO}	Receive Output Drive Level	R _L = 600 Ω	-2.5		2.5	V

Transmission Characteristics (Continued) Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$ by correlation with 100% electrical testing at $T_A = 25^\circ C$. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, $f = 1.02$ kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D _{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D _{XR}	Transmit Delay, Relative to D _{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D _{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D _{RR}	Receive Delay, Relative to D _{RA}	f = 500 Hz–1000 Hz	–40	–25		μs
		f = 1000 Hz–1600 Hz	–30	–20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N _{XC}	Transmit Noise, C Message Weighted	TP3052, TP3053, TP3054 TP3054-1 (Note 1)		12	15 16	dBrnC0 dBrnC0
N _{XP}	Transmit Noise, P Message Weighted	TP3057 TP3057-1 (Note 1)		–74	– 67 – 66	dBm0p dBm0p
N _{RC}	Receive Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero — TP3052/53/54 TP3054-1		8	11 13	dBrnC0 dBrnC0
N _{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero — TP3057-1		–82	– 79 – 77	dBm0p dBm0p
N _{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, V _{FX1} ⁺ = 0 Vrms			–53	dBm0
PPSR _X	Positive Power Supply Rejection, Transmit	V _{FX1} ⁺ = –50 dBm0 V _{CC} = 5.0 V _{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	40			dB
NPSR _X	Negative Power Supply Rejection, Transmit	V _{FX1} ⁺ = –50 dBm0 V _{BB} = –5.0 V _{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	40			dB
PPSR _R	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V _{CC} = 5.0 V _{DC} + 100 mVrms Measure V _{FR0}				
		f = 0 Hz–4000 Hz	40			dB
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB
		f = 0–4 kHz (TP3054-1/57-1)	38			dB
		f = 4–50 kHz (TP3054-1/57-1)	35			dB
NPSR _R	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V _{BB} = –5.0 V _{DC} + 100 mVrms Measure V _{FR0}				
		f = 0 Hz–4000 Hz	40			dB
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB

Transmission Characteristics (Continued) Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$ by correlation with 100% electrical testing at $T_A = 25^\circ C$. All other limits are assured by correlation with other production tests and/or product design and characterization. $G_{NDA} = 0V$, $f = 1.02$ kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R . 4600 Hz–7600 Hz 7600 Hz–8400 Hz 8400 Hz–100,000 Hz			–30 –30 –40 –30	dB dB dB dB

DISTORTION

STD _X STD _R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3) Level = 3.0 dBm0 = 0 dBm0 to –30 dBm0 = –40 dBm0 XMT RCV = –55 dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
SFD _X	Single Frequency Distortion, Transmit				– 46	dB
SFD _R	Single Frequency Distortion, Receive				– 46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $VF_X^+ = -4$ dBm0 to -21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			– 41	dB

CROSSTALK

CT _{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	$f = 300$ Hz–3400 Hz $D_R =$ Quiet PCM Code		–90	– 75	dB
CT _{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	$f = 300$ Hz–3400 Hz, $VF_X =$ Multitone (Note 2)		–90	– 70	dB

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3053, TP3054 μ -Law	TP3057 A-Law (Includes Even Bit Inversion)
V_{IN} (at GS _X) = + Full-Scale	1 0 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS _X) = 0V	$\begin{cases} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{cases}$	$\begin{matrix} 1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \end{matrix}$
V_{IN} (at GS _X) = – Full-Scale	0 0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

Note 1: Measured by extrapolation from the distortion test result at -50 dBm0.

Note 2: PPSR_X, NPSR_X, and CT_{R-X} are measured with a -50 dBm0 activation signal applied to $VF_X|$.

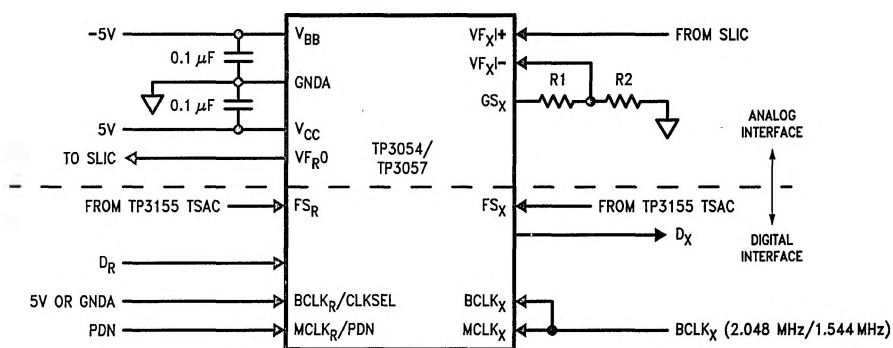
Note 3: Devices are measured using C message weighted filter for μ -Law and psophometric weighted filter for A-Law.

Applications Information (Continued)

TABLE II. Attenuator Tables for $Z1 = Z2 = 300\Omega$
(All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



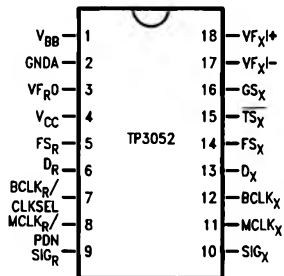
Note 1: $XMIT\ gain = 20 \times \log \left(\frac{R1 + R2}{R2} \right)$ where $(R1 + R2) > 10\text{ K}\Omega$.

FIGURE 4

TL/H/5510-6

Connection Diagrams (Continued)

Dual-In-Line Package

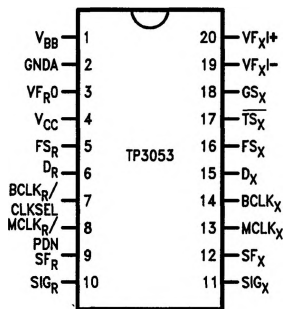


TL/H/5510-8

Top View

Order Number TP3052J
See NS Package Number J18A

Dual-In-Line Package

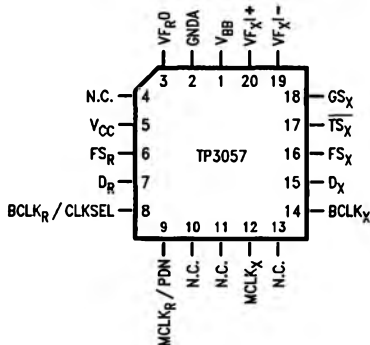


TL/H/5510-9

Top View

Order Number TP3053J
See NS Package Number J20A

Plastic Chip Carrier



TL/H/5510-7

Top View

Order Number TP3057V*
See NS Package Number V20A

*Available mid 1990