TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900 Series

TMP96C031Z

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-bit Microcontrollers

TMP96C031ZF

1. Outline and Device Characteristics

TMP96C031Z is high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP96C031ZF comes in a 64-pin flat package.

(1) Original 16-bit CPU

- TLCS-90 instruction mnemonic upward compatible.
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication / division and bit transfer/arithmetic instructions
- High-speed μ DMA :4 channels (1.6 μs/2 bytes @20MHz)

(2) Minimum instruction execution time : 200 ns (@20 MHz)

(3) External memory expansion

- Can be expanded up to16M-byte (for both programs and data).
- External data bus width selection pin (AM8/$\overline{16}$).
- Can mix 8- and 16-bit external data buses.
  ··· Dynamic data bus sizing

(4) 8-bit timer : 4 channels

(5) 16-bit timer : 1 channel

(6) Pattern generator : 4 bits, 2 channels

(7) Serial interface : 2 channels

(8) 6-bit A/D converter : 4 channels

(9) DRAM controller

(10) Watchdog timer

(11) Chip select/wait controller : 4 blocks

(12) Interrupt functions

- 3 CPU interrupts··· SWI instruction, priviledged violation, and Illegal instruction
- 12 internal interrupts
- 9 external interrupts

7-level priority can be set.

(13) I/O ports
37 pins

(14) Standby function : 3 HALT modes (RUN, IDLE, STOP)

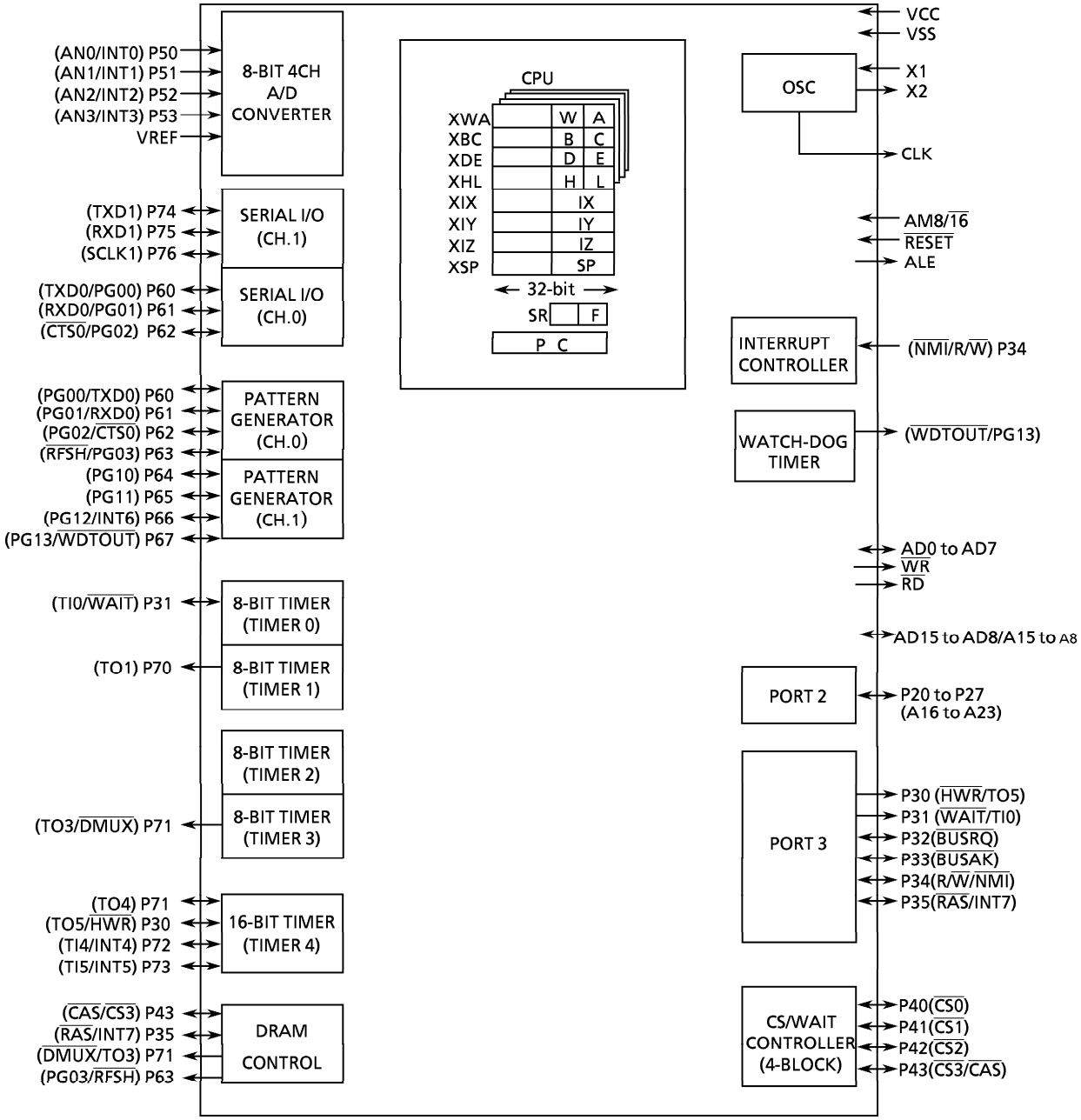


Figure1 TMP96C031Z Block Diagram

2. Pin Assignment and Function

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP96C031ZF.

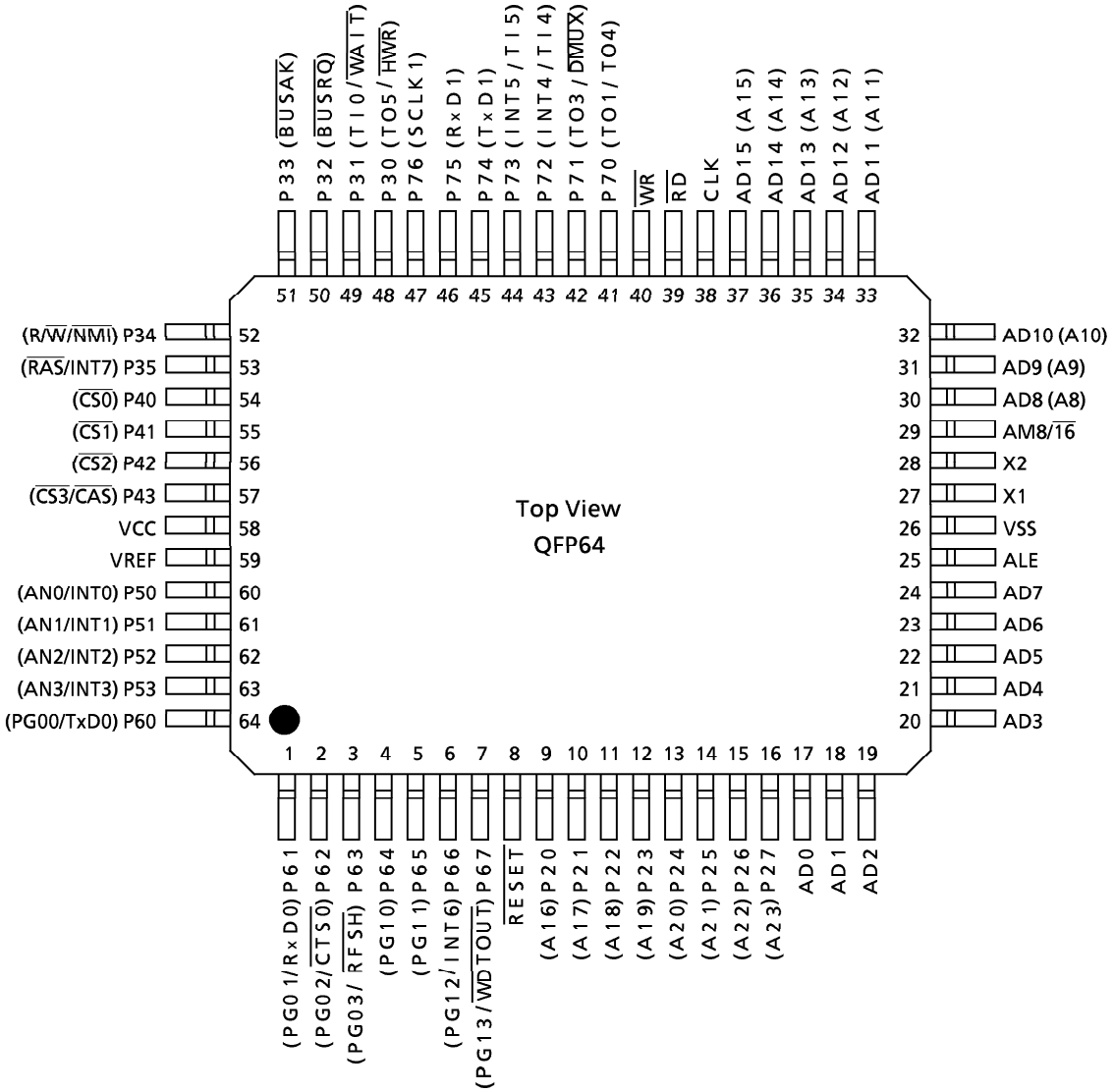


Figure2.1 Pin Assignment (64QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
AD0 to AD7	8	Tri-state	Address/data (lower): 0 to 7 for address/data bus
AD8 to AD15 A8 to A15	8	Tri-state Output	Address data (upper): 8 to 15 for address/data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resister) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 TO5 $\overline{HWR}$	1	I/O Output Output	Port 30: I/O port (with pull-up register) Timer output 5: Timer 4 output pin High write: Strobe signal for writing data on pins AD8 to 15
P31 TIO $\overline{WAIT}$	1	I/O Input Input	Port 31: I/O port (with pull-up register) Timer input 0: Timer 0 input Wait: Pin used to request CPU bus wait
P32 $\overline{BUSRQ}$	1	I/O Input	Port 32: I/O port (with pull-up register) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P33 $\overline{BUSAK}$	1	I/O Output	Port 33: I/O port (with pull-up register) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ.
P34 R/$\overline{W}$ $\overline{NMI}$	1	I/O Output Input	Port 34: I/O port (with pull-up register) Read/write: 1 represents read or dummy cycle; 0, write cycle. Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
P35 $\overline{RAS}$ INT7	1	I/O Output Input	Port 35: I/O port (with pull-up register) Row address strobe: Outputs RAS strobe for DRAM. Interrupt request pin 7: Interrupt request pin with rising edge.
P40 $\overline{CS0}$	1	Output Output	Port 40: Output port Chip select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	Output Output	Port 41: Output port Chip select 1: Outputs 0 if address is within specified address area.

Note : The internal I/O of this device cannot be accessed using an external DMA controller.

Pin name	Number of pins	I/O	Functions
P42 $\overline{CS2}$	1	Output Output	Port 42: Output port (with pull-up resister) Chip select 2: Outputs 0 if address is within specified address area.
P43 $\overline{CS3}$ $\overline{CAS}$	1	Output Output Output	Port 43: Output port (with pull-up resister) Chip select 3: Outputs 0 if address is within specified address area. Column address strobe : Output $\overline{CAS}$ strobe for DRAM if address is within specified address area.
VREF	1	Input	A/D convertor reference voltage input
P50 to P53 AN0 to AN3 INT0 to INT3	4	Input Input Input	Port 50 to 53: Input port Analog input: Input to A/D converter Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. Interrupt request pin 1: Interrupt request pin with programmable rising/falling edge. Interrupt request pin 2 to 3: Interrupt request pin with rising edge.
P60 TxD0 PG00	1	I/O Output Output	Port 60: I/O port Serial send data 0 Pattern generator port 00
P61 RxD0 PG01	1	I/O Input Output	Port 61: I/O port Serial receive data 0 Pattern generator port 01
P62 $\overline{CTS0}$ PG02	1	I/O Input Output	Port 62: I/O port Serial data send enable 0 (Clear to Send) Pattern generator port 02
P63 $\overline{RFSH}$ PG03	1	I/O Output Output	Port 63: I/O port Refresh out : This is a state signal output pin which indicates that the DRAM controller is in refresh cycle. Pattern generator port 03
P64 PG10	1	I/O Output	Port 64: I/O port Pattern generator port 10
P65 PG11	1	I/O Output	Port 65: I/O port Pattern generator port 11
P66 INT6 PG12	1	I/O Input Output	Port 66: I/O port Interrupt request pin 6 : Interrupt request pin with rising edge. Pattern generator port 12
P67 $\overline{WDTOUT}$ PG13	1	I/O Output Output	Port 67: I/O port Watchdog timer output pin Pattern generator port 13
P70 TO1 TO4	1	I/O Output Output	Port 70: I/O port Timer output 1: Timer 0 or 1 output pin Timer output 4: Timer 4 output pin

Pin name	Number of pins	I/O	Functions
P71 TO3 $\overline{DMUX}$	1	I/O Output Output	Port 71: I/O Port Timer output 3: Timer 2 or Timer 3 output pin DRAM address multiplexor : This pin outputs row address, column address, and selector select signal.
P72 INT4 TI4	1	I/O Input Input	Port 72: I/O Port Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge. Timer input 4: Timer 4 count/capture trigger signal input
P73 INT5 TI5	1	I/O Input Input	Port 73: I/O Port Interrupt request pin 5:Interrupt request pin with rising edge. Timer input 5: Timer 4 count/capture trigger signal input
P74 TxD1	1	I/O Output	Port 74: I/O Port Serial send data 1
P75 RxD1	1	I/O Input	Port 75: I/O Port Serial receive data 1
P76 SCLK1	1	I/O I/O	Port 76: I/O Port Serial clock I/O 1
CLK	1	Output	Clock output : Outputs「X1÷4」clock. Pulled-up during reset.
$\overline{RD}$	1	Output	Read: Strobe signal for reading external memory.
$\overline{WR}$	1	Output	Write: Strove signal for writing data on pins AD0 to 7.
AM8/$\overline{16}$	1	Input	Address mode : External data bus width selection pin. Set to "0" for fixed external 16-bit bus or for mixed external 8/16 bit bus and to "1" for fixed external 8-bit bus.
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resister)
ALE	1	Output	Address latch enable
X1/X2	1	I/O	Oscillator connecting pin
VCC	1		Power supply pin (+ 5 V) (All Vcc pins should be connected with the power supply pin.)
VSS	1		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : Pull-up /pull-down resister can be released from the pin by software.

3. Operation

This section describes in blocks the functions and basic operations of TMP96C031Z device.

Check the 「7. Care Points and Resection 」because of the Care Points etc are described.

3.1 CPU

TMP96C031Z device have a built-in high-performance 16-bit CPU (900_CPU). (For CPU operation, see TLCS-900 CPU in the previous section).

This section describes CPU functions unique to TMP96C031Z that are not described in the previous section.

3.1.1 Reset

To reset the TMP96C031Z, the $\overline{\text{RESET}}$ input must be kept at 0 for at least 10 system clocks (10 states: 1 μs with a 20 MHz system clock) within an operating voltage range and with a stable oscillation.

When reset is accepted, the CPU sets as follows:

- Program counter (PC) to 8000H.
- Stack pointer (XSP) for system mode to 100H.
- SYSM bit of status register (SR) to 1. (Sets to system mode.)
- IFF2 to 0 bits of status register to 111. (Sets mask register to interrupt level 7.)
- MAX bit of status register to 0. (Sets to minimum mode)
- Bits RFP2 to 0 of status register to 000. (Sets register banks to 0.)

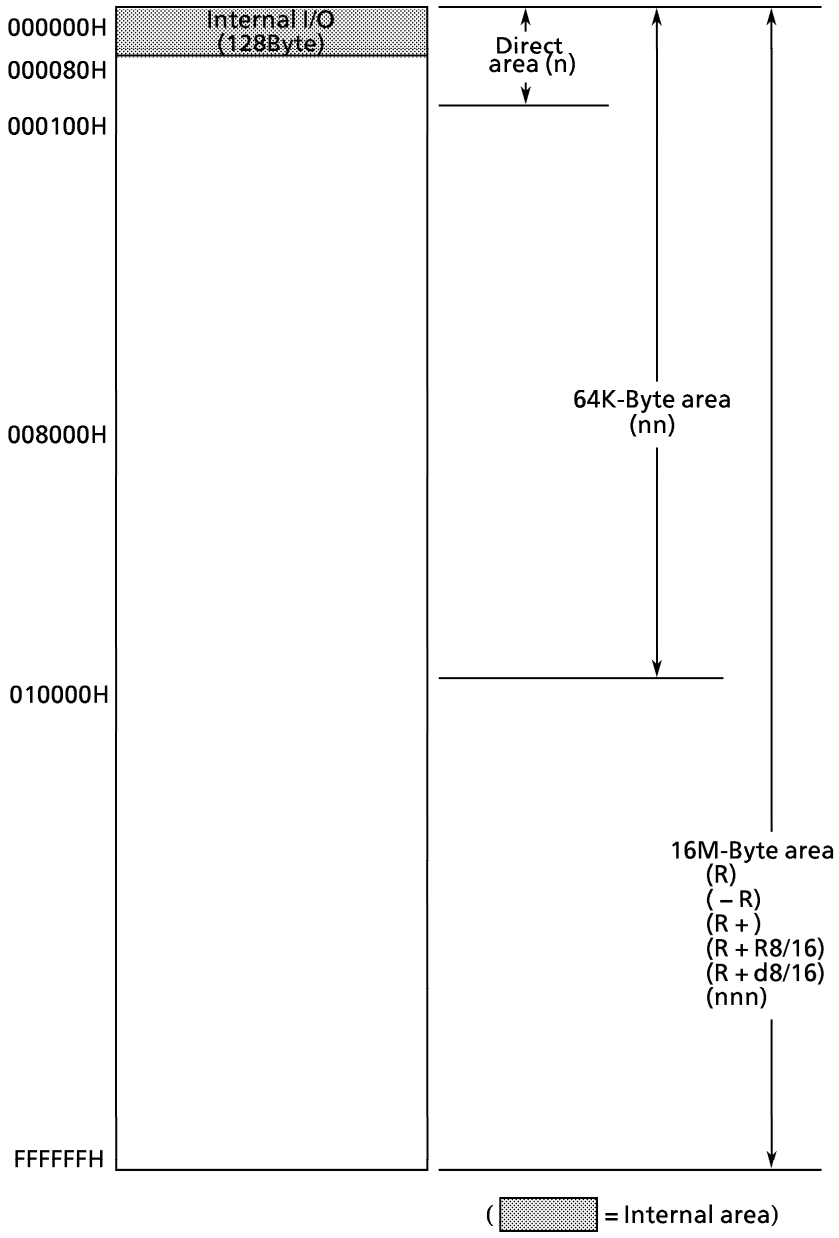
When reset is released, instruction execution starts from address 8000H. CPU internal registers other than the above are not changed.

When reset is accepted, processing for built-in I/Os, ports, and other pins is as follows

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input/output port mode (sets I/O ports to input ports).
- Pulls up the CLK pin to 1.
- Sets the ALE pin to 0.

3.2 Memory Map

Figure 3.2 is a memory map of the TMP96C031Z.



Note : The start address after reset is 8000H. Resetting sets the stack pointer (XSP) on the system mode side to 100H.

Figure3.2 Memory map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP96C031Z)

Parameter	Symbol	Rating	Unit
Power Supply voltage	V cc	– 0.5 to 6.5	V
Input voltage	V IN	– 0.5 to Vcc + 0.5	V
Output Current (total)	Σ IOL	100	mA
Output Current (total)	Σ IOH	– 100	mA
Power Dissipation (Ta = 70℃)	P D	600	mW
Soldering Temperature (10 s)	T SOLDER	260	℃
Storage temperature	T STG	– 65 to 150	℃
Operating temperature	T OPR	– 20 to 70	℃

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (TMP96C031Z)

Vcc = 5 V ± 10%, Ta = – 20 to 70℃ (Typical values are for Ta = 25℃ and Vcc = 5 V.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (AD0 to 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET,NMI,INT0 AM8/16 X1	V IL V IL1 V IL2 V IL3 V IL4		– 0.3 – 0.3 – 0.3 – 0.3 – 0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V
Input High Voltage (AD0 to 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET, NMI, INT0 AM8/16 X1	V IH V IH1 V IH2 V IH3 V IH4		2.2 0.7 Vcc 0.75 Vcc Vcc – 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V OL	I OL = 1.6 mA		0.45	V
Output High Voltage	V OH V OH1 V OH2	I OH = – 400 μA I OH = – 100 μA I OH = – 20 μA	2.4 0.75 Vcc 0.9 Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I DAR	V EXT = 1.5 V R EXT = 1.1 kΩ	– 1.0	– 3.5	mA
Input Leakage Current Output Leakage Current	I LI I LO	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE STOP (Ta = – 20 to 70℃) STOP (Ta = 0 to 50℃)	I cc	t osc = 20 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2	30 (Typ) 2.0 (Typ) 0.2 (Typ)	60 10 50 10	mA mA μA μA
Power Down Voltage (@STOP, RAM Back up)	V STOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc	2.0	6.0	V
RESET Pull Up Resistor	R RST		50	150	kΩ
Pin Capacitance	C IO	tosc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 (P50)	V TH		0.4	1.0 (Typ)	V
Programmable Pull Down Resistor	R KL		10	80	kΩ
Programmable Pull Up Resistor	R KH		50	150	kΩ

Note : I-DAR is guaranteed for a total of up to 8 ports.

4.3 AC Electrical Characteristics (TMP96C031ZF)

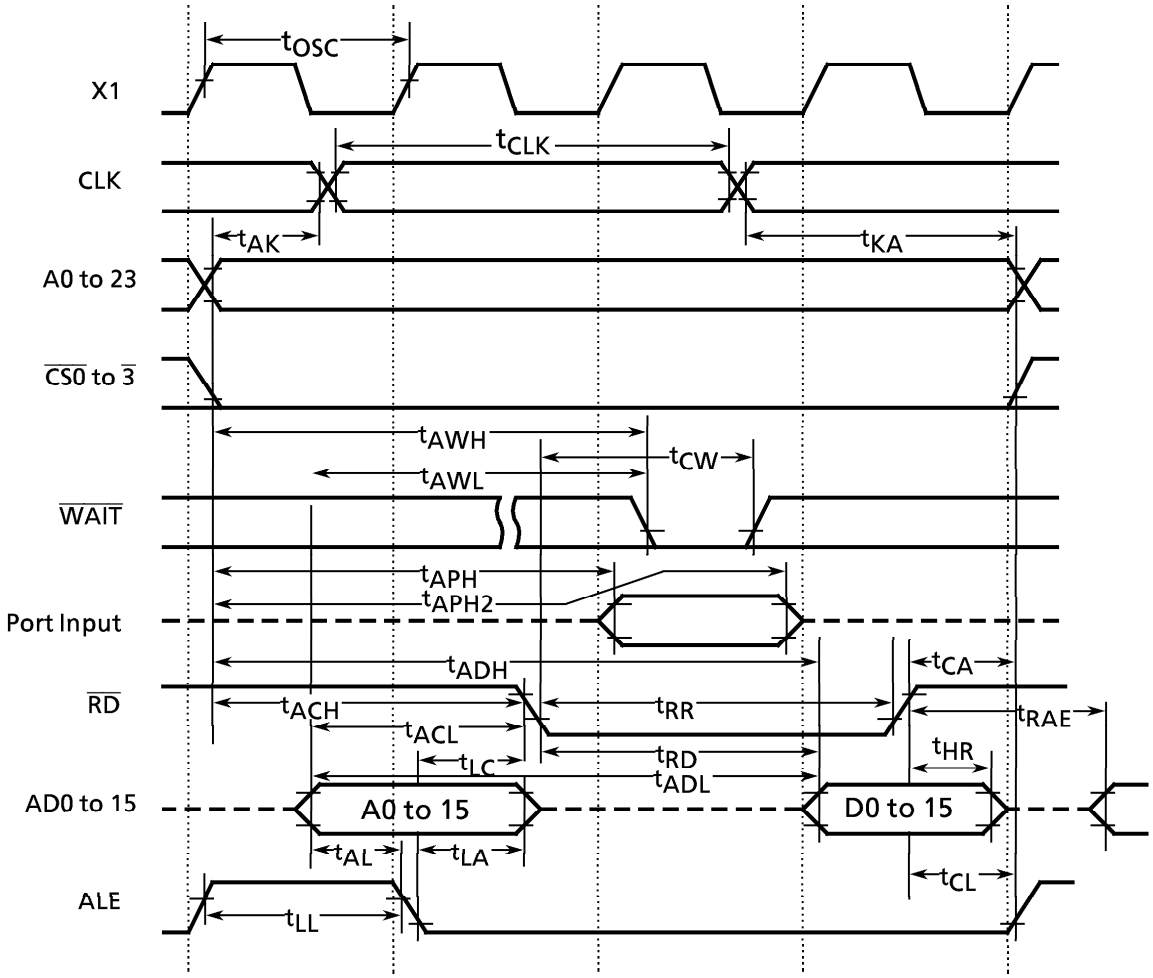
Vcc = 5 V ± 10% , TA = – 20 to 70℃
(4 MHz to 20 MHz)

No.	Paramerer	Symbol	Voriable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	250	62.5		50		ns
2	CLK width	t_{CLK}	2x – 40		85		60		ns
3	A0 to 23 Valid → CLK Hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK Valid → A0 to 23 Hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to 15 Valid → ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall → A0 to 15 Hold	t_{LA}	0.5x – 15		16		10		ns
7	ALE High width	t_{LL}	x – 40		23		10		ns
8	ALE fall → $\overline{RD}/\overline{WR}$ fall	t_{LC}	0.5x – 30		1		– 5		ns
9	$\overline{RD}/\overline{WR}$ rise → ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to 15 Valid → $\overline{RD}/\overline{WR}$ fall	t_{ACL}	x – 25		38		25		ns
11	A0 to 23 Valid → $\overline{RD}/\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}/\overline{WR}$ rise → A0 to 23 Hold	t_{CA}	0.5x – 20		11		5		ns
13	A0 to 15 Valid → D0 to 15 input	t_{ADL}		3.0x – 45		143		105	ns
14	A0 to 23 Valid → D0 to 15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$fall → D0 to 15 input	t_{RD}		2.0x – 50		75		50	ns
16	$\overline{RD}$ Low width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$rise → D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$rise → A0 to 15 output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ Low width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to 15 Valid → $\overline{WR}$rise	t_{DW}	2.0x – 50		75		50		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5x – 10		21		15		ns
22	A0 to 23 Valid → $\overline{WAIT}$ input ($^{1WAIT}_{+n\ mode}$)	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to 15 Valid → $\overline{WAIT}$ input ($^{1WAIT}_{+n\ mode}$)	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}/\overline{WR}$ fall →$\overline{WAIT}$ Hold ($^{1WAIT}_{+n\ mode}$)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to 23 Valid → PORT input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to 23 Valid → PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise → PORT Valid	t_{CP}		200		200		200	ns

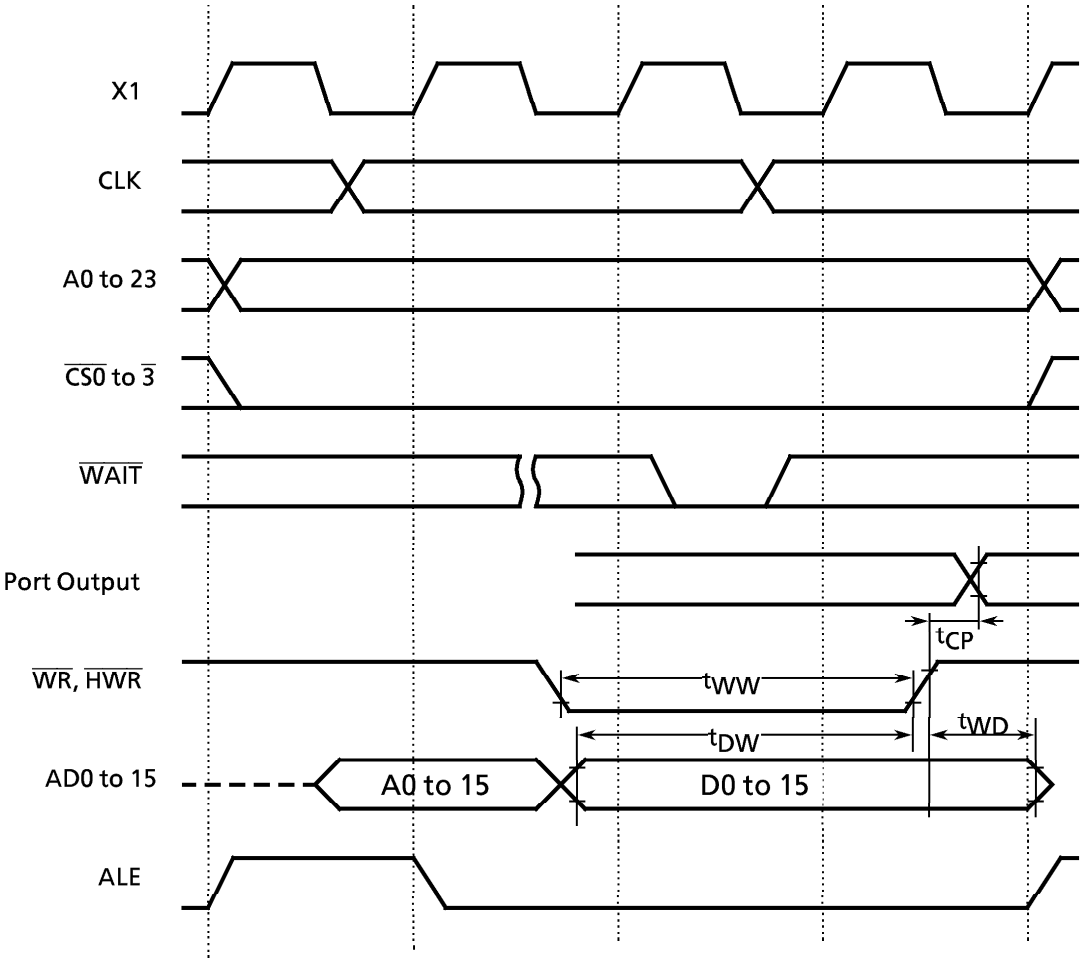
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK, $\overline{CS0}$ to $\overline{CS3}$)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

(1) Read Cycle


X1
CLK
A0 to 23
CS0 to 3
WAIT
Port Input
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tADH
tCA
tACH
tRR
tRAE
tACL
tLC
tRD
tADL
tHR
A0 to 15
D0 to 15
tAL
tLA
tCL
tLL

(2) Write Cycle



4.4 DRAM Control AC Characteristics (TMP96C031Z)

Vcc = 5 V ± 10% , TA = – 20 to 70℃
(4 MHz to 20 MHz)

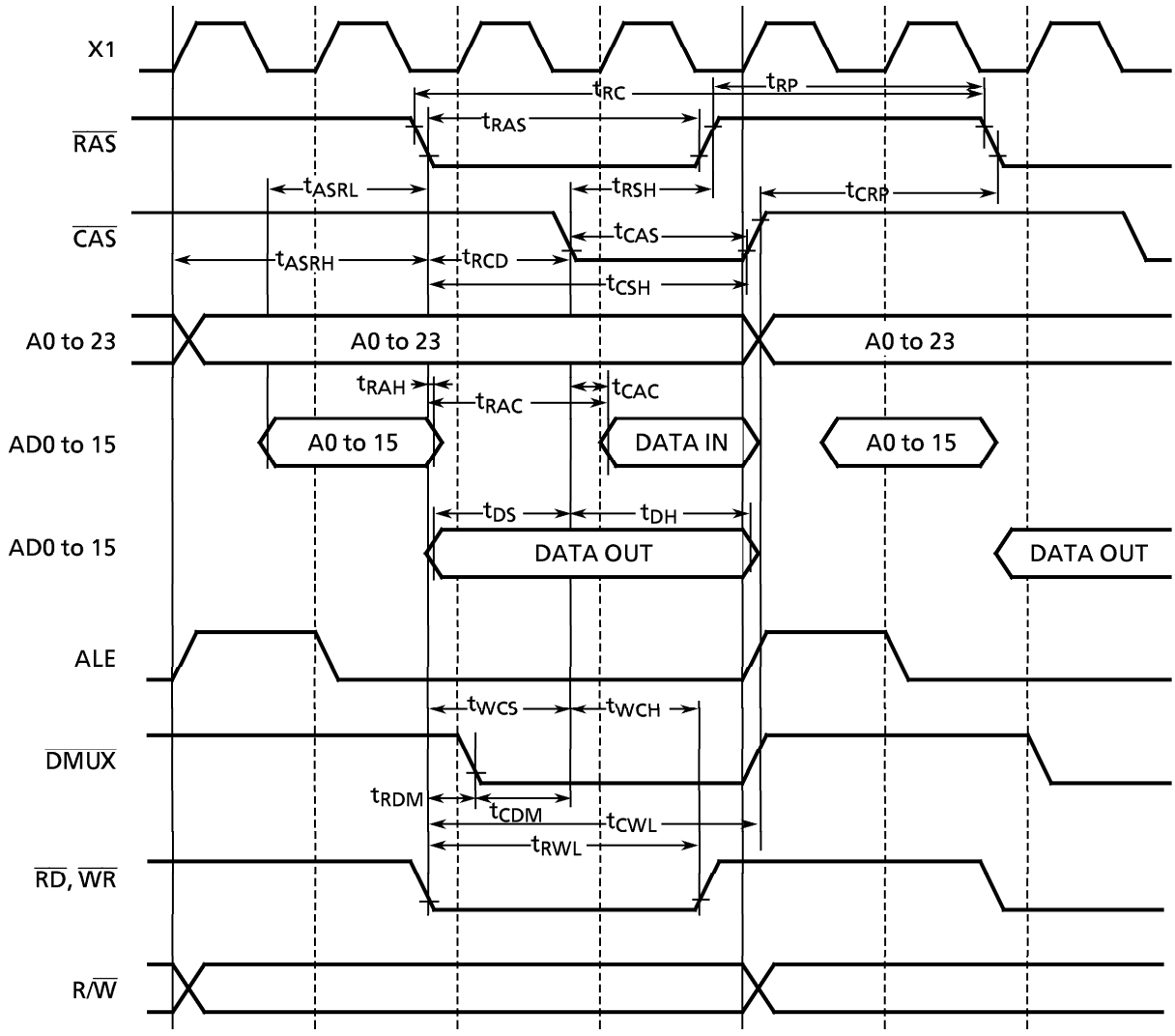
No.	Parameter	Symbol	Voriable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	$\overline{RAS}$ cycle time	t_{RC}	4X-10		240		190		ns
2	$\overline{RAS}$ fall → data input	t_{RAC}		2X-50		75		50	ns
3	$\overline{CAS}$ fall → data input	t_{CAC}		1X-42		20.5		8	ns
4	$\overline{RAS}$ high pulse width	t_{RP}	2X-40		85		60		ns
5	$\overline{RAS}$ low pulse width	t_{RAS}	2X-20		105		80		ns
6	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1X-25		38		25		ns
7	$\overline{RAS}$ fall → $\overline{CAS}$ rise	t_{CSH}	2X-20		105		80		ns
8	$\overline{CAS}$ low pulse width	t_{CAS}	1.5X-30		64		45		ns
9	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1X-10	1X + 10	53	73	40	60	ns
10	$\overline{CAS}$ rise → $\overline{RAS}$ fall	t_{CRP}	1.5X-50		44		25		ns
11	$\overline{RAS}$ fall → A0-15 hold	t_{RAH}	-30		-30		-30		ns
12	$A_{0\ to\ 15}$ valid → $\overline{RAS}$ fall	t_{ASRL}	1X-10		53		40		ns
13	$A_{0\ to\ 23}$ valid → $\overline{RAS}$ fall	t_{ASRH}	1.5X-10		84		65		ns
14	$\overline{WR}$ fall → $\overline{RAS}$ rise	t_{RWL}	2X-50		75		50		ns
15	$\overline{WR}$ fall → $\overline{CAS}$ rise	t_{CWL}	2X-50		75		50		ns
16	Data output → $\overline{CAS}$ fall setup	t_{DS}	1X-30		33		20		ns
17	$\overline{CAS}$ fall → data output hold	t_{DH}	1.5X-50		44		25		ns
18	$\overline{RAS}$ fall → data output hold	t_{DHR}	2.5X-50		106		75		ns
19	$\overline{WR}$ fall → CAS fall setup	t_{WCS}	1X-30		33		20		ns
20	$\overline{CAS}$ fall → WR hold	t_{WCH}	1X-30		33		20		ns
21	$\overline{RAS}$ fall → DMUX fall	t_{RDM}	0.5X-10	0.5X	21	31	15	25	ns
22	$\overline{DMUX}$ fall → $\overline{CAS}$ fall	t_{CDM}	0.5X	0.5X + 10	31	41	25	35	ns
23	$\overline{RAS}$ fall → $\overline{CAS}$ rise	t_{CHR}*1	2X-50		75		50		ns
24	$\overline{RAS}$ rise → $\overline{CAS}$ fall	t_{RPC}*	1.5X-30		64		45		ns
25	$\overline{CAS}$ high pulse width	t_{CP}*	1.5X-60		34		15		ns
26	$\overline{CAS}$ fall → $\overline{RAS}$ fall	t_{CSR}*	0.5X-10		21		15		ns
27	$\overline{RAS}$ low pulse width	t_{RASS}*2	2000X		125		100		μs
28	$\overline{RAS}$ precharge time	t_{RPS}*2	4X-50		200		150		ns
29	$\overline{CAS}$ hold time	t_{CHS}*2	-10		-10		-10		ns
30	$\overline{RFSH}$ fall → $\overline{CAS}$ fall	t_{CFL}*	1X-10		53		40		ns
31	$\overline{CAS}$ rise → $\overline{RFSH}$ rise	t_{CFH}*	0.5X-10		21		15		ns

*1 $\overline{CAS}$ before $\overline{RAS}$ interval refresh mode
*2 $\overline{CAS}$ before $\overline{RAS}$ self-refresh mode
* Both refresh modes

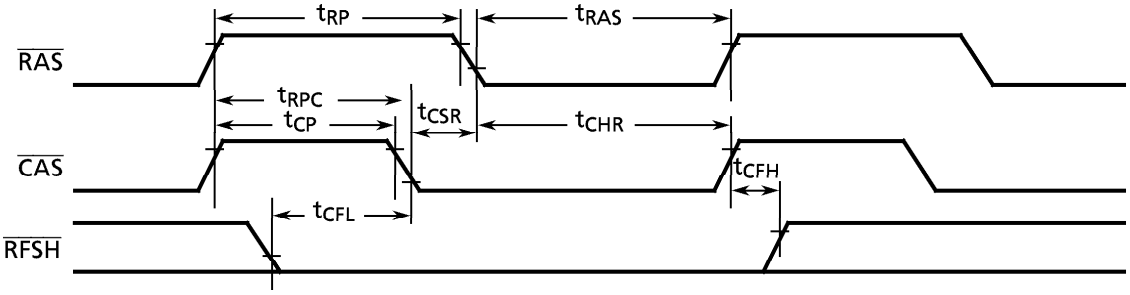
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

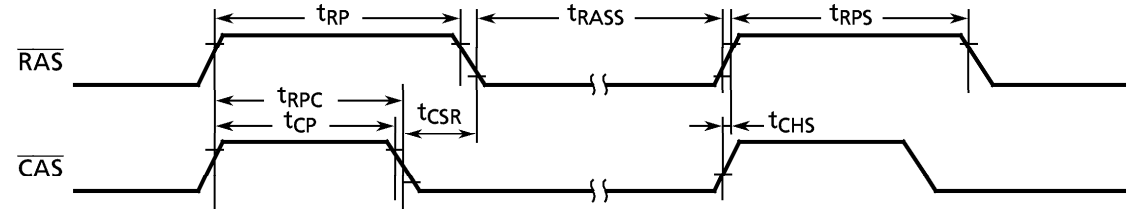
(1) Read/Write Access Cycle



(2) $\overline{CAS}$ before $\overline{RAS}$ interval refresh cycle



(3) $\overline{CAS}$ before $\overline{RAS}$ self-refresh cycle



4.5 A/D Conversion Characteristics

Vcc = 5 V ± 10% TA = – 20 to 70°C

Parameter	Symbol	Min	Typ.	Max	Unit
Analog reference voltage	V_{REF}	Vcc – 1.5		Vcc	V
Analog reference voltage	A_{GND}	Vss		Vss	
Analog input voltage range	V_{AIN}	Vss		Vcc	
Anlog current for analog reference voltage	I_{REF}		0.5	1.5	mA
Total error	Error(Quantize error of ± 0.5 LSB not included)			2.0	LSB

4.6 Serial Channel Timing – I/O Interface Mode

(1) SCLK Input Mode

Vcc = 5 V ± 10% TA = – 20 to 70°C

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		1		0.8		μs
Output Data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 – 5X – 50		137		100		ns
SCLK rising edge→ Output Data hold	t_{OHS}	5X – 100		212		150		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} – 5X – 100		587		450	ns

(2) SCLK Output Mode

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16X	8192X	1	512	0.8	409.6	μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} – 2X – 150		725		550		ns
SCLK rising edge→ Output Data hold	t_{OHS}	2X – 80		45		20		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} – 2X – 150		725		550	ns

4.7 Timer/Counter Input Clock (TI0, TI4, TI5)

Vcc = 5 V ± 10% TA = – 20 to 70°C

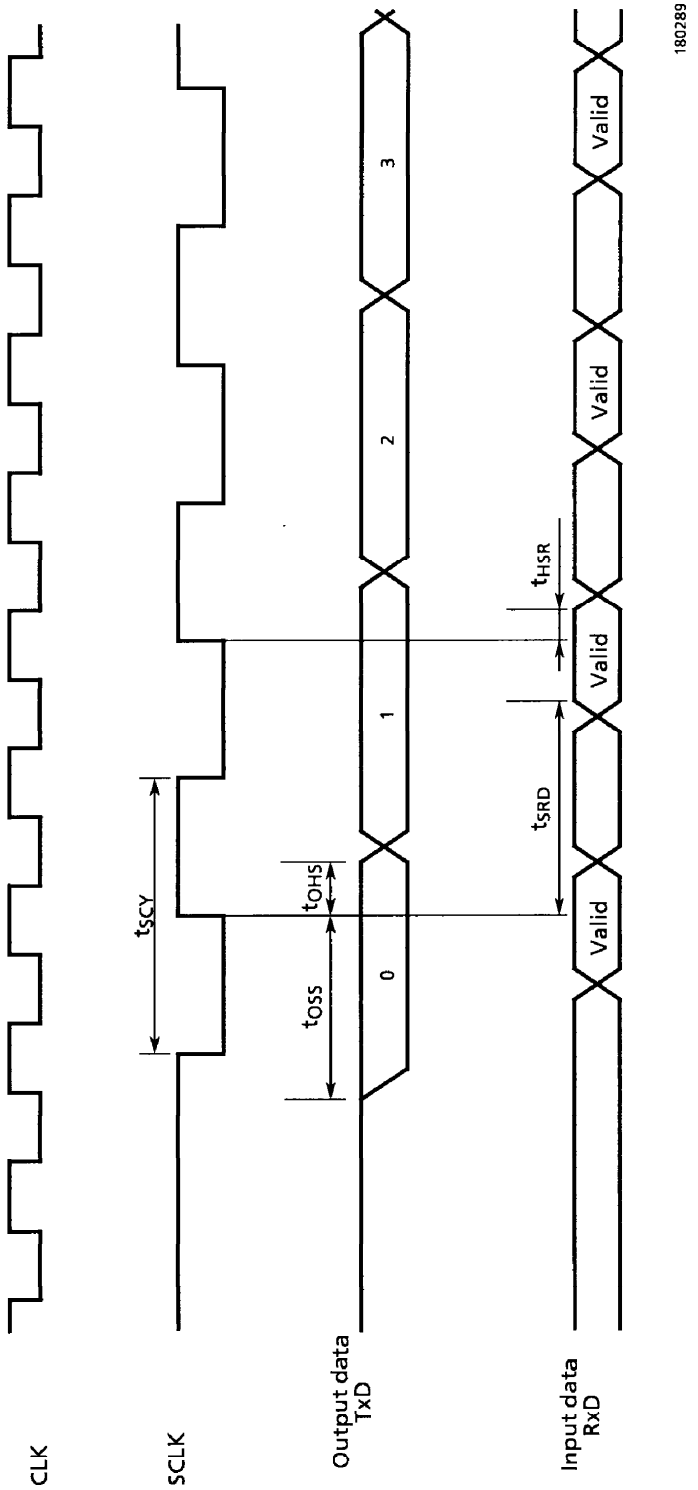
Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		600		500		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		290		240		ns
High level clock Pulse width	t_{VCKH}	4X + 40		290		240		ns

4.8 Interrupt Operation

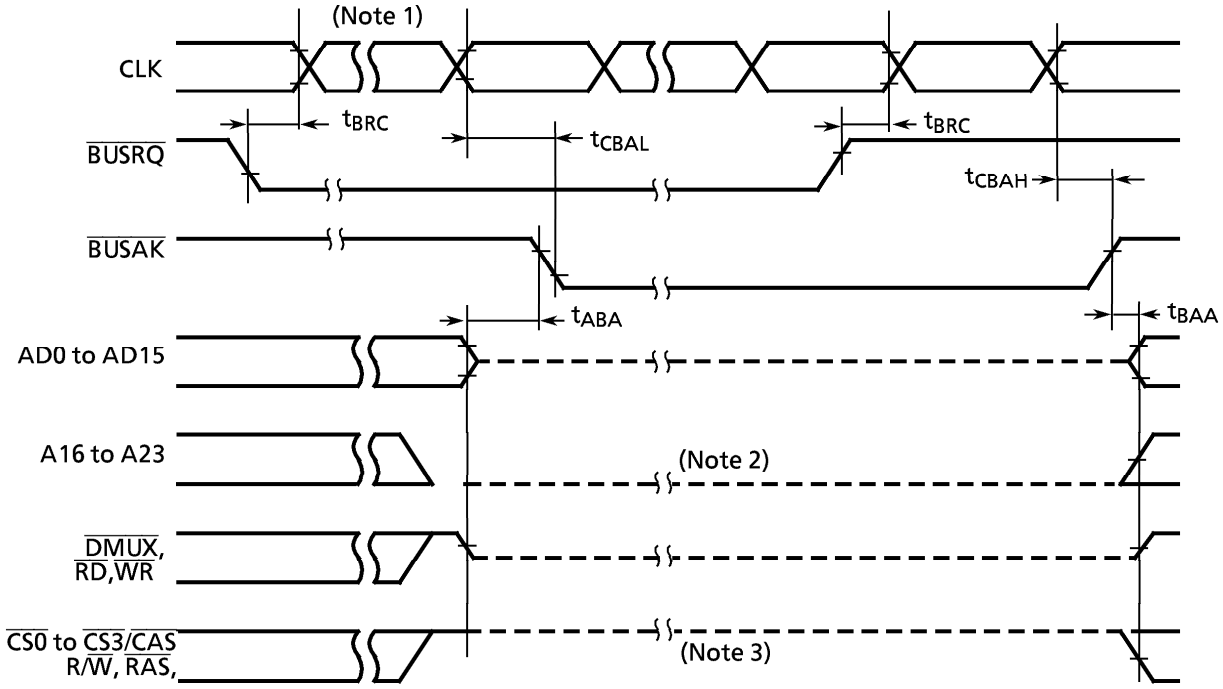
Vcc = 5 V ± 10% TA = – 20 to 70°C

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level Pulse width	t_{INTAL}	4X		250		200		ns
$\overline{NMI}$, INT0 High level Pulse width	t_{INTAH}	4X		250		200		ns
INT1 to INT7 Low level Pulse width	t_{INTBL}	8X + 100		600		500		ns
INT1 to INT7 High level Pulse width	t_{INTBH}	8X + 100		600		500		ns

4.9 Timing Chart for I/O Interface Mode



4.10 Timing Chart for Bus Request/BUS Acknowledge



Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{\text{BUSRQ}}$ set-up time for CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{\text{BUSAK}}$ falling edge	t_{CBAL}		2.0x + 120		214		220	ns
CLK→ $\overline{\text{BUSAK}}$ rising edge	t_{CBAH}		0.5x + 40		71		65	ns
Output Buffer is off to $\overline{\text{BUSAK}}$ ↓	t_{ABA}	0	80	0	80	0	80	ns
$\overline{\text{BUSAK}}$ ↑ to Output Buffer is on.	t_{BAA}	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the $\overline{\text{WAIT}}$ request is inactive, when the $\overline{\text{BUSRQ}}$ is set to "0" during "Wait" cycle.
Note 2 : An internal programmable pull-down resistor must be connected.
Note 3 : An internal programmable pull-up resistor must be connected.

4.11 Typical characteristics

Vcc = 5 V, Ta = 25°C, unless otherwise noted.

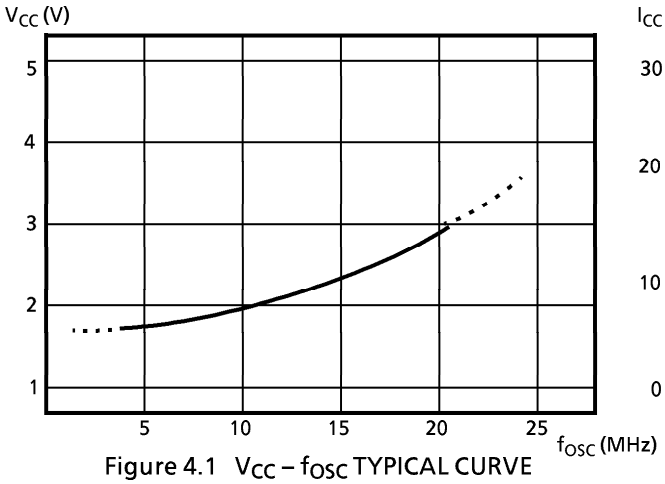


Figure 4.1 V_{CC} – f_{OSC} TYPICAL CURVE

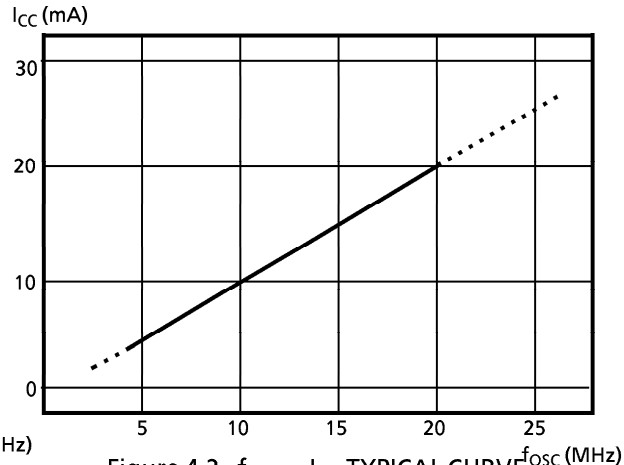


Figure 4.2 f_{OSC} – I_{CC} TYPICAL CURVE

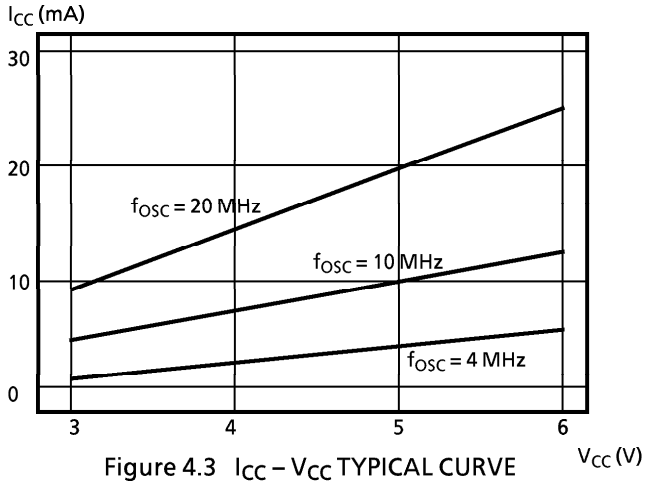


Figure 4.3 I_{CC} – V_{CC} TYPICAL CURVE

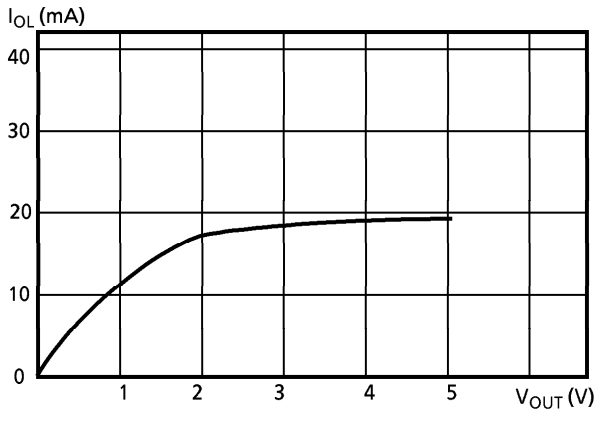


Figure 4.4 V_{OUT} – I_{OL} TYPICAL CURVE

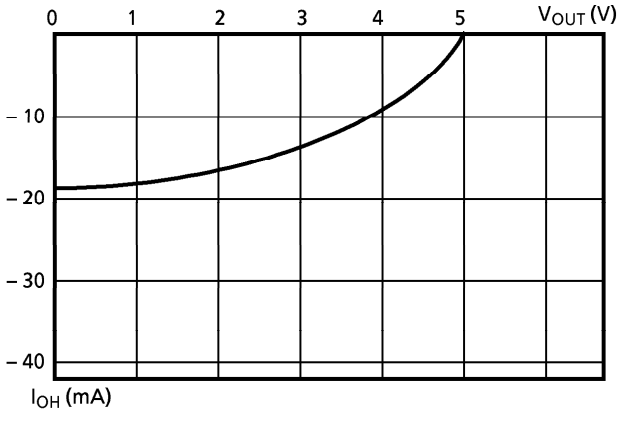


Figure 4.5 V_{OUT} – I_{OH} TYPICAL CURVE