TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/H Series

TMP95C063

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, $\overline{\text{NMI2}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontroller

TMP95C063F

1. Outline and Features

TMP95CO63F was developed as a high-speed, advanced 16-bit microcontroller for a range of mid- to large-scale equipment.

TMP95CO63F is presented in a 144-pin plastic flat package. Its features are as follows.

(1) Original high-speed 16-bit CPU (900H_CPU)
- Instruction mnemonics upwardly compatible with TLCS-90/900
- 16M-byte linear address space
- General-purpose registers using register bank system
- 16-bit multiplication / division instructions, bit transfer / arithmetic instructions
- Micro DMA: four channels (640 ns / 2 bytes at 25 MHz)

(2) Minimum instruction execution time: 160 ns (at 25 MHz)

(3) Internal RAM : No
Internal ROM : No

(4) External memory expansion
- Expandable to 16 Mbytes (common to programs and data)
- External data bus width selection pin (AM8 / $\overline{16}$)
- Can use both 8- and 16-bit external buses
...dynamic data bus sizing

(5) Internal DRAM controller: two channels
- 2$\overline{CAS}$ / 2$\overline{WE}$ selectable

(6) 8-bit timer : eight channels

(7) 16-bit timer : two channels

(8) Pattern generator : four bits, two channels

(9) General-purpose serial interface : two channels
- Baud rate generated by external clock

(10) 10-bit AD converter : eight channels

(11) 8-bit DA converter : two channels

(12) Watchdog timer

(13) Chip selector, wait controller : four blocks

(14) Interrupt function
- CPU interrupts : 2 (software interrupt instructions, illegal instructions)
- Internal interrupts: 22 (seven priority levels available)
- External interrupts: 11 (seven priority levels available)

(15) Input / output ports
91 pins

(16) Standby function
Three HALT modes (RUN, IDLE, STOP)

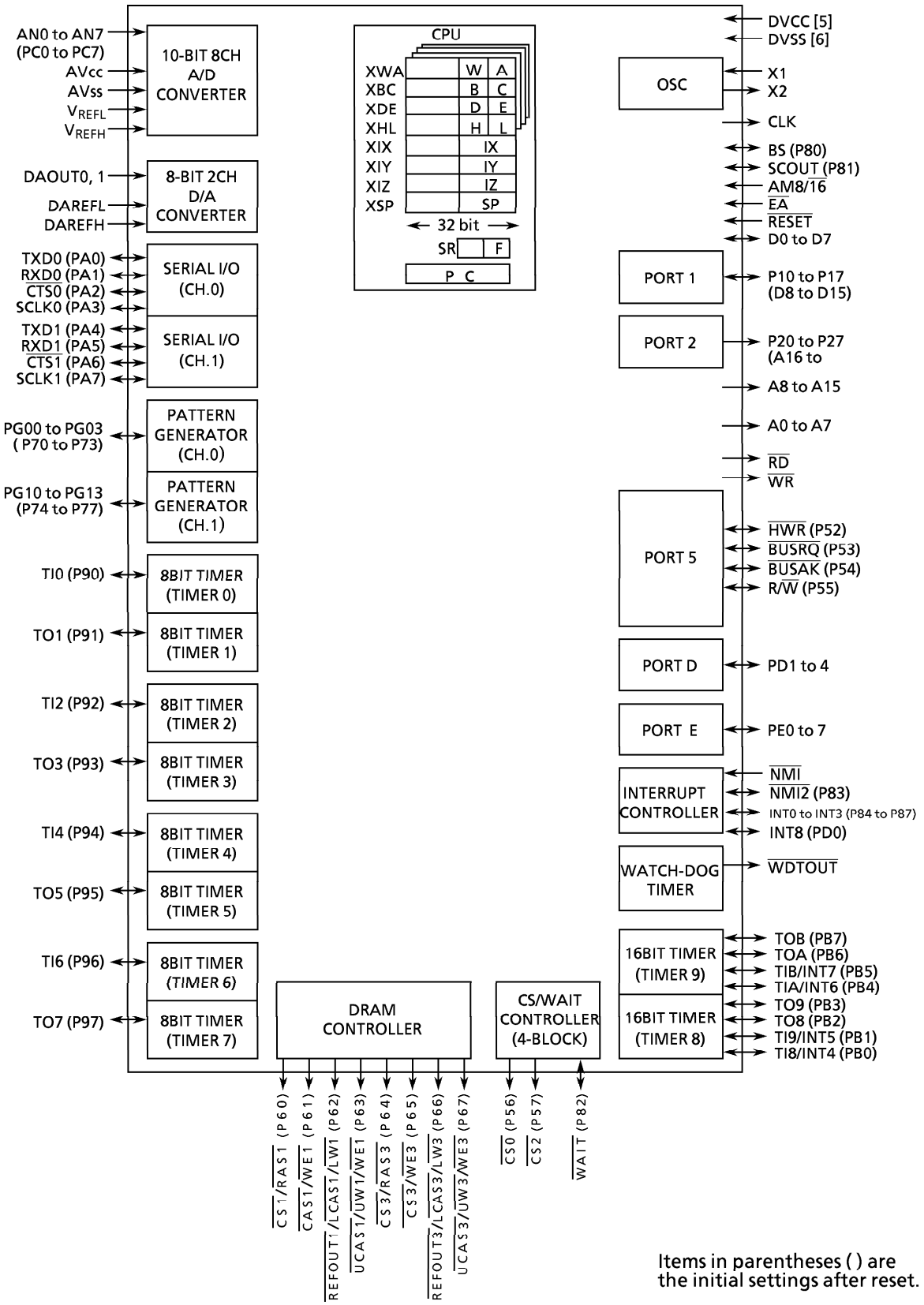


Figure 1 TMP95CO63 Block Diagram

2. Pin Assignment and Functions

2.1 Pin Assignment (Top view)

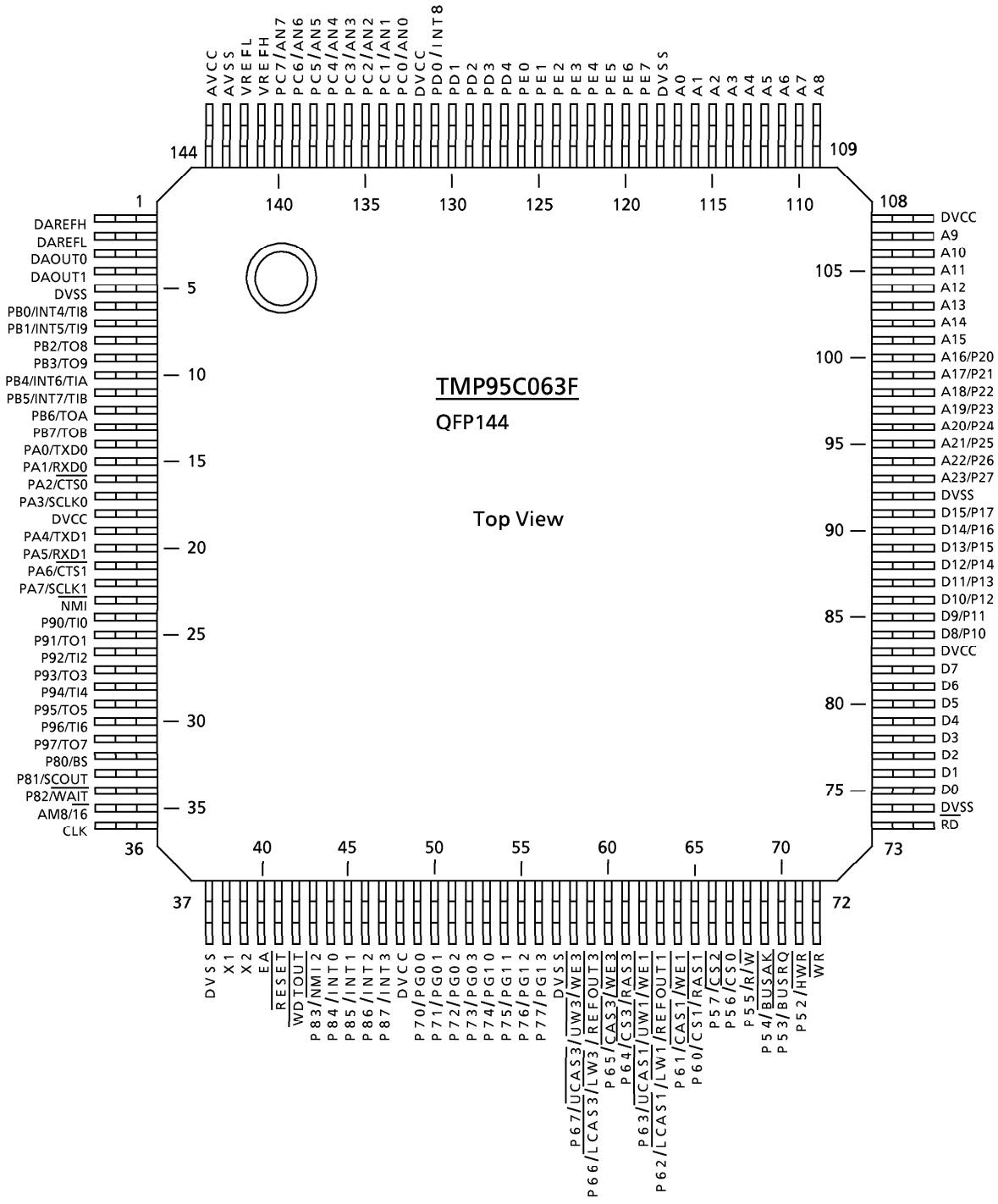


Figure 2.1 Pin Assignment

2.2 Pin Names and Functions

Table 2.2 shows the I/O pin names and their functions.

Table 2.2

Pin Name	Pin Number	Input / Output	Function
D0 to D7	8	Input / Output	Data : Data bus 0 to 7
P10 to P17 D8 to D15	8	Input / Output Input / Output	Port 1 : I/O ports. Individual pins can be set as inputs or outputs. Data : Data bus 8 to 15
P20 to P27 A16 to A23	8	Output Output	Port 2 : Output-only ports Address : Address bus 16 to 23
A8 to A15	8	Output	Address : Address bus 8 to 15
A0 to A7	8	Output	Address : Address bus 0 to 7
$\overline{RD}$	1	Output	Read : Strobe signal to read external memory (Setting bit 0 of the P5 register (RDE) to "0" outputs $\overline{RD}$ even when reading internal areas.)
$\overline{WR}$	1	Output	Write : Strobe signal to write data of pins D0 to 7.
P52 $\overline{HWR}$	1	Input / Output Output	Port 52 : I/O port (with pull-up) Upper write: Strobe signal for writing data of pins D8 to 15.
P53 $\overline{BUSRQ}$	1	Input / Output Input	Port 53 : I/O port (with pull-up) Input Bus request: Signal to request following pins set to high impedance: D0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{REFOUT}$ (*). (for external DMAC)
P54 $\overline{BUSAK}$	1	Input / Output Output	Port 54 : I/O port (with pull-up) Input Bus acknowledge: Signal to indicate following pins set to high impedance in response to $\overline{BUSRQ}$ signal: D0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{REFOUT}$ (*). (for external DMAC)
P55 R/$\overline{W}$	1	Input / Output Output	Port 55 : I/O port (with pull-up) Read/write: "1" indicates read or dummy cycle; "0" indicates write cycle.
P56 $\overline{CS0}$	1	Output Output	Port 56 : Output-only port Chip select 0: Outputs 0 if address is within specified address range.
P57 $\overline{CS2}$	1	Output Output	Port 57 : Output-only port Chip select 2: Outputs 0 if address is within specified address range.

Note : The external DMA controller, which uses the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins, cannot access the internal memory or internal I/O of TMP95C063.

(*) The DRAM control pins are high impedance only when bus release mode is set by the DRAM controller. For details, see 3.7, Dynamic RAM (DRAM) Controller.

Pin name	Pin Number	Input / Output	Function
P60 $\overline{CS1}$ $\overline{RAS1}$	1	Output Output Output	Port 60: Output-only port Chip select 1: Outputs 0 if address is within specified address range. Low address strobe 1: Outputs $\overline{RAS}$ strobe for DRAM if address is within specified address range.
P61 $\overline{CAS1}$ $\overline{WE1}$	1	Output Output Output	Port 61: Output-only port Column address strobe 1: Outputs 0 if address is within specified address range. (8-bit bus or 2WE mode) Write enable 1: Outputs write enable signal for DRAM. (2CAS mode)
P62 $\overline{LCAS1}$ $\overline{LW1}$ $\overline{REFOUT1}$	1	Output Output Output Output	Port 62: Output-only port Lower column address strobe 1: Outputs lower CAS strobe for DRAM if address is within specified address range. (2CAS mode) Lower write enable 1: Outputs lower write enable signal for DRAM. (2WE mode) Refresh out 1: 0 indicates generation of refresh cycle. (8-bit bus mode)
P63 $\overline{UCAS1}$ $\overline{UW1}$ $\overline{WE1}$	1	Output Output Output Output	Port 63: Output-only port Upper column address strobe 1: Outputs upper CAS strobe for DRAM if address is within specified address range. (2CAS mode) Upper write enable 1: Outputs upper write enable signal for DRAM. (2WE mode) Write enable 1: Outputs write enable signal for DRAM. (8-bit bus mode)
P64 $\overline{CS3}$ $\overline{RAS3}$	1	Output Output Output	Port 64: Output-only port Chip select 3: Outputs 0 if address is within specified address range. Low address strobe 3: Outputs $\overline{RAS}$ strobe for DRAM if address is within specified address range.
P65 $\overline{CAS3}$ $\overline{WE3}$	1	Output Output Output	Port 65: Output-only port Column address strobe 3: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address range. (8-bit bus or 2WE mode) Write enable 3: Outputs write enable signal for DRAM. (2CAS mode)
P66 $\overline{LCAS3}$ $\overline{LW3}$ $\overline{REFOUT3}$	1	Output Output Output Output	Port 66: Output-only port Lower column address strobe 3: Outputs lower CAS strobe for DRAM if address is within specified address range. (2CAS mode) Lower write enable 3: Outputs lower write enable signal for DRAM. (2WE mode) Refresh out 3: 0 indicates generation of refresh cycle. (8-bit bus mode)

Pin name	Pin Number	Input / Output	Function
P67 $\overline{UCAS3}$ $\overline{UW3}$ $\overline{WE3}$	1	Output Output Output Output	Port 67: Output-only port Upper column address strobe 3: Outputs upper CAS strobe for DRAM if address is within specified address range. (2CAS mode) Upper write enable 3: Outputs upper write enable signal for DRAM. (2WE mode) Write enable 3: Outputs write enable signal for DRAM. (8-bit bus mode)
P70 to P73 PG00 to PG03	4	Input / Output Output	Ports 70 to 73: I/O ports. Individual pins can be set as inputs or outputs. (with pull-up) Pattern generator ports 00-03
P74 to P77 PG10 to PG13	4	Input / Output Output	Ports 74 to 77: I/O ports. Individual pins can be set as inputs or outputs. (with pull-up) Pattern generator ports 10-13
P80 BS	1	Input / Output Output	Port 80: I/O port (with pull-up) Bus start: Indicates start of bus cycle.
P81 SCOUT	1	Input / Output Output	Port 81: I/O port (with pull-up) System clock output: Outputs system clock (external clock divided by 2).
P82 $\overline{WAIT}$	1	Input / Output Input	Port 82: I/O port (with pull-up) Wait: CPU bus wait request pin. (1 + N or 0 + NWAIT mode)
P83 $\overline{NMI2}$	1	Input / Output Input	Port 83: I/O port (with pull-up) Non-maskable interrupt request pin 2: Falling-edge interrupt request pin
P84 INT0	1	Input / Output Input	Port 84: I/O port (with pull-up) Interrupt request pin 0: Can be programmed for level or rising-edge detection.
P85 INT1	1	Input / Output Input	Port 85: I/O port (with pull-up) Interrupt request pin 1: Rising-edge interrupt request pin
P86 INT2	1	Input / Output Input	Port 86: I/O port (with pull-up) Interrupt request pin 2: Rising-edge interrupt request pin
P87 INT3	1	Input / Output Input	Port 87: I/O port (with pull-up) Interrupt request pin 3: Rising-edge interrupt request pin
P90 TI0	1	Input / Output Input	Port 90: I/O port (with pull-up) Timer input 0: Timer 0 input
P91 TO1	1	Input / Output Output	Port 91: I/O port (with pull-up) Timer output 1: Timer 0 or 1 output
P92 TI2	1	Input / Output Input	Port 92: I/O port (with pull-up) Timer input 2: Timer 2 input
P93 TO3	1	Input / Output Output	Port 93: I/O port (with pull-up) Timer output 3: Timer 2 or 3 output
P94 TI4	1	Input / Output Input	Port 94: I/O port (with pull-up) Timer input 4: Timer 4 input

Pin name	Pin Number	Input / Output	Function
P95 TO5	1	Input / Output Output	Port 95: I/O port (with pull-up) Timer output 5: Timer 4 or 5 output
P96 TI6	1	Input / Output Input	Port 96: I/O port (with pull-up) Timer input 6: Timer 6 input
P97 TO7	1	Input / Output Output	Port 97: I/O port (with pull-up) Timer output 7: Timer 6 or 7 output
PA0 TXD0	1	Input / Output Output	Port A0: I/O port (with pull-up) Serial transmit data output 0
PA1 RXD0	1	Input / Output Input	Port A1: I/O port (with pull-up) Serial receive data input 0
PA2 $\overline{\text{CTS0}}$	1	Input / Output Input	Port A2: I/O port (with pull-up) Serial data clear to send 0
PA3 SCLK0	1	Input / Output Input / Output	Port A3: I/O port (with pull-up) Serial clock input/output 0
PA4 TXD1	1	Input / Output Output	Port A4: I/O port (with pull-up) Serial data output 1
PA5 RXD1	1	Input / Output Input	Port A5: I/O port (with pull-up) Serial data input 1
PA6 $\overline{\text{CTS1}}$	1	Input / Output Input	Port A6: I/O port (with pull-up) Serial data clear to send 1
PA7 SCLK1	1	Input / Output Input / Output	Port A7: I/O port (with pull-up) Serial clock input / output 1
PB0 TI8 INT4	1	Input / Output Input Input	Port B0: I/O port (with pull-up) Timer input 8: Used as count or capture trigger input for timer 8. Interrupt request pin 4: Can be programmed for rising- or falling-edge detection.
PB1 TI9 INT5	1	Input / Output Input Input	Port B1: I/O port (with pull-up) Timer input 9: Used as count or capture trigger input for timer 8. Interrupt request pin 5: Rising-edge interrupt request pin
PB2 TO8	1	Input / Output Output	Port B2: I/O port (with pull-up) Timer output 8: Timer 8 output pin
PB3 TO9	1	Input / Output Output	Port B3: I/O port (with pull-up) Timer output 9: Timer 8 output pin
PB4 TIA INT6	1	Input / Output Input Input	Port B4: I/O port (with pull-up) Timer input A: Used as count or capture trigger input for timer 9. Interrupt request pin 6: Can be programmed for rising or falling edge detection.
PB5 TIB INT7	1	Input / Output Input Input	Port B5: I/O port (with pull-up) Timer input B: Used as count or capture trigger input for timer 9. Interrupt request pin 7: Rising-edge interrupt request pin

Pin Name	Pin Number	Input / Output	Function
PB6 TOA	1	Input / Output Output	Port B6: I/O port (with pull-up) Timer output A: Timer 9 output pin
PB7 TOB	1	Input / Output Output	Port B7: I/O port (with pull-up) Timer output B: Timer 9 output pin
PC0 to PC7 AN0 to AN7	8	Input Input	Input Port C: Input ports Analog inputs: A/D converter inputs
PD0	1	Input / Output Input	Port D0: I/O port (with pull-up) Interrupt request pin 8: Rising-edge interrupt request pin
PD1 to 4	4	Input / Output	Port D1 to D4: I/O ports (with pull-up)
PE0 to 7	8	Input / Output	Port E0 to E7: I/O ports (with pull-up)
DAREFH	1	Input	Reference voltage input pin for D/A converter (H)
DAREFL	1	Input	Reference voltage input pin for D/A converter (L)
DAOUT0	1	Output	D/A output 0: D/A converter 0 analog current output pin
DAOUT1	1	Output	D/A output 1: D/A converter 1 analog current output pin
$\overline{\text{WDTOUT}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Falling-edge interrupt request pin. Can also be programmed as rising-edge interrupt request pin.
CLK	1	Output	Clock output: Outputs external input clock X1 divided by 4. Pulled up during reset.
$\overline{\text{EA}}$	1	Input	Fixed to ground.
AM8/$\overline{16}$	1	Input	Address mode: External data bus width selection pin. Set to 0 when using fixed 16-bit external bus or dual 8/16-bit external bus. Set to 1 with 8-bit external bus fixed.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (with pull-up)
VREFH	1	Input	Reference voltage input pin for A/D converter (H)
VREFL	1	Input	Reference voltage input pin for A/D converter (L)
AVCC	1		A/D converter power supply pin
AVSS	1		A/D converter ground pin (0 V)
X1/X2	2	Input / Output	Oscillator connecting pins
DVCC	5		Power supply pin (+ 5 V)
DVSS	6		Ground pin (0 V)

Note 1 : Apart from the RESET pin, the pull-up resistors can be disconnected by software.
Note 2 : Connect all DVCC and AVCC pins to power supply and all DVSS and AVSS pins to GND.

3. Operation

The following is a block-by-block description of the functions and basic operation of TMP95C063.

Note that the description concludes with cautions and restrictions for each block in 7, Usage Cautions and Restrictions.

3.1 CPU

TMP95C063 contains an advanced, high-speed 16-bit CPU (the 900H_CPU). The CPU is described in the TLCS-900 CPU section in the previous chapter.

The following describes the CPU functions unique to TMP95C063 that are not described in "TLCS-900 CPU".

3.1.1 Reset Operation

At TMP95C063 reset, the power supply voltage must be within the operating range and internal oscillation must be stable. Set the $\overline{\text{RESET}}$ input to 0 for at least ten system clocks (= 10 states: 0.8 μs for a 25-MHz clock).

When the reset is accepted, the CPU:

- Sets the program counter (PC) to the reset vector stored at addresses FFFF00H to FFFF02H.
  PC (7 : 0) ← value at address FFFF00H
  PC (15 : 8) ← value at address FFFF01H
  PC (23 : 16) ← value at address FFFF02H
- Sets the stack pointer (XSP) to 100H
- Sets bits IFF2 to 0 of the status register (SR) to 111 (this sets the interrupt level mask register to level 7).
- Sets the MAX bit of the status register (SR) to 1 (this sets maximum mode). (Note: This product does not support minimum mode. Do not use the MIN instruction.)
- Clears bits RFP2 to 0 of the status register (SR) to 000 (this sets the register banks to 0).

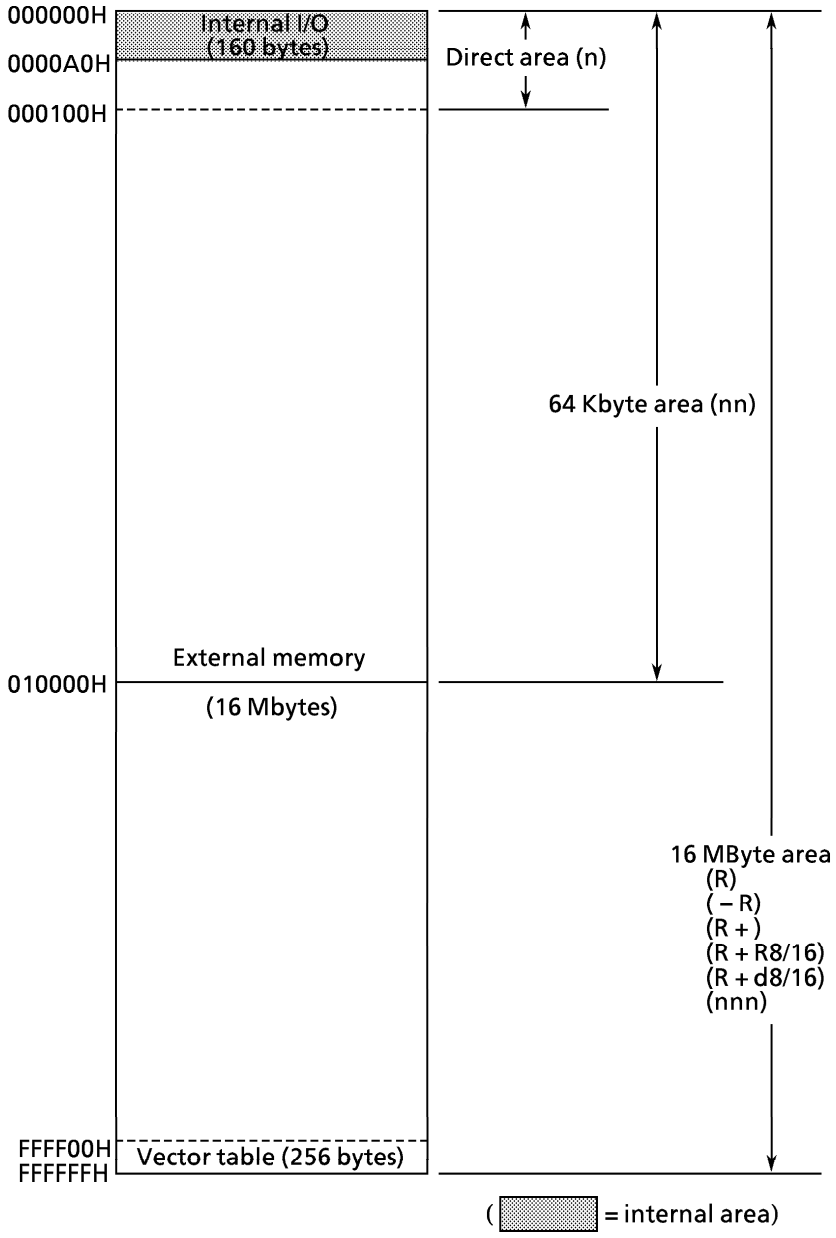
After reset is released, the CPU begins execution from the instruction at the location specified in the PC. Other than the changes described above, reset does not alter any internal CPU registers.

When reset is accepted, processing of the internal I/O, port, and other pins are as follows:

- Initializes the internal I/O registers as per specifications.
- Sets port pins (including pins also used as internal I/O) to general-purpose input or output mode.
- Sets the $\overline{\text{WDTOUT}}$ pin to 0 (watchdog timer is enabled after reset).
- Pulls up the clock pin to 1.

3.2 Memory Map

Figure 3.2 shows the TMP95C063 memory map.



Note : After reset, the stack pointer (XSP) is set to 100H.

Figure 3.2 Memory Map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V cc	– 0.5 to 6.5	V
Input voltage	V IN	– 0.5 to Vcc + 0.5	V
Output current (total)	Σ IOL	120	mA
Output current (total)	Σ IOH	– 120	mA
Power dissipation (Ta = 70°C)	P D	600	mW
Soldering temperature (10 s)	T SOLDER	260	°C
Storage temperature	T STG	– 65 to 150	°C
Operating temperature	T OPR	– 20 to 70	°C

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Electrical Characteristics

Vcc = 5 V ± 10%, TA = – 20 to 70°C (8 to 25 MHz)

(Typ values are for Ta = 25°C and Vcc = 5 V)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) P5, P7, P8, P9, PA, PB, PC, PD, PE RESET, NMI, INT0 to 3, INT8, NMI2 EA, AM8/16 X1	V IL V IL1 V IL2 V IL3 V IL4		– 0.3 – 0.3 – 0.3 – 0.3 – 0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2Vcc	V V V V V
Input High Voltage (D0 to 15) P5, P7, P8, P9, PA, PB, PC, PD, PE RESET, NMI, INT0 to 3, INT8, NMI2 EA, AM8/16 X1	V IH V IH1 V IH2 V IH3 V IH4		2.2 0.7 Vcc 0.75 Vcc Vcc – 0.3 0.8Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V OL	I OL = 1.6 mA		0.45	V
Output High Voltage	V OH V OH1 V OH2	I OH = – 400 μA I OH = – 100 μA I OH = – 20 μA	2.4 0.75 Vcc 0.9 Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I DAR	V EXT = 1.5 V R EXT = 1.1 kΩ	– 1.0	– 3.5	mA
Input Leakage Current Output Leakage Current	I LI I LO	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE STOP (Ta = – 20 to 70°C) STOP (Ta = 0 to 50°C)	I cc	fc = 25 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2	37 (Typ) 3.5 (Typ) 0.5 (Typ)	50 10 50 10	mA mA μA μA
Power Down Voltage (at STOP)	V STOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc	2.0	6.0	V
RESET Pull Up Resistance	R RST		50	150	kΩ
Pin Capacitance	C IO	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 to 3, INT8, NMI2	V TH		0.4	1.0 (Typ)	V
PullUp Resistance	R K		30	150	kΩ

Note: I DAR guarantees driving of up to eight output port pins between any two Vcc pins.

4.3 AC Electrical Characteristics

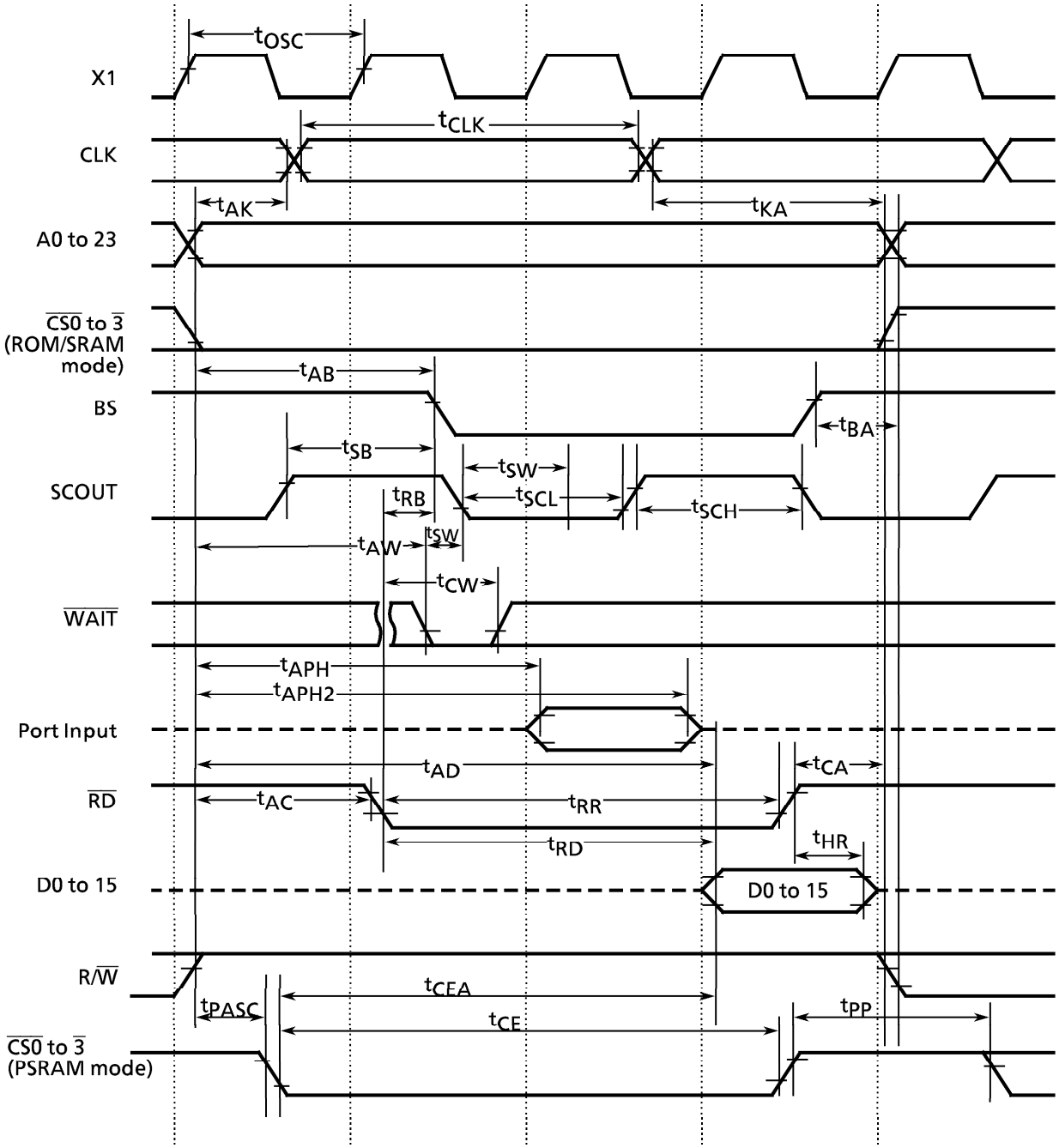
Vcc = 5 V ± 10%, TA = – 20 to 70°C
(8 MHz to 25 MHz)

No.	Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	40	125	50		40		ns
2	Clock pulse width	t_{CLK}	2x – 40		60		40		ns
3	A0 to A23 valid→ clock hold	t_{AK}	0.5x – 20		5		0		ns
4	Clock valid→ A0 to A23 hold	t_{KA}	1.5x – 60		5		0		ns
5	A0 to A23 valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{AC}	1.0x – 20		30		20		ns
6	$\overline{RD}$/$\overline{WR}$ rise→ A0 to A23 hold	t_{CA}	0.5x – 20		5		0		ns
7	A0 to A23 valid→ D0 to D15 input	t_{AD}		3.5x – 40		135		100	ns
8	$\overline{RD}$ fall→ D0 to D15 input	t_{RD}		2.5x – 45		80		55	ns
9	$\overline{RD}$ Low pulse width	t_{RR}	2.5x – 40		85		60		ns
10	$\overline{RD}$ rise→ D0 to D15 hold	t_{HR}	0		0		0		ns
11	$\overline{WR}$ Low pulse width	t_{WW}	2.5x – 40		85		60		ns
12	D0 to D15 valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 40		60		40		ns
13	$\overline{WR}$ rise →D0 to D15 hold	t_{WD}	0.5x – 10		15		10		ns
14	A0 to A23 valid→ $\overline{WAIT}$ input (1 + N WAIT)	t_{AW}		3.5x – 90		85		50	ns
	A0 to A23 valid→ $\overline{WAIT}$ input (0 + N WAIT)	t_{AW}		1.5x – 40		35		20	ns
15	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ hold (1 + N WAIT)	t_{CW}	2.5x + 0		125		100		ns
	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ hold (0 + N WAIT)	t_{CW}	0.5x + 0		25		20		ns
16	A0 to 23 valid→ PORT input	t_{APH}		2.5x – 90		35		10	ns
17	A0 to 23 valid→ PORT holt	t_{APH2}	2.5x + 50		175		150		ns
18	$\overline{WR}$ rise→ PORT valid	t_{CP}		200		200		200	ns
19	$\overline{CS}$ Low pulse width (PSRAM mode)	t_{CE}	3x – 40		110		80		ns
20	$\overline{CS}$fall→ D0 to 15 input (PSRAM mood)	t_{CEA}		3x – 60		90		60	ns
21	Address setup time (PSRAM mode)	t_{PASC}	0.5x – 15		10		5		ns
22	$\overline{CS}$ precharge time (PSRAM mode)	t_{PP}	1x – 10		40		30		ns
23	$\overline{RD}$/$\overline{WR}$ fall → BS fall	t_{RB}	0.5x		25		20		ns
24	A0 to A23 valid → BS fall	t_{AB}	1.5x – 20		55		40		ns
25	BS rise → A0 to A23 valid	t_{BA}		0.5x + 15		40		35	ns
26	SCOUT rise → BS fall	t_{SB}		1x + 30		80		70	ns
27	SCOUT fall → $\overline{WAIT}$ input (1 + N WAIT) / (0 + N WAIT)	t_{SW}	60		60		60		ns
28	SCOUT Low pulse width	t_{SCL}	1x – 20		30		20		ns
29	SCOUT High pulse width	t_{SCH}	1x – 20		30		20		ns

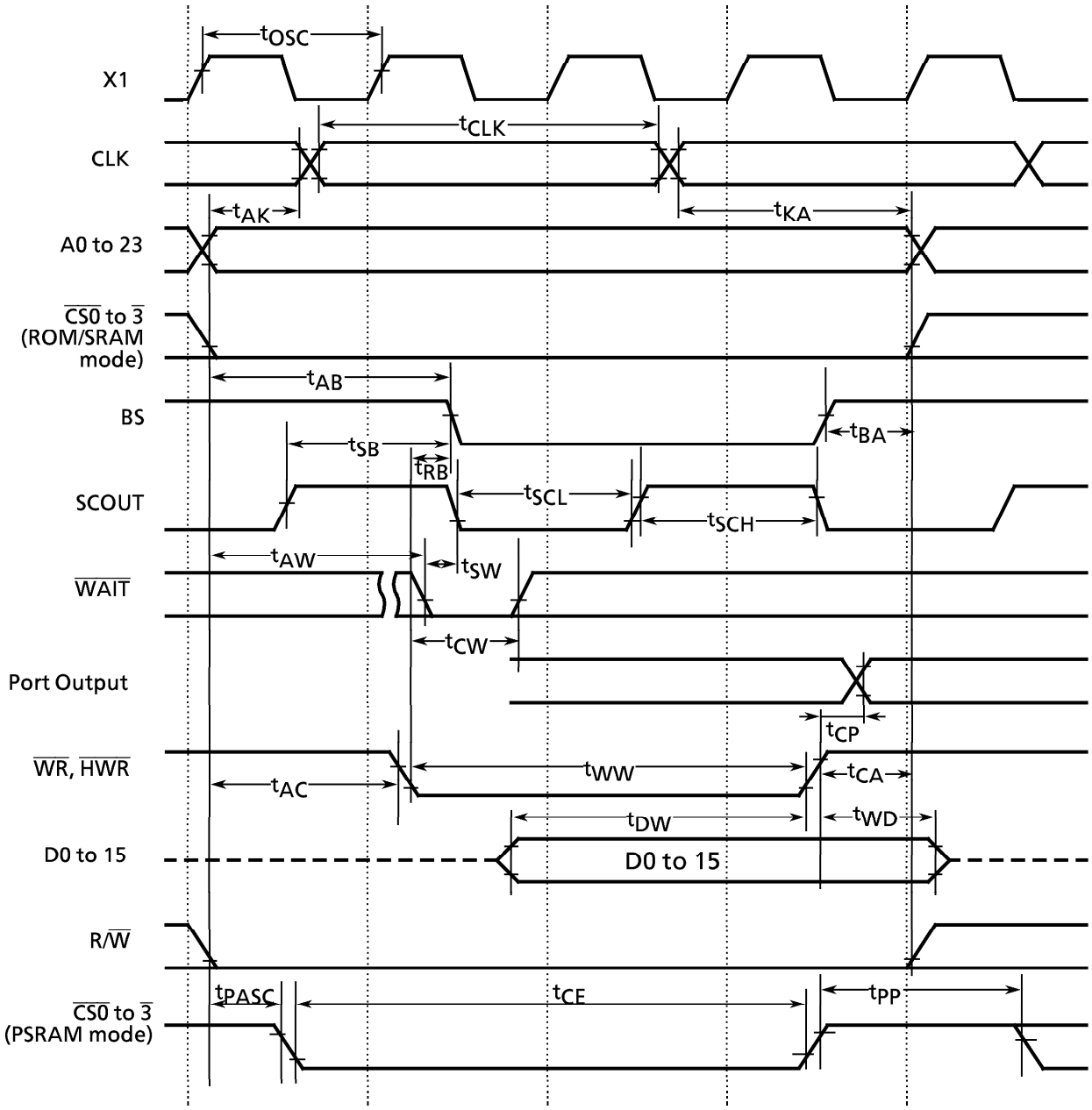
AC measuring conditions

- Output level : High 2.2 V /Low 0.8 V , CL = 50 pF
  (Note that for D0 to D15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, and CLK, CL = 100 pF, and for SCOUT, CL = 30pF)
- Input level : High 2.4 V /Low 0.45 V (D0 to D15)
  High 0.8 Vcc /Low 0.2 Vcc (except for D0 to D15)

(1) Read cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to 23
CS0 to 3 (ROM/SRAM mode)
tAB
BS
tBA
tSB
tSW
SCOUT
tRB
tSCL
tSCH
tSW
tAW
tCW
WAIT
tAPH
tAPH2
Port Input
tAD
tCA
RD
tAC
tRR
tRD
tHR
D0 to 15
D0 to 15
R/W
tCEA
tPASC
tCE
tPP
CS0 to 3 (PSRAM mode)

(2) Write cycle



4.4 DRAM Control AC Electrical Characteristics

Vcc = 5 V ± 10%, TA = – 20 to 70°C
(8 MHz to 25 MHz)

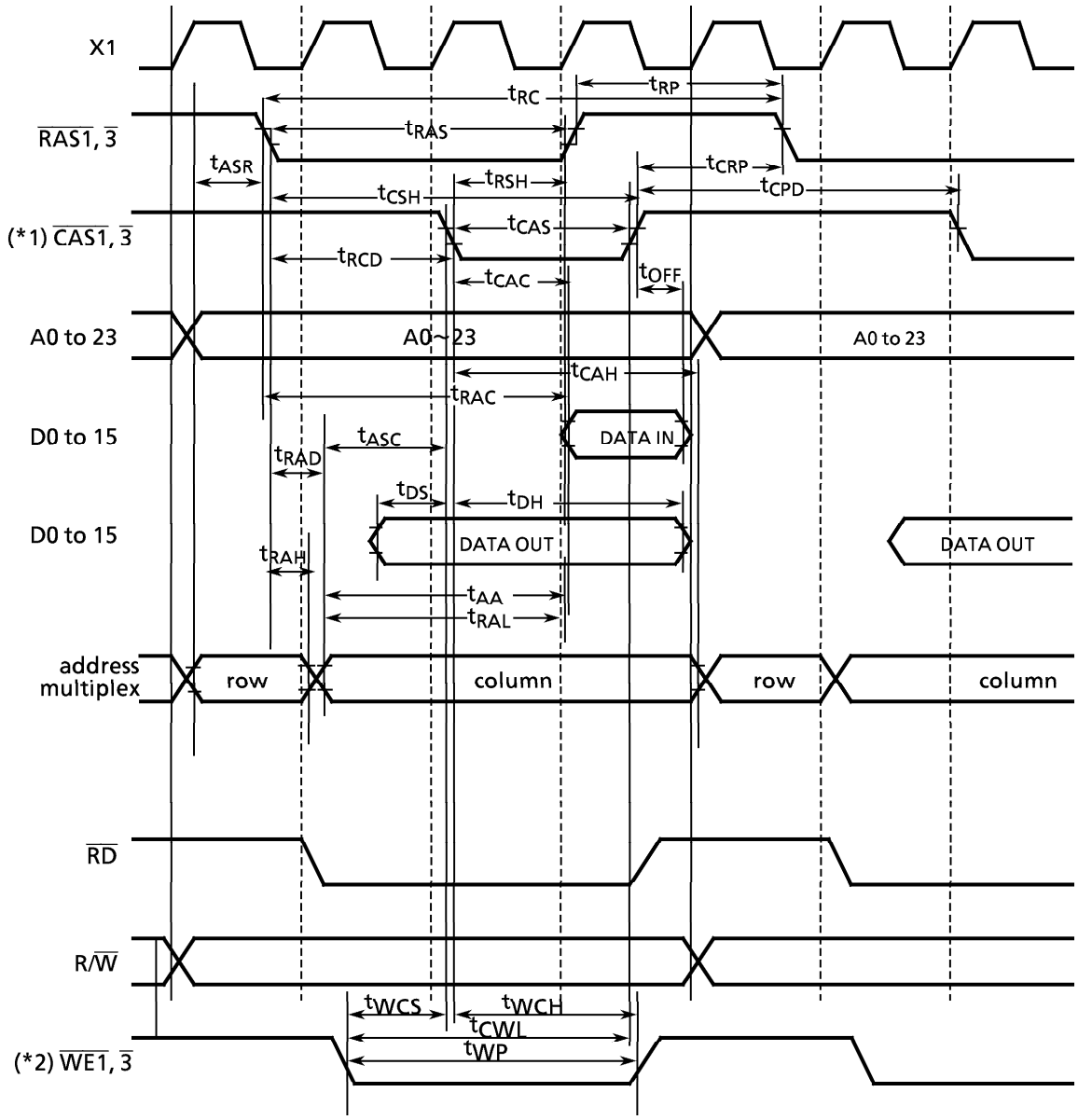
No.	Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	$\overline{RAS}$ cycle time	t_{RC}	4X		200		160		ns
2	$\overline{RAS}$ access time	t_{RAC}		3X-50		100		70	ns
3	$\overline{CAS}$ access time	t_{CAC}		1.5X-35		40		25	ns
4	Column address access time	t_{AA}		2.5X-55		70		45	ns
5	Input data hold time	t_{OFF}	0		0		0		ns
6	$\overline{RAS}$ precharge time	t_{RP}	1.5X-10		65		50		ns
7	$\overline{RAS}$ pulse width	t_{RAS}	2.5X-30		95		70		ns
8	$\overline{RAS}$ hold time	t_{RSH}	1X-15		35		25		ns
9	$\overline{CAS}$ hold time	t_{CSH}	3X-35		115		85		ns
10	$\overline{CAS}$ pulse width	t_{CAS}	1.5X-15		65		45		ns
11	$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	1.5X-40	1.5X	35	75	20	60	ns
12	$\overline{RAS}$ column address delay time	t_{RAD}	0.5X-5	0.5X + 20	20	45	15	40	ns
13	$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	1X-35		15		5		ns
14	$\overline{CAS}$ precharge time	t_{CPD}	2.5X-35		90		65		ns
15	Row address setup time	t_{ASR}	0.5X-15		10		5		ns
16	Row address hold time	t_{RAH}	0.5X-5		20		15		ns
17	Column address setup time	t_{ASC}	1X-25		25		15		ns
18	Column address hold time	t_{CAH}	2X-50		50		30		ns
19	Column address $\overline{RAS}$ read time	t_{RAL}	2X-45		55		35		ns
20	Write command $\overline{CAS}$ read time	t_{CWL}	2.0X-35		65		45		ns
21	Data output setup time	t_{DS}	0.5X-15		10		5		ns
22	Data output hold time	t_{DH}	2X-35		65		45		ns
23	Write command setup time	t_{WCS}	0.5X-20		5		0		ns
24	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CHR}*1	2X-50		50		30		ns
25	$\overline{RAS}$ precharge $\overline{CAS}$ active time	t_{RPC}*	1.5X-30		45		30		ns
26	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CSR}*	0.5X-10		15		10		ns
27	$\overline{RAS}$ precharge time (self-refresh)	t_{RPS}*2	4X-20		180		140		ns
28	$\overline{CAS}$ hold time (self-refresh)	t_{CHS}*2	0		0		0		ns
29	Refresh setup time	t_{CFL}*	1X-5		45		35		ns
30	Refresh hold time	t_{CFH}*	1X-10		40		30		ns
31	Write command pulse width	t_{WP}	2.0x-40		60		40		ns
32	Write command hold time	t_{WCH}	1.5x-40		35		20		ns

*1 $\overline{CAS}$-before-$\overline{RAS}$ interval refresh mode
*2 $\overline{CAS}$-before-$\overline{RAS}$ self-refresh mode
* $\overline{CAS}$-before-$\overline{RAS}$ interval refresh and self-refresh modes

AC measuring conditions

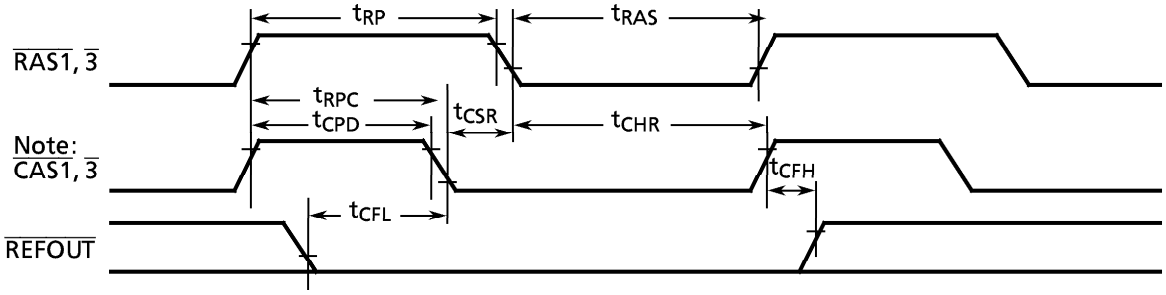
- Output level : High 2.2 V /Low 0.8 V , CL = 50 pF
  (Note that for D0 to D15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, and R/$\overline{W}$, CL = 100 pF)
- Input level : High 2.4 V /Low 0.45 V (D0 to D15)
  High 0.8 Vcc /Low 0.2 Vcc (except for D0 to D15)

(1) Read/Write Access Cycle

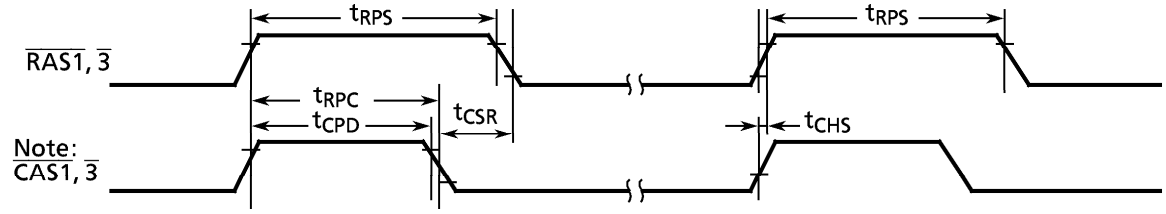


Note 1: Here, $\overline{CAS}$ includes $\overline{LCAS}$ and $\overline{UCAS}$.
Note 2: Here, $\overline{WE}$ includes $\overline{LW}$ and $\overline{UW}$.

(2) $\overline{CAS}$-before-$\overline{RAS}$ Interval Refresh Cycle



(3) $\overline{CAS}$-before-$\overline{RAS}$ Self-Refresh Cycle



Note : Here, $\overline{CAS}$ includes $\overline{LCAS}$ and $\overline{UCAS}$.

4.5 A/D Converter Characteristics

V_{CC} = 5 V ± 10%, TA = − 20 to 70°C (8 to 25 MHz)

Parameter		Symbol	Min	Typ.	Max	Unit
Analog reference voltage (+)		VREFH	V_{CC}-0.2 V	V_{CC}	V_{CC}	V
Analog reference voltage (−)		VREFL	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage		VAIN	VREFL		VREFH	
Analog reference voltage power supply current		I_{REF}				
V_{CC} = 5 V ± 10%	<VREFON> = 1	(VREFL = 0 V)		0.5	1.5	mA
V_{CC} = 5 V ± 10%	<VREFON> = 0			0.02	5.0	μA
V_{CC} = 5 V ± 10%	Total tolerance	Conversion tolerance		± 3.0	± 6	LSB

Note 1: 1LSB = (VREFH − VREFL) / 2^10 [V]

Note 2: Power supply current ICC from the digital power supply includes the power supply from the AVCC pin.

4.6 Serial Channel Timing

(1) SCLK input mode (I/O interface mode)

V_{CC} = 5 V ± 10%, TA = − 20 to 70°C (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		0.8		0.64		μs
Output Data → SCLK rise	t_{OSS}	t_{SCY}/2 − 5X − 50		100		70		ns
SCLK rise→ Output Data hold	t_{OHS}	5X − 100		150		100		ns
SCLK rise→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rise→ valid data input	t_{SRD}		t_{SCY} − 5X − 100		450		340	ns

(2) SCLK output mode (I/O interface mode) Vcc = 5 V ± 10%, TA = − 20 to 70℃ (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16X	8192X	0.8	409.6	0.64	327.6	μs
Output Data → SCLK rise	t_{OSS}	t_{SCY} − 2X − 150		550		410		ns
SCLK rise→ Output Data halt	t_{OHS}	2X − 80		20		0		ns
SCLK rise→ Input Data halt	t_{HSR}	0		0		0		ns
SCLK rise→ valid data input	t_{SRD}		t_{SCY} − 2X − 150		550		410	ns

(3) SCLK input mode (UART mode) Vcc = 5 V ± 10%, TA = − 20 to 70℃ (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4X + 20		220		180		ns
SCLK low-level pulse width	t_{SCYL}	2X + 5		105		85		ns
SCLK high-level pulse width	t_{SCYH}	2X + 5		105		85		ns

4.7 Event Counter (TI0, TI2, TI4, TI6, TI8, TI9, TIA, TIB)

Vcc = 5 V ± 10%, TA = − 20 to 70℃ (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock cycle	t_{VCK}	8X + 100		500		420		ns
Clock low-level pulse width	t_{VCKL}	4X + 40		240		200		ns
Clock high-level pulse width	t_{VCKH}	4X + 40		240		200		ns

4.8 Interrupt Operation

Vcc = 5 V ± 10%, TA = − 20 to 70℃ (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, $\overline{NMI2}$, INT0 to 3,8 low-level pulse width	t_{INTAL}	4X		200		160		ns
$\overline{NMI}$, $\overline{NMI2}$, INT0 to 3,8 high-level pulse width	t_{INTAH}	4X		200		160		ns
INT4 to INT7 low-level pulse width	t_{INTBL}	8X + 100		500		420		ns
INT4 to INT7 high-level pulse width	t_{INTBH}	8X + 100		500		420		ns

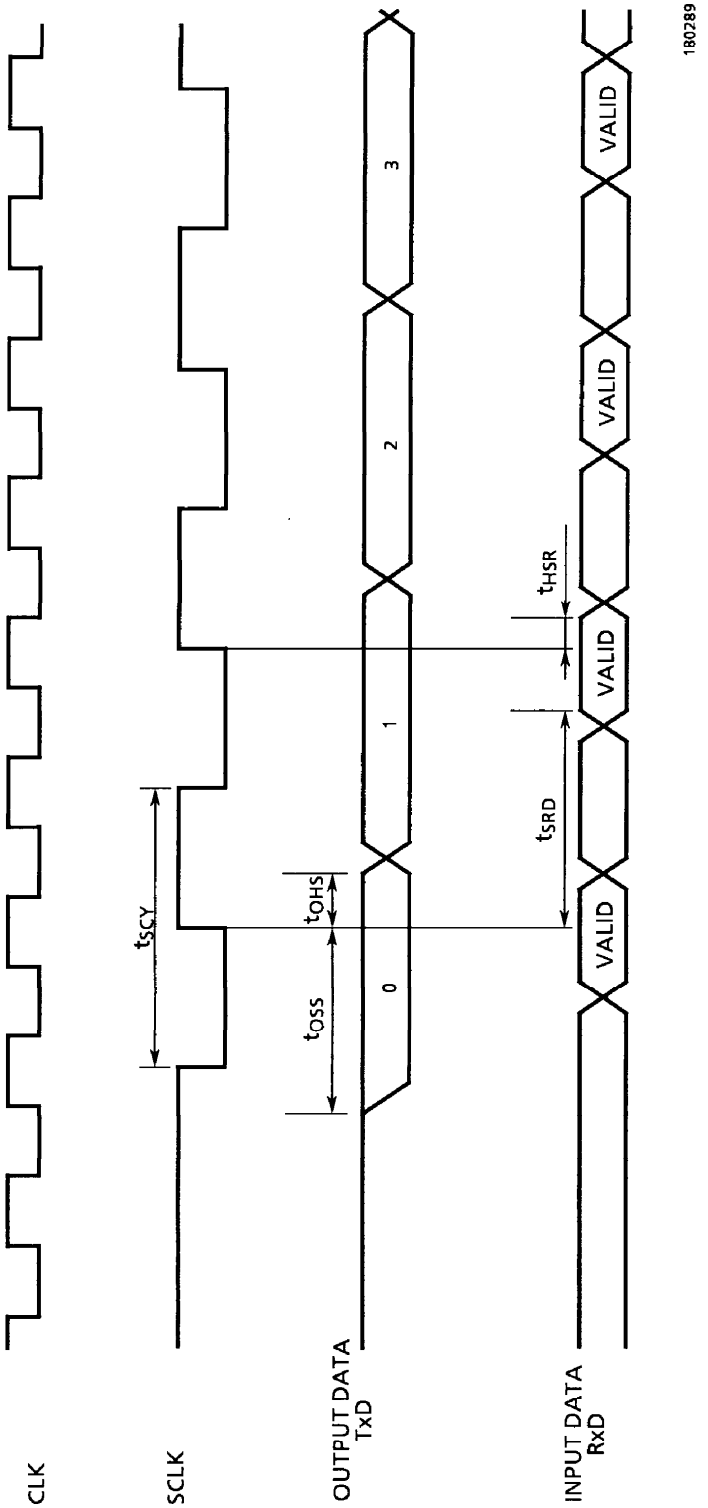
4.9 D/A Conversion Characteristics (Unless otherwise specified, Vcc = 5 V, Vss = DAREFL = 0 V)

Vcc = 5 V ± 10% TA = − 20 to 70℃
f = 8 to 25 MHz

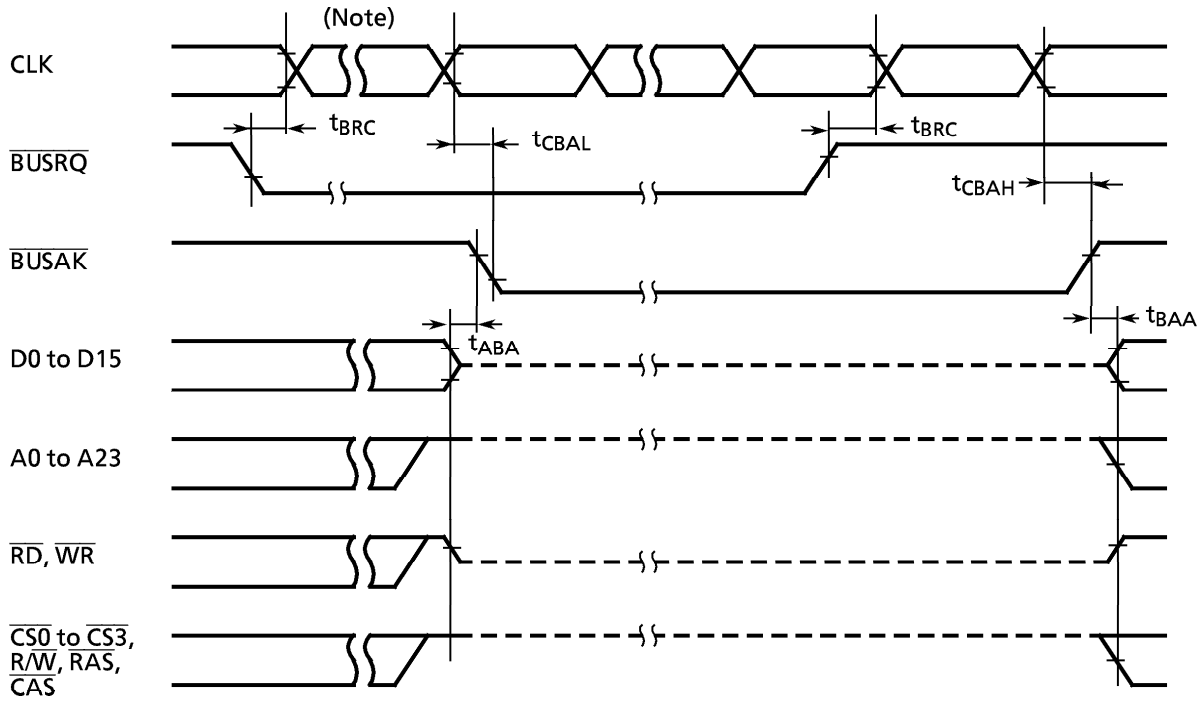
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Analog reference voltage	DAREFH		4.0		Vcc	V
Analog reference voltage	DAREFL		Vss		Vss	
Resolution	Conversion tolerance				8	BIT
Total tolerance		R = 1 MΩ (See note 1) R = 5 MΩ (See note 1) R = 10 MΩ (See note 1)			7.0 4.5 4.0	LSB LSB LSB
Differential linear error				2.0		LSB

Note : "R" is the load resistance on the D/A converter output pin.

4.10 I/O Interface Mode Timing Diagram



4.11 Bus Request/Bus Acknowledge Timing



Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ setup time for CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{BUSAK}$ fall	t_{CBAL}		2.0x + 120		220		200	ns
CLK→ $\overline{BUSAK}$ rise	t_{CBAH}		0.5x + 40		65		60	ns
Time from output buffer off until $\overline{BUSAK}$ fall	t_{ABA}	0	80	0	80	0	80	ns
Time from $\overline{BUSAK}$ rise until output buffer on	t_{BAA}	0	80	0	80	0	80	ns

Note: When bus release is requested with $\overline{BUSRQ}$ cleared to 0, that request cannot be granted until the previous bus cycle is terminated by a WAIT, and the WAIT is released.