CMOS 8-Bit Microcontroller

TMP88CS38N, TMP88CM38AN/F, TMP88CP38AN/F

The TMP88CS38/CM38A/CP38A is the high speed and high performance 8-bit single chip microcomputers. This MCU contain CPU core, ROM, RAM, input/output ports, four Multi-function timer/counters, serial bus interface, on-screen display, PWM output, 8-bit AD converter, and remote control signal preprocessor on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP88CS38N	64 K X 8-bit	2 K X 8-bit	P-SDIP42-600-1.78	TMP88PS38N/F
TMP88CM38AN/F	32 K X 8-bit	1.5 K X 8-bit	P-SDIP42-600-1.78	
TMP88CP38AN/F	48 K X 8-bit		P-QFP44-1414-0.80D	

Features

- 8-bit single chip microcomputer TLCS-870/X Series
- Instruction execution time: 0.25 μs (at 16 MHz)
- 842 basic instructions
  - Multiplication and Division (8 bits X 8 bits, 16 bits X 8 bits, 16 bits/8 bits)
  - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
  - 16-bit data and 20-bit data operations
  - 1-byte jump/subroutine-call(Short relative jump/Vector call)
- I/O ports: Maximum 33 (High current output: 4)
- 16 interrupt sources: External 5, Internal 11
  - All sources have independent latches each, and nested interrupt control is available.
  - Edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ROM corrective function
- Two 16-bit timer/counters: TC1, TC2
  - Timer, Event-counter, Pulse width measurement, External trigger timer, Window modes
- Two 8-bit timer/counters: TC3, TC4
  - Timer, Event counter, Capture (Pulse width/duty measurement) mode

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
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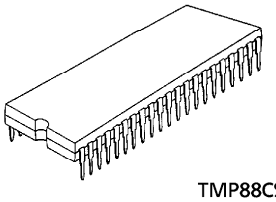
- ◆ Time base timer (Interrupt frequency: 0.95 Hz to 31250 Hz)
- ◆ Watchdog timer
  - Interrupt sourse/reset output
- ◆ Serial bus interface
  - I^2C bus, 8-bit SIO mode (Selectable two I/O channels)
- ◆ On-screen display circuit
  - Font ROM characters: 384 characters
  - Characters display: 32 columns X 12 lines
  - Composition: 16 X 18 dots
  - Size of character: 3 kinds (line by line)
  - Color of character: 8 or 15 kinds (character by character)
  - Variable display position: Horizontal 256 steps, Vertical 512 steps
  - Fringing, Smoothing, Slant, Underline , Blinking function
- ◆ Jitter elimination
- ◆ Data slicer circuit 1ch
- ◆ DA conversion (Pulse Width Modulation) outputs
  - 14/12-bit resolution (2 channels)
  - 12-bit resolution (2 channels)
  - 7-bit resolution (6 channels)
- ◆ 8-bit successive approximate type AD converter with sample and hold
- ◆ Remote control signal preprocessor
- ◆ Two power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
  - IDLE mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- ◆ Emulation POD: BM88CS38N0A

Package

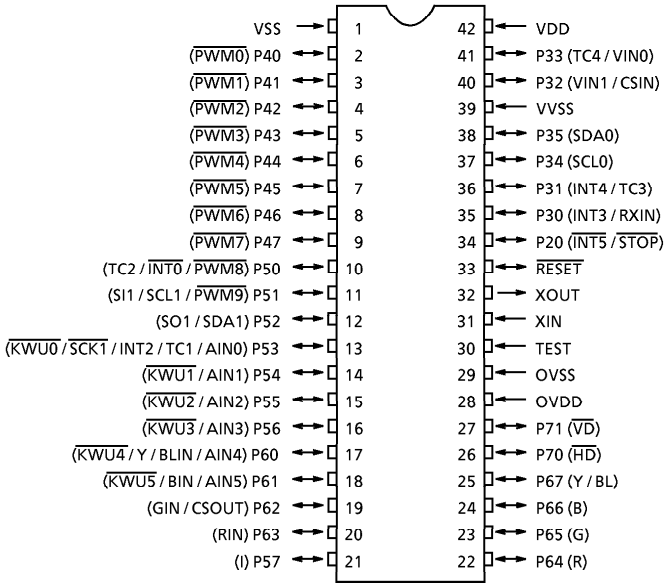
P-SDIP42-600-1.78



TMP88CS38N
TMP88CP38AN
TMP88CM38AN
TMP88PS38N

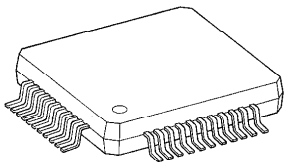
Pin Assignments

P-SDIP42-600-1.78



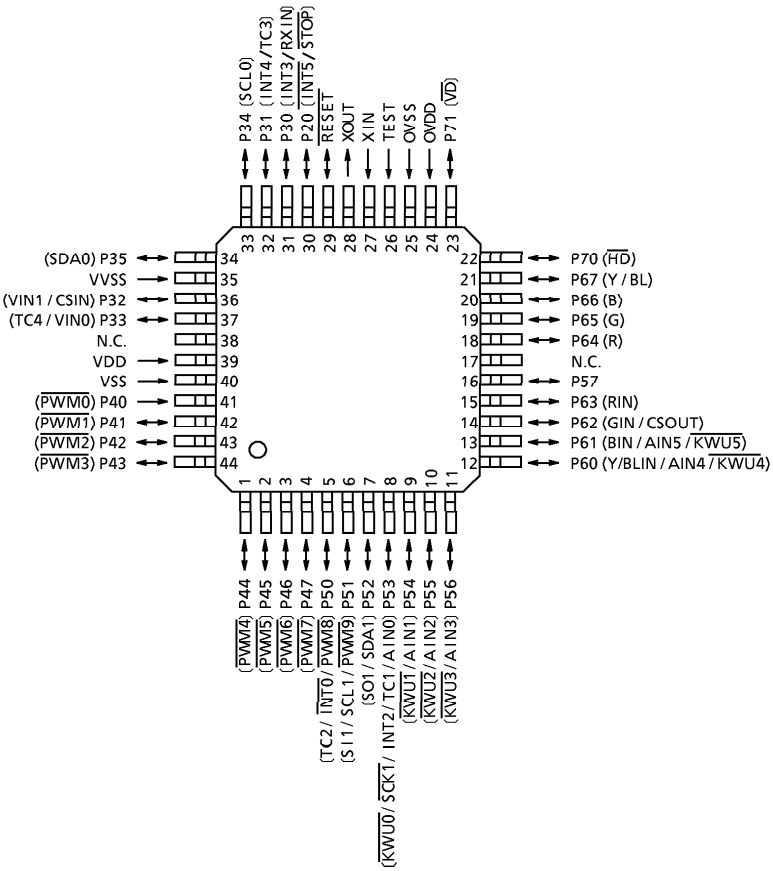
Package

P-QFP44-1414-0.80D



TMP88CS38F
TMP88CP38AF
TMP88CM38AF
TMP88PS38F

P-QFP44-1414-0.80D



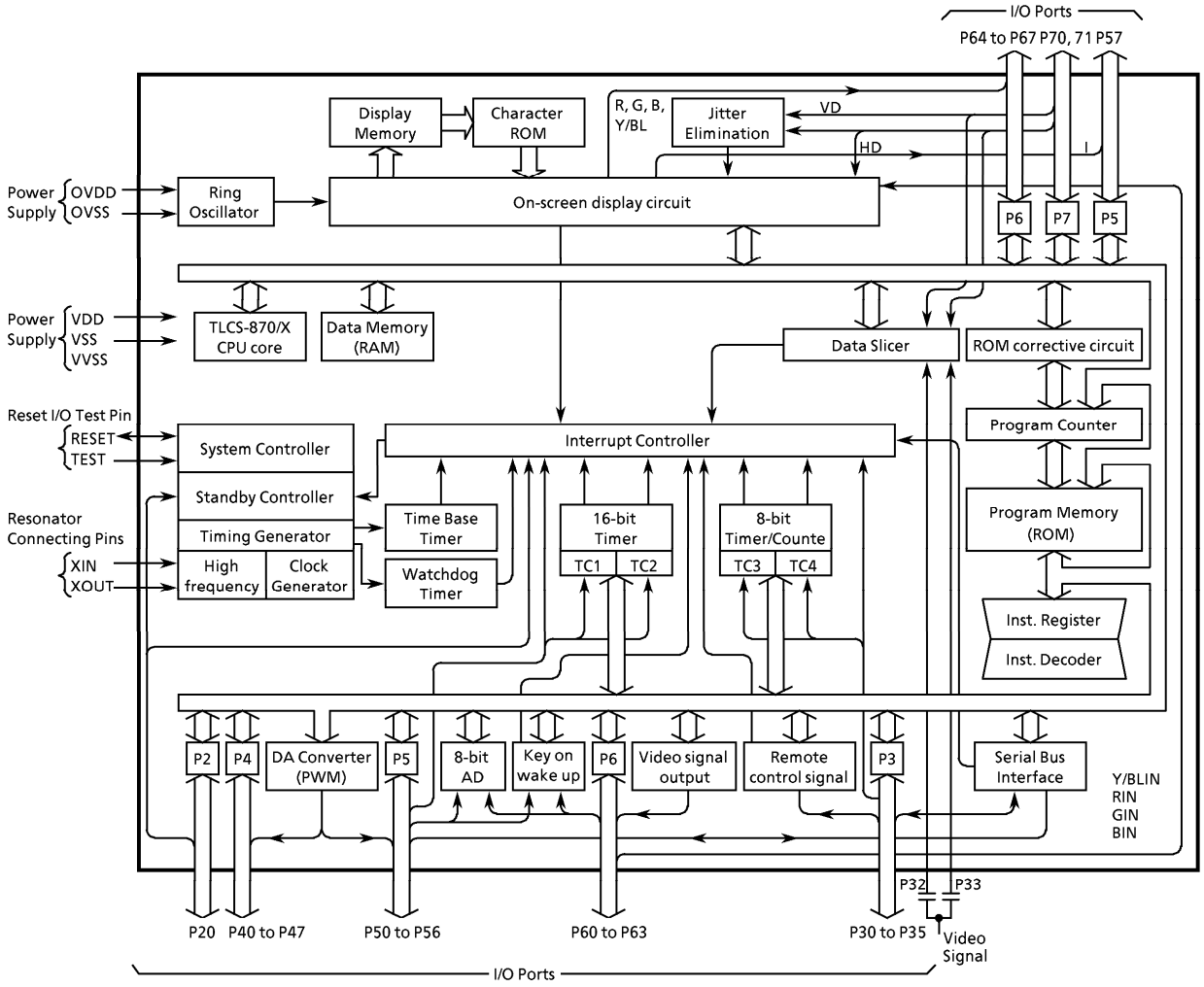
Pin Functions (1/2)

Pin Name	I/O	Function	
P20 ($\overline{INT5}$/$\overline{STOP}$)	I/O (Input)	1-bit input/output port with latch. When used as an input port, the latch must be set to "1".	External interrupt input 5 or STOP mode release signal input
P35 (SDA0)	I/O (Input/Output)	6-bit programmable input/output port. Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a serial bus interface input/output, the latch must be set to "1".	I^2C bus serial data input/output 0
P34 (SCL0)	I/O (Input/Output)		I^2C bus serial clock input/output 0
P33 (TC4/VIN0)	I/O (Input)		Timer Counter input 4 or Video signal Input 0
P32 (VIN1/CSIN)	I/O (Input)		Video signal input 1 or Composite sync input
P31 (INT4/TC3)	I/O (Input)		External interrupt input 4 or Timer/Counter input 3
P30 (INT3/RXIN)	I/O (Input)		External interrupt input 3 or Remote control signal preprocessor input
P47 ($\overline{PWM7}$)	I/O (Output)	8-bit programmable input/output port. Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a PWM output, the latch must be set to "1".	7-bit DA conversion (PWM) outputs
P46 ($\overline{PWM6}$)	I/O (Output)		
P45 ($\overline{PWM5}$)	I/O (Output)		
P44 ($\overline{PWM4}$)	I/O (Output)		
P43 ($\overline{PWM3}$)	I/O (Output)		12-bit DA conversion (PWM) outputs
P42 ($\overline{PWM2}$)	I/O (Output)		
P41($\overline{PWM1}$)	I/O (Output)		14/12-bit DA conversion (PWM) outputs
P40 ($\overline{PWM0}$)	I/O (Output)		
P57 (I)	I/O (Output)	8-bit programmable input/output port. Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a PWM output, a serial bus interface input/output, the latch must be set to "1".	Translucent signal output
P56 ($\overline{KWU3}$/AIN3)	I/O (Input)		Key on wake-up inputs or AD converter analog inputs
P55 ($\overline{KWU2}$/AIN2)	I/O (Input)		
P54 ($\overline{KWU1}$/AIN1)	I/O (Input)		
P53 ($\overline{KWU0}$/AIN0/TC1 /INT2/$\overline{SCK1}$)	I/O (Input /Input/Input /Input/Output)		Key on wake-up input or AD converter analog input or Timer/counter input 1 or External interrupt input 2 or SIO serial clock input /output 1
P52 (SDA1/SO1)	I/O (Input/Output /Output)		I^2C bus serial data Input/Output 1 or SIO serial data output 1
P51 ($\overline{PWM9}$/SCL1/SI1)	I/O (Output/Input/ Output/Input)		7-bit DA conversion (PWM) output or I^2C bus serial data input/Output 1 or SIO serial data input 1
P50 ($\overline{PWM8}$/TC2/$\overline{INT0}$)	I/O (Output/Input /Input)		7-bit DA conversion (PWM) output or Timer/Counter input 2 or External interrupt input 0
P67 (Y/BL)	I/O (Output)	8-bit programmable input/output port. (P67 to 64 : Tri-State, P63 to 60 : High current output) Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used P64 to P67 as port , each bit of the P6 port data selection register (bit 7 to 4 in ORP6S) must be set to "1".	Y or BL output
P66 (B)	I/O (Output)		R/G/B outputs
P65 (G)	I/O (Output)		
P64 (R)	I/O (Output)		
P63 (RIN)	I/O (Input)		R input
P62 (GIN/CSOUT)	I/O (Input/Output)		G input or TEST Video Singal output
P61 ($\overline{KWU5}$/BIN/AIN5)	I/O (Input)		Key on wake-up input 5 or B input or AD converter analog input 5
P60 ($\overline{KWU4}$/YBLIN/AIN4)	I/O (Input)		Key on wake-up input 4 or Y/BL input or AD converter analog input 4

Pin Functions (2/2)

Pin Name	I/O	Function	
P71 ($\overline{VD}$)	I/O (Input)	2-bit programmable input/output port. Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs.	Vertical synchronous signal input
P70 ($\overline{HD}$)	I/O (Input)		Horizontal synchronous signal input
XIN,XOUT	Input, Output	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
RESET	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-rest output	
TEST	Input	Test pin for out-going test. Be tied to low.	
OVDD,OVSS	Power Supply	+ 5 V, 0 V (GND) for oscillator circuit	
VDD,VSS,VVSS	Power Supply	+ 5 V, 0 V (GND)	

Block Diagram



Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.
This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP88CS38/CM38A/CP38A memory consists of four blocks: ROM, RAM, SFR (Special Function Register), and DBR (Data Buffer Register). They are all mapped to a 1-Mbyte address space. Figure 1.1.1 shows the TMP88CS38/CM38A/CP38A memory address map. There are 16 banks of the general-purpose register. The register banks are also assigned to the RAM address space.

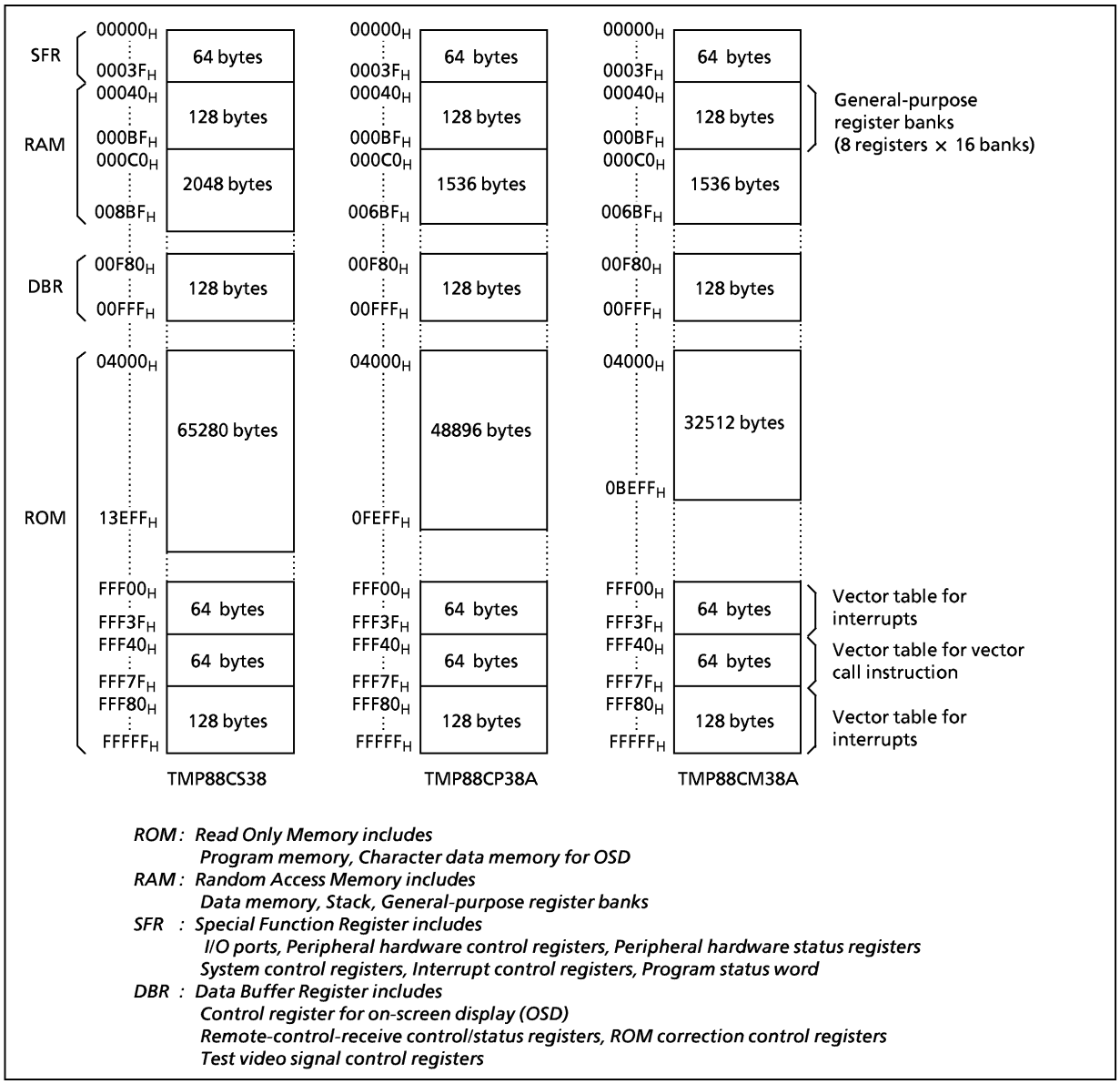


Figure 1.1.1 Memory Address Map

Electrical Characteristics

Absolute maximum ratings

(V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}	—	– 0.3 to 6.5	V
Input Voltage	V_{IN}	—	– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}	—	– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	3.2	mA
	I_{OUT2}	Ports P60 to P63	30	
Output Current (Total)	ΣI_{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	120	
	ΣI_{OUT2}	Ports P60 to P63	120	
Power Dissipation [Topr = 70°C]	PD	—	TMP88CS38: 600 TMP88CP38A/CM38A: 400	mW
Soldering Temperature (time)	Tsld	—	260 (10 s)	°C
Storage Temperature	Tstg	—	– 55 to 125	
Operating Temperature	Topr	—	– 30 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended operating conditions

(V_{SS} = 0 V, Topr = –30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 16 MHz	NORMAL mode	4.5	5.5	V
			fc = 16 MHz	IDLE mode			
				STOP mode			
Input High Voltage	V_{IH1}	Except hysteresis input	V_{DD} = 4.5 to 5.5 V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
Input Low Voltage	V_{IL1}	Except hysteresis input	V_{DD} = 4.5 to 5.5 V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL4}	Key-on Wake-up input	V_{DD} = 4.5 to 5.5 V			$V_{DD} \times 0.65$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		8.0	16.0	MHz
	f_{OSC}	Internal clock	V_{DD} = 4.5 to 5.5 V	fc = 8 MHz	8.0	12.0	
				fc = 16 MHz	16.0	24.0	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL mode and IDLE mode.

Note 3: Smaller value is alternatively specified as the maximum value.

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	
	I_{IN3}	Tri-state ports	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	
	I_{IN4}	$\overline{RESET}$, $\overline{STOP}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	
Input Resistance	R_{IN2}	$\overline{RESET}$	V_{DD} = 5.5 V, V_{IN} = 0 V	100	220	450	kΩ
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and ports P60 to P63	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Output Low current	I_{OL3}	Port P60 to P63	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL mode	I_{DD}	—	V_{DD} = 5.5 V fc = 16 MHz (Note3) V_{IN} = 5.3 V/0.2 V	–	25	30	
Supply Current in IDLE mode				–	20	25	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	μA

Note 1 : Typical values show those at Topr = 25°C , V_{DD} = 5 V.

Note 2 : Input Current I_{IN3} ; The current through resistor is not included.

Note 3 : Supply Current I_{DD} ; The current (Typ. 0.5 mA) through ladder resistors of ADC is included in NORMAL mode and IDLE mode.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	supplied from V_{DD} pin.	–	V_{DD}	–	V
	V_{ASS}	supplied from V_{SS} pin.	–	0	–	
Analog Reference Voltage Range	$\triangle V_{AREF}$	= V_{DD} – V_{SS}	–	V_{DD}	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{DD}	
Nonlinearity Error		V_{DD} = 5.0 V	–	–	± 1	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 3	

Note: The total error means all error except quanting error.

AC characteristics

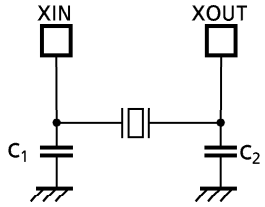
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL mode	0.5	–	1.0	μs
		In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 16 MHz	31.25	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					

Recommended oscillating conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator	Recommended Constant	
				C_1	C_2
High-frequency Osillation	Ceramic Resonator	8 MHz	Murata CSA8.00MTZ	30 pF	30 pF
		16 MHz	Murata CSA16.00MXZ040	5 pF	5 pF



High-frequency Oscillation

Note 1: To keep reliable operation, shield the device electrically with the metal plate on its package mold surface against the high electric field, for example, by CRT (Cathode Ray Tube) .

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

http://www.murata.co.jp/search/index.html