#### CMOS 8-Bit Microcontroller

#### TMP88CK49N, TMP88CM49N TMP88CK49F, TMP88CM49F

TMP88CK49N, TMP88CM49N, TMP88CK49F, and TMP88CM49F, are high-speed and high-function 8-bit singlechip microcomputers whose built-in features include large-capacity RAM, multi-function timer / counter, and 10-bit AD converter, serial interface (UART/I<sup>2</sup>C bus). They are equipped with 3 phase brushless DC sensorless / sensor motor control, and AC motor inverter control.

	Part No.	ROM	RAM	Package	OTP MCU
	TMP88CK49N	24K huter		P-SDIP64-750-1.78	TMP88PS49N
ſ	TMP88CK49F	24K bytes	1K bytes	P-QFP64-1420-1.00A	TMP88PS49F
	TMP88CM49N	22K huter	TK bytes	P-SDIP64-750-1.78	TMP88PS49N
ľ	TMP88CM49F	32K bytes		P-QFP64-1420-1.00A	TMP88PS49F

#### Features

- ♦ 8-bit single-chip microcomputer TLCS-870/X series microcomputer
- Interrupt sources: 34 (6 external, 28 Internal)
- ♦I/O ports: 56 pins
- Large-current output: 8 pins (typ. 20 mA), LED direct drive
   16-bit timer/counter: 2 channels
  - Timer, event counter, programmable pulse generator (PPG) output, pulse width measurement, external trigger timer, window mode
- 8-bit Timer/Counter: 3 channels
  - Timer, event counter, capture (pulse width/duty measurement), pulse width modulation (PWM) output, programmable divider output (PDO) mode
- Time base timer (interrupt frequency: 1 to 16384 Hz)
- Watchdog timer
- Divider output function (frequency: 1 to 8 kHz)
- Programmable motor driver (PMD): 2 channels
  - Rotor position: minimum resolution of 250 ns for detecting rotor position
  - Motor control timer, timer capture function
     Overload protection function
  - DC overload protection function AC overload protection function PWM output circuit)
  - Protection circuit for malfunction (urgent halt)
- Automatic direction change, automatic position detection start High-speed PWM output: 2 channels
- Cycle: 32 kHz, 64 kHz, 128 kHz
- Resolution: 8-bit, 7-bit, 6-bit mode selectable

P-SDIP64-750-1.78

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• For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

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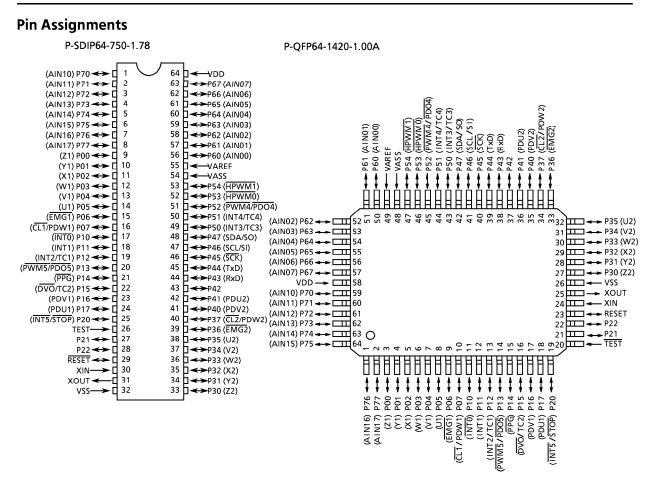


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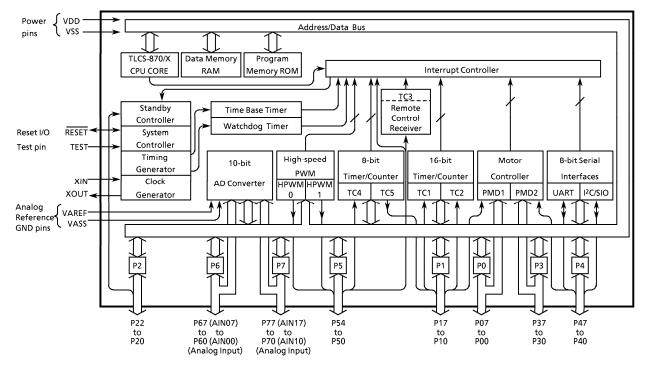
◆ Serial interface

- 8-bit SIO / I<sup>2</sup>C bus
- Universal asynchronous receiver transmitter (UART)
- ◆ 10-bit successive approximation type AD converter
- Analog input: 16 channels
   Conversion time: 11.5 μs / 46 μs (at 16 MHz operation)
   Low power dissipation operation (2 modes)

  - STOP mode: Stops oscillation (battery or capacitor backup). Port output hold or high impedance selectable
  - IDLE mode: Stops CPU but continues operation of peripheral hardware. Released by interrupt (restarts CPU)
- ◆Operating voltage: 4.5 to 5.5 V at 16 MHz operation ◆Emulation pod: BM88CM49N0A



### **Block Diagram**



# **Pin Function**

Pin Name	I/O	Function				
P07 (CL1/PDW1) P06 (EMG1)	I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable in units of bits. When using pins for motor control	Overload protection input 1/motor control circuit w1-phase position detection input Motor control circuit malfunction			
P05 (U1) P04 (V1)	 I/O (Output)	circuit, set accordingly using POCR, then MDCR to 1.	detection input 1 Motor control circuit U1-/V1-/W1-phase output			
P03 (W1) P02 (X1) P01 (Y1) P00 (Z1)			Motor control circuit X1-/ Y1-/Z1-phase output			
P00 (Z1) P17 (PDU1) P16 (PDV1)	··· I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable units of bits. When using pins for motor control	Motor control circuit U1-phase positior detection input Motor control circuit V1-phase positior			
P15 (DVO/TC2) P14 (PPG)	II/O (Output/Input)	circuit, timer/counter input, or external interrupt input, set them to input mode. When using pins for PPG output, divider	detection input Divider output or Timer/Counter 2 input Programmable pulse generator output			
P13 (PWM5/PDO5) P12 (INT2/TC1)	··· I/O (Output)	output, or PWM output/PDO output, set them to output mode.	PWM5 output/PDO5 output External interrupt input 2 or Timer			
P11 (INT1) P10 (INT0)	··· I/O (Input) 		Counter 1 input External interrupt input 1 External interrupt input 0			
P22 P21	··· I/O	3-bit I/O port When using pins for input port, external				
P20 (INT5/STOP)	l/O (Input)	interrupt input, or STOP mode release input, set output latches to 1.	External interrupt input 5 or STOP mode release signal input			
P37 (CL2/PDW2)	I/O (Input)	8-bit I/O port (large-current output) When using pins for motor control circuit input, set output latches to 1, then MDCR2 to 1.	Overload protection input 2/motor control circuit W2-phase position detection input Motor control circuit malfunction detection input 2			
P36 (EMG2)			Motor control circuit malfunction detection input 2			
P35 (U2) P34 (V2) P33 (W2)	 I/O (Output)		Motor control circuit U2-/V2-/W2-phase output			
P32 (X2) P31 (Y2) P30 (Z2)	 I/O (Output)		Motor control circuit X2-/Y2-/Z2-phase output			
P47 (SDA/SO)	I/O (I/O/Output)	8-bit I/O port				
P46 (SCL1/SI) P45 (SCK) P44 (TxD) P43 (RxD)	I/O (I/O/Input) I/O (I/O) I/O (Input) I/O (Output)	When using pins for motor control circuit input, UART/I <sup>2</sup> C/SIO, set output latches to 1.	I <sup>2</sup> C/SIO I/O UART data input UART data output			
P42 P41 (PDU2)	I/O		Motor control circuit U2-phase position detection input			
P40 (PDV2)	··· I/O (Input)		Motor control circuit V2-phase position detection input			

Pin Name	Input/Output	Put Function						
P54 (HPWM1) P53 (HPWM0)		5-bit input/output port with latch. When using pins for input port, HPWM	High-speed PWM output					
P52 (PWM4/PDO4)	l/O (Output)	output, PWM output/PDO output, external interrupt input, or	8-BIT PWM output 4 or, 8-bit programmable divider output 4					
P51 (INT4/TC4)	l/O (Input)	Timer/Counter input, set output latches to 1.	External interrupt 4 input or Timer/Counter 4 input					
P50 (INT3/TC3)	i/O (input)		External interrupt 3 input or Timer/Counter 3 input					
P67 (AIN07) to P60 (AIN00)	I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable in units of bits. When using pins for analog input, set to input mode using P6CR and ADCCR.	AD converter analog input					
P77 (AIN17) to P70 (AIN10)	I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable in units of bits. When using pins for analog input, set to input mode using P7CR and ADCCR.	AD converter analog input					
XIN, XOUT	Input, Output	High-frequency oscillator connecting pin and leave XOUT open.	ns. For external clock input, input to XIN					
RESET	I/O	Reset signal input, watchdog timer output, address trap reset output, system cla reset output						
TEST	Input	Shipment test pin, fix to "L" level.						
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)						
VAREF, VASS		Analog reference voltage for AD conversion	on. Reference GND.					

# Operation

# 1. CPU Core Functions

The CPU core consists of the CPU, system clock control circuit, and interrupt control circuit. This chapter describes the CPU core, program memory, data memory and the reset circuit.

## 1.1 Memory Address Map

The TMP88CK49/M49 memory consists of four blocks: ROM, RAM, special function registers (SFR) and Data buffer registers (DBR). They are all mapped to a 1 Mbyte address space. Figure 1-1 shows the TMP88CK49/M49 memory address map. There are 16 general-purpose registers mapped to the RAM address space.

SFR ( RAM DBR (	00000 <sub>H</sub> 0003F 00040 000BF 000C0 0043F 00043F 000F80	64 bytes 128 bytes 896 bytes 128 bytes	00000 <sub>H</sub> 0003F 00040 000BF 000C0 0043F 0043F 00580 005F5 :	64 bytes 128 bytes 896 bytes 128 bytes	General-purpose register banks (8 registers x 16 banks)		Read Only Memory includes Program memory Vector tables Random Access Memory includes Data memory Stack General-purpose register banks
ROM	<ul> <li>04000</li> <li>08FFF</li> </ul>	32 Kbytes	04000 09FFF	24 Kbytes	÷	SFR:	Special Function Register includes I/O ports Peripheral control registers Peripheral status registers System control registers Interrupt control registers Program Status Word
	FFF00 FFF3F FFF40 FFF7F FFF80	64 bytes 64 bytes 128 bytes 88CM49	FFF00 FFF3F FFF40 FFF7F FFF80 FFFF80 FFFFF	64 bytes 64 bytes 128 bytes 88CK49	Vector table for vector call instruction Vector table Vector table for interrup		Data Buffer Registers includes Motor control register UART control registers UART status registers Timer/counter 6 control registers

Figure 1-1. Memory Address Map

# 1.2 Program Memory (ROM)

TMP88CK49 contains a 24 Kbyte program memory (mask ROM) at addresses from 04000 to 09EFF<sub>H</sub>. TMP88CM49 contains a 32 Kbyte program memory (mask ROM) at addresses from 04000 to 0BEFF<sub>H</sub>. In addition, both contain a 256 byte program memory (mask ROM) at addresses from FFF00 to FFFF<sub>H</sub>.

## **Electrical Characteristics**

Absolute Maximum Ratings	(V <sub>SS</sub> =	0 V)			
Parameter	Symbol	Pins	Ratings	Unit	
Supply Voltage	V <sub>DD</sub>		– 0.3 to 6.5	V	
Input Voltage	V <sub>IN</sub>		– 0.3 to V <sub>DD</sub> + 0.3	V	
Output Maltage	V <sub>OUT1</sub>	Port P21, P22, RESET, Tri-state port	- 0.3 to V <sub>DD</sub> + 0.3	v	
Output Voltage	V <sub>OUT2</sub>	Port P20, Sink open drain port	– 0.3 to 5.5	]	
	I <sub>OUT1</sub>	Ports P1, P2, P4, P5, P6, P7	3.2		
Output Current	I <sub>OUT2</sub>	Port P0	20	mA	
Output Current	I <sub>OUT3</sub>	Port P3	30		
	$\Sigma I_{OUT1}$	Ports P1, P2, P4, P5, P6, P7	120		
Output Current	$\Sigma I_{OUT2}$	Port P0	60	mA	
	$\Sigma I_{OUT3}$	Port P3	120		
Deven Dissignation [Terms 70%]		TMP88CK49N/TMP88CM49N	600		
Power Dissipation [Topr = 70°C]	PD	TMP88CK49F/TMP88CM49F	350	- mW	
Soldering Temperature (time)	Tsld		260 (10 s)	°C	
Storage Temperature	Tstg		– 55 to 125	°C	
Operating Temperature	Topr		– 40 to 85	°C	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating	g Conditions	(V <sub>SS</sub> = 0 V, Topr = -	40 to 85°C)	)			
Parameter	Symbol	Pins	c	Conditions		Max	Unit
			fc =	NORMAL mode			
Supply Voltage	V <sub>DD</sub>		16 MHz	IDLE mode	4.5	5.5	V
				STOP mode			
	V <sub>IH1</sub>	Except hysteresis input	$V_{DD} \ge 4.5 V$		V <sub>DD</sub> × 0.70		
Input High Voltage	V <sub>IH2</sub>	Hysteresis input			$V_{DD} \times 0.75$	V <sub>DD</sub>	V
	V <sub>IH3</sub>		v v	<sub>DD</sub> <4.5 V	$V_{DD} \times 0.90$	V <sub>DD</sub>	
	V <sub>IL1</sub>	Except hysteresis input		$V_{DD} \ge 4.5 V$		$V_{DD} \times 0.30$	
Input Low Voltage	V <sub>IL2</sub>	Hysteresis input	v v			$V_{DD} \times 0.25$	V
	V <sub>IL3</sub>		V	<sub>DD</sub> <4.5 V		V <sub>DD</sub> × 0.10	
Clock Frequency	fc	XIN, XOUT	V <sub>DD</sub>	= 4.5 to 5.5 V	8.0	16.0	MHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: The condition of supply voltage range is the value in NORMAL and IDLE modes.

D.C. Characte	eristics	$(V_{SS} = 0 V, Topr = -40 tc$	985°C)				
Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis inputs		-	0.9	-	v
	I <sub>IN1</sub>	TEST					
Input Current	I <sub>IN2</sub>	Sink open drain, Tri-state ports		-	-	± 2	μA
	I <sub>IN3</sub>	RESET, STOP	Conditions         Min         Typ.         I $-$ 0.9         -         0.9 $V_{DD} = 5.5 V$ $   V_{IN} = 5.5 V/0 V$ $   20$ 70 $  V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V$ $  V_{DD} = 4.5 V, V_{OLT} = 5.5 V/0 V$ $  V_{DD} = 4.5 V, V_{OL} = 0.7 mA$ $4.1$ $ V_{DD} = 4.5 V, V_{OL} = 0.4 V$ $ 1.6$ $V_{DD} = 4.5 V, V_{OL} = 1.0 V$ $ 1.6$ $V_{DD} = 5.5 V$ $ 20$ $V_{DD} = 5.5 V$ $ 20$ $V_{DD} = 5.5 V$ $ 10$ $V_{DD} = 5.5 V$ $ 10$				
la suit De siste s (*)		TEST with pull-down		20	70	170	1.0
Input Resistor (*)	R <sub>IN</sub>	RESET		90	220	510	kΩ
Output Leakage Current	I <sub>OL</sub>	Sink open drain, Tri-state ports	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V/0 V	-	-	± 2	μA
Output High Voltage	V <sub>OH</sub>	Tri-state ports	$V_{DD} = 4.5 V, I_{OH} = -0.7 mA$	4.1	_	I	v
	I <sub>OL1</sub>	Except XOUT, Ports P0, P3.	$V_{DD} = 4.5 V, V_{OL} = 0.4 V$	-	1.6	-	
Output Low Current	I <sub>OL2</sub>	Port P0		6	10	-	mA
	I <sub>OL3</sub>	Port P3	$v_{DD} = 4.5 v, v_{OL} = 1.0 v$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-	1	
Supply Current in NORMAL Mode				-	20	32	mA
Supply Current in IDLE Mode				-	10	16	mA
Supply Current in STOP Mode			V <sub>DD</sub> = 5.5 V V <sub>IN</sub> = 5.3 V/0.2 V	_	0.5	20	μΑ

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD}$  = 5 V.

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Note 2: Input Current I<sub>IN1</sub>, I<sub>IN3</sub>; The current through registor is not included, when the input resistor (pull-up or pull-down) is contained.

Note 3: IDD except I<sub>REF</sub>.

AD Conversion Characteris	tics	(Topr = - 40 to 85°C)							
						Max			
Parameter	Symbol	Conditions	Min	Тур.	ADCDR1		DR2	Unit	
						ACK = 0	ACK = 1		
Analog Reference Voltage	V <sub>AREF</sub>		V <sub>DD</sub> – 1.0	—	V <sub>DD</sub>		v		
Analog Neterence Voltage	V <sub>ASS</sub>	V <sub>AREF</sub> – V <sub>ASS</sub> ≧3.5 V	V <sub>SS</sub>	_	1.0			V	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>ASS</sub>	—		V <sub>AREF</sub>		V	
Analog Supply Current	I <sub>REF</sub>	V <sub>AREF</sub> = 5.5 V, V <sub>ASS</sub> = 0.0 V	_	0.5		1.0		mA	
Non-Linearity Error			_	_	± 1	± 3	± 2		
Zero Point Error		$V_{DD} = 5.0 V, V_{SS} = 0.0 V$	_	_	± 1	± 3	± 2		
Full Scale Error		V <sub>AREF</sub> = 5.000 V V <sub>ASS</sub> = 0.000 V	_	_	± 1	± 3	± 2	LSB	
Total Error			_	_	± 2	± 6	± 4		

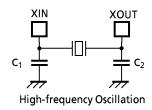
ADCDR2: 10-bit AD conversion result (1LSB =  $\Delta V_{AREF}/250$ ) ADCDR2: 10-bit AD conversion result (1LSB =  $\Delta V_{AREF}/1024$ ) Note 2: Total error includes all errors except quantization error.

A.C. Characteristics		$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$						
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit		
Machine Cycle Time	tov	NORMAL mode	0.25		0.5			
Machine Cycle Time	tcy	IDLE mode	0.23	_	0.5	μs		
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation	31.25		62.5			
Low Level Clock Pulse Width	t <sub>WCL</sub>	(XIN input)	51.25	_	02.5	ns		

Recommended Oscillating Conditions

 $(V_{SS} = 0 V, V_{DD} = 4.5 \text{ to } 5.5 V, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Oscillator	Oscillation	Recommended Oscillator	Recommended Constant		
Faranieter	Oscillator	Frequency	Recommended Oscillator C <sub>1</sub>		C <sub>2</sub>	
High-frequency Oscillation	Ceramic Resonator	16 MHz	MURATA CSA 16.00 MXZ	5 pF	5 pF	
	Ceramic Resonator		MURATA CST 16.00 MXW	built-in 5 pF	built-in 5 pF	



Note: An electrical shield by metal shield on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.