

CMOS 8-Bit Microcontroller

TMP87CM24AF, TMP87CP24AF

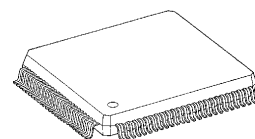
The TMP87CM24A/P24A are the high speed and high performance 8-bit single chip microcomputers. These MCU contain, large ROM, RAM, input/output ports, LCD driver, a 8-bit AD converter, four multi-function timer/counters, two serial interfaces, and two clock generators on chip.

| Product No. | ROM | RAM | Package | OTP MCU |
|-------------|---------------|--------------|----------------------|------------|
| TMP87CM24A | 32 K × 8 bits | 2 K × 8 bits | P-LQFP100-1414-0.50C | TMP87PP24A |
| TMP87CP24A | 48 K × 8 bits | | | |

Features

- ◆ 8-bit single chip microcomputer TLCS-870 Series
- ◆ Instruction execution time: 0.5 μ s (at 8 MHz), 122 μ s (at 32 kHz)
- ◆ 129 types and 412 basic instructions
 - Multiplication and Division (8 bits × 8 bits, 16 bits ÷ 8 bits): Execution time 3.5 μ s (at 8 MHz)
 - Bit manipulations (Set/Clear/Complement/Load/Store/Test/Exclusive OR)
 - 16-bit data operations
 - 1-byte jump/call (Short relative jump/Vector call)
- ◆ 14 interrupt sources (External: 5, Internal: 9)
 - All sources have independent latches each, and nested interrupt control is available
 - 4 edge-selectable external interrupts with noise reject
 - High-speed task switching by register bank changeover
- ◆ 10-input/output ports (Max 69 pins)
- ◆ Two 16-bit timer/counters
 - Timer, Event counter, External trigger timer, Window, PPG output Pulse width measurement modes
- ◆ Two 8-bit timer/counters
 - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, PDO modes
- ◆ Time Base Timer (Interrupt frequency: 1 Hz to 16384 kHz)
- ◆ Divider output function (frequency: 1 kHz to 8 kHz)
- ◆ Watchdog Timer
- ◆ Two 8-bit Serial Interfaces
 - Each 8 bytes transmit/receive data buffer
 - Internal/external serial clock, and 4-/8-bit mode

P-LQFP100-1414-0.50C



TMP87CM24AF
TMP87CP24AF
TMP87PP24AF

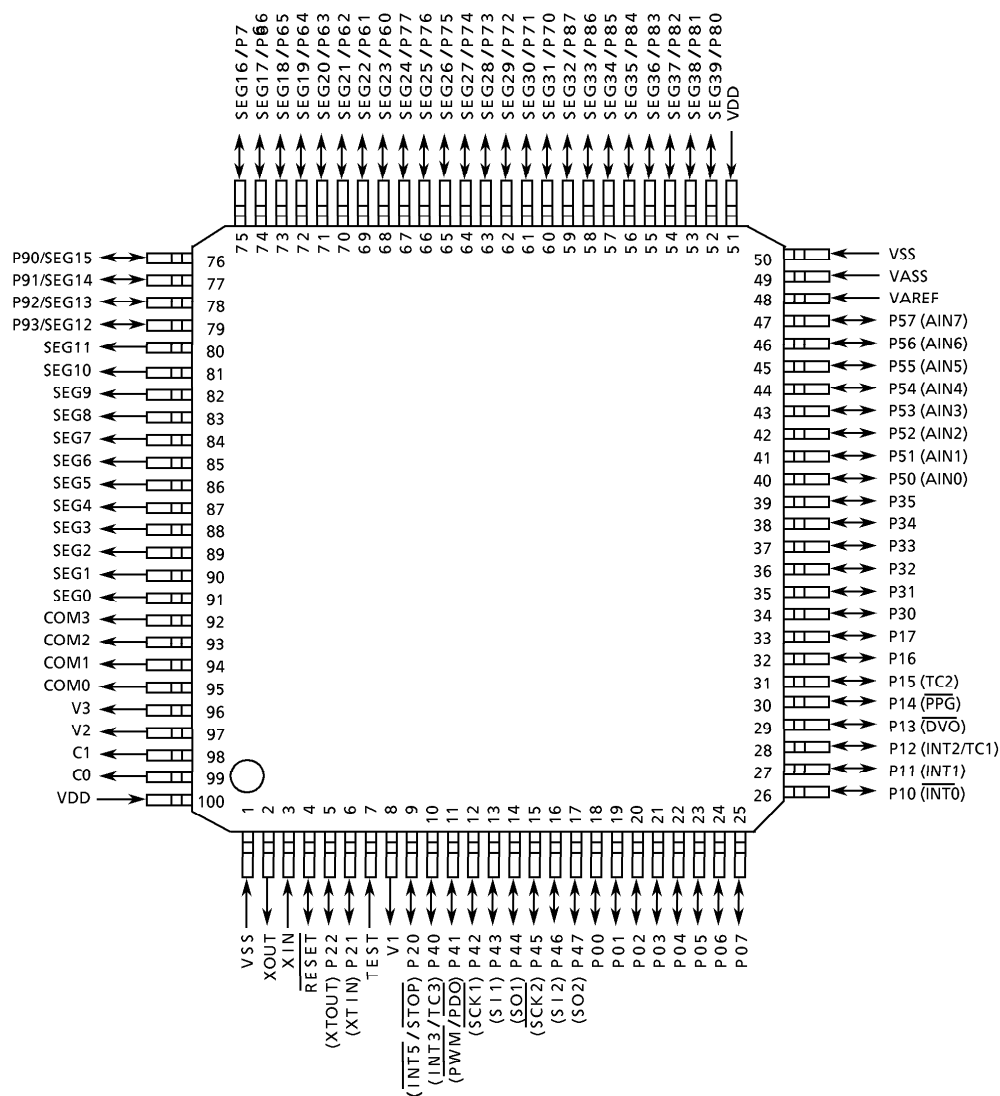
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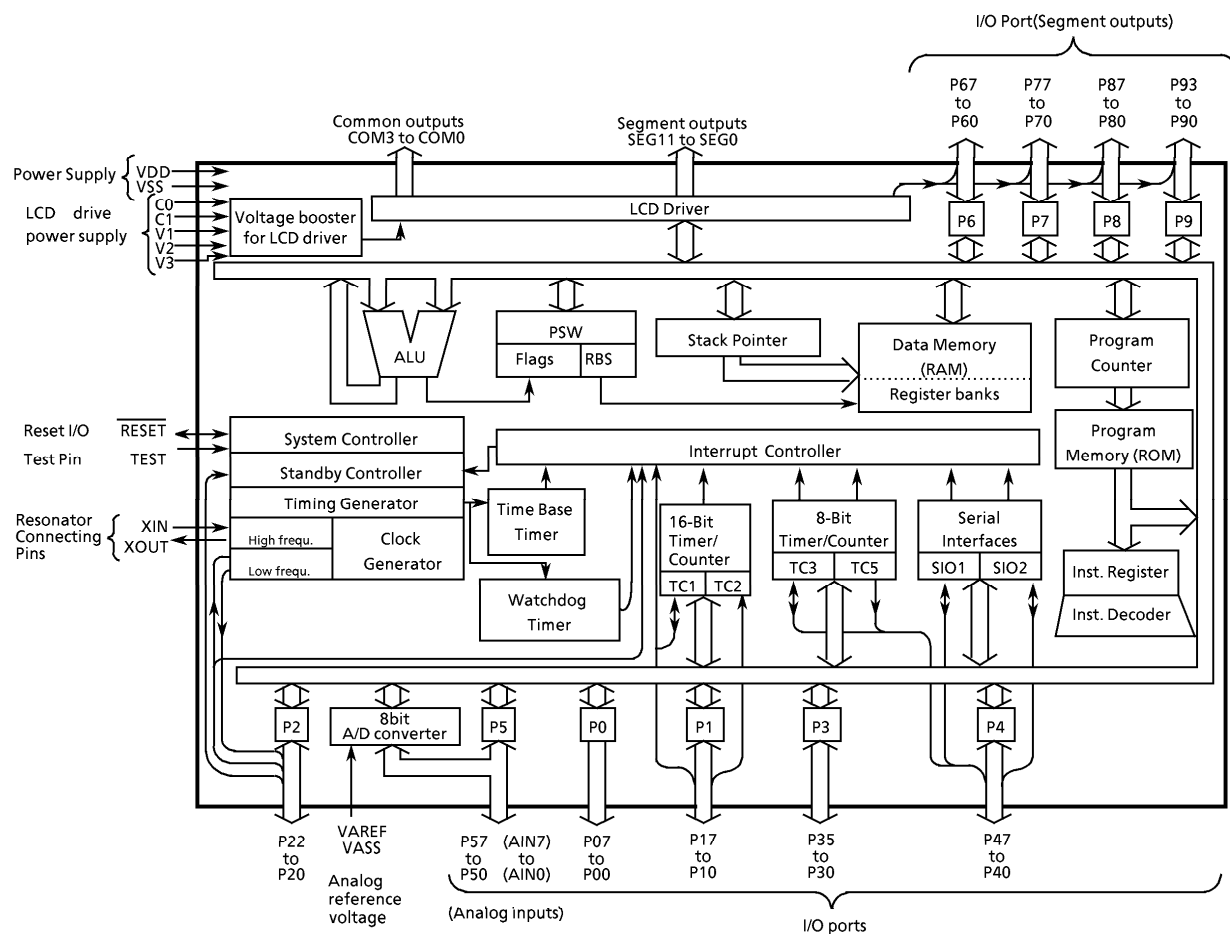
- ◆ LCD driver
 - Built-in voltage booster for LCD driver
 - With display memory (20 bytes)
 - LCD direct drive capability (Max 40 seg × 4 com)
 - 1/4, 1/3, 1/2 duty or static drive are programmably selectable
- ◆ 8-bit successive approximate type AD converter with sample and hold
 - 8 analog inputs
 - Conversion time: 23 μ s/92 μ s (at 8 MHz)
- ◆ Dual clock operation (optional)
- ◆ Five Power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
 - SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
 - IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock.
Release by interrupts.
 - IDLE2 mode: CPU stops, and Peripherals operate using high and low frequency clock.
Release by interrupts.
 - SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock.
Release by interrupts.
- ◆ Operating Voltage: 2.2 to 5.5 V at 4.2 MHz/32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz
- ◆ Emulation Pod: BM87CP24F0A

Pin Assignments (Top View)

P-LQFP100-1414-0.50C



Block Diagram



Pin Functions

| Pin Name | Input/Output | Function | |
|-------------------------------|-------------------------|---|---|
| P07 to P00 P17, P16 | I/O | 8-bit programmable input/output ports (tri-state). | |
| P15 (TC2) | I/O (Input) | Each bit of these ports can be individually configured as an input or an output under software control. | Timer/Counter 2 input |
| P14 (PPG) | I/O (Output) | | Programmable pulse generator output |
| P13 (DVO) | I/O (Input) | When used as an input port, timer/counter input or external interrupt input, the P0CR/P1CR must be set to "0". When used as timer/counter output or divider output, the P0CR/P1CR must be set to "1" after setting output latch to "1". | Divider output |
| P12 (INT2/TC1) | | | External interrupt 2 input or Timer/Counter 1 input |
| P11 (INT1) | | | External interrupt 1 input |
| P10 (INT0) | | | External interrupt 0 input |
| P22 (XTOUT) | I/O (Output) | 3-bit input/output port with latch. | Resonator connecting pins (32.768 kHz). |
| P21 (XTIN) | I/O (Input) | When used as an input port, external interrupt input or STOP mode release input, the output latch must be set to "1". | For inputting external clock, XTIN is used and XTOUT is opened. |
| P20 (INT5/STOP) | | | External interrupt 5 input or STOP mode release signal input |
| P35 to P30 | I/O | 6-bit input/output port with latch. When used as input port, the output latch must be set to "1". | |
| P47 (SO2) | I/O (Output) | 8-bit input/output port with latch. | SIO2 serial data output |
| P46 (SI2) | I/O (Input) | When used as serial interface output or timer/counter output, the P4CR1 must be set to "1" after setting output latch to "1". | SIO2 serial data input |
| P45 (SCK2) | I/O (I/O) | | SIO2 serial clock input/output |
| P44 (SO1) | I/O (Output) | When used as an input port, serial interface input or external interrupt input, the P4CR1 must be set to "0". | SIO1 serial data output |
| P43 (SI1) | I/O (Input) | | SIO1 serial data input |
| P42 (SCK1) | I/O (I/O) | | SIO1 serial clock input/output |
| P41 (PWM/PDO) | I/O (Output) | | 8-bit PWM output, 8-bit programmable divider output |
| P40 (INT3/TC3) | I/O (Input) | | External interrupt 3 input, Timer/Counter 3 input |
| P57 (AIN07) to P50 (AIN00) | I/O (Input) | 8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output under software control. When used as analog input, the P5CR must be set to "0". | AD converter analog inputs |
| SEG39 (P80) to SEG32 (P87) | Output (I/O) | 8-bit input/output port with latch. | LCD segment outputs. When used as segment output, the segment output control register must be set to "1". |
| SEG31 (P70) to SEG24 (P77) | Output (I/O) | When used as an input port, the segment output control register must be set to "0" after setting output latch to "1". | |
| SEG23 (P60) to SEG16 (P67) | Output (I/O) | | |
| SEG15 (P90) to SEG12 (P93) | Output (I/O) | 4-bit input/output port with latch. When used as an input port, the segment output control register must be set to "0" after setting output latch to "1". | |
| SEG11 to SEG0 | Output | LCD segment outputs | |
| COM3 to COM0 | Output | LCD common outputs | |
| XIN, XOUT | Input, Output | Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened. | |
| RESET | I/O | Reset signal input or watchdog timer output/address-trap-reset output | |
| TEST | Input | Test pin for out-going test. Be fixed to low. | |
| VDD, VSS | Power Supply | + 5 V, 0 V (GND) | |
| VAREF, VASS | | Analog reference voltage inputs (High, Low) | |
| C0, C1, V1, V2, V3 | LCD voltage booster pin | LCD voltage booster pin. Capacitors are required between C0 and C1 pin and between V1/V2/V3 pin and GND. | |

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the TMP87CM24A/P24A. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

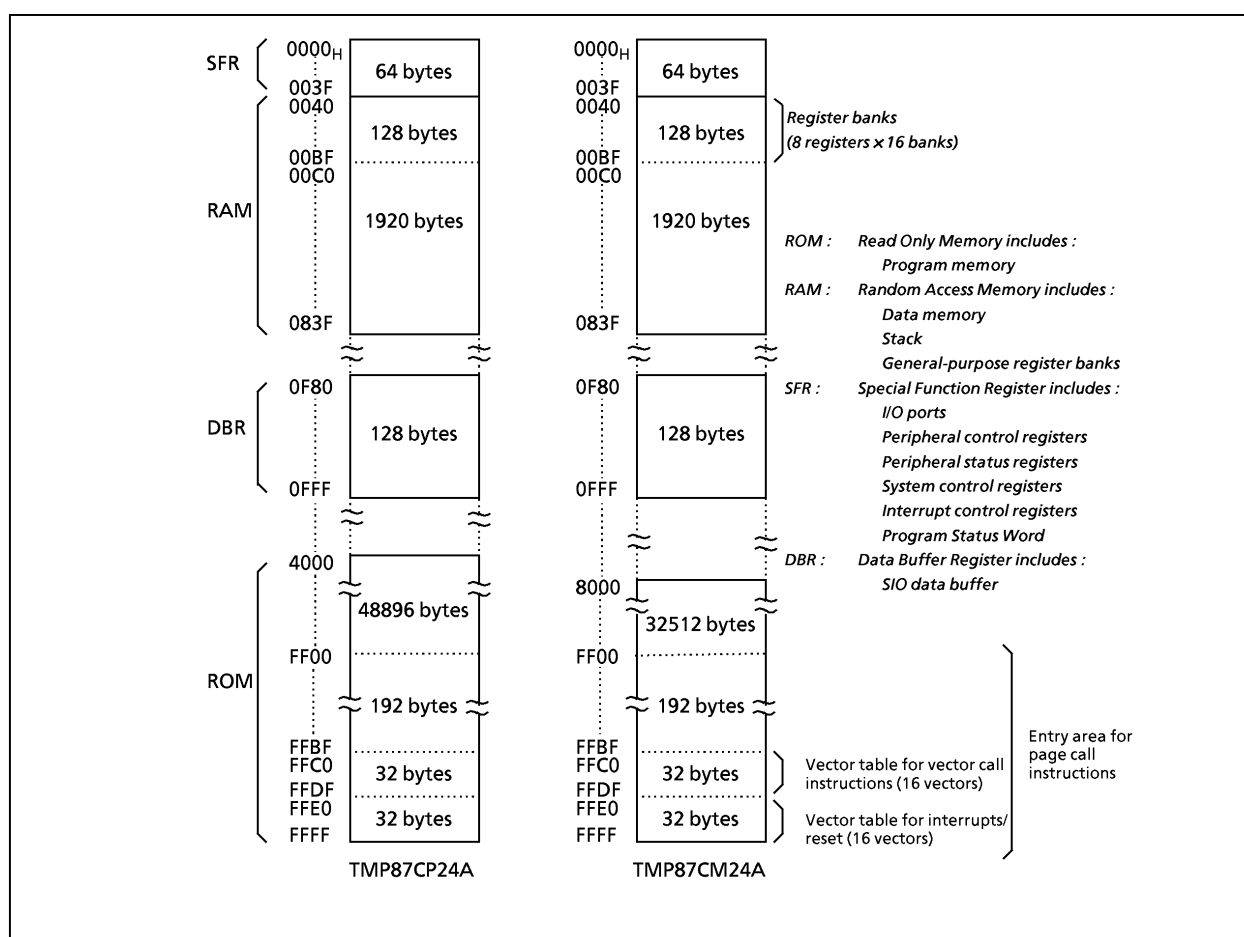


Figure 1-1. Memory Address Maps

Electrical Characteristics

| Absolute Maximum Ratings | | (V _{SS} = 0 V) | | |
|---|---------------------|---|--------------------------------|------|
| Parameter | Symbol | Pins | Ratings | Unit |
| Supply Voltage | V _{DD} | | – 0.3 to 6.5 | V |
| Input Voltage | V _{IN} | | – 0.3 to V _{DD} + 0.3 | |
| Output Voltage | V _{OUT1} | Except P20 and P3 ports | – 0.3 to V _{DD} + 0.3 | |
| | V _{OUT2} | Ports P20, P3 | – 0.3 to 5.5 | |
| Output Current (Per 1 pin) | I _{OUT1} | Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41) | 3.2 | mA |
| | I _{OUT2} | P41 | 30 | |
| Output Current (Total) | Σ I _{OUT1} | Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41) | 120 | |
| | Σ I _{OUT2} | P41 | 30 | |
| Power Dissipation [T _{opr} = 70°C] | PD | | 350 | mW |
| Soldering Temperature (time) | T _{sld} | | 260 (10 s) | °C |
| Storage Temperature | T _{stg} | | – 55 to 125 | |
| Operating Temperature | T _{opr} | | – 10 to 70 | |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

| Recommended Operating Conditions | | | (V _{SS} = 0 V, T _{opr} = – 10 to 70°C) | | | | |
|----------------------------------|------------------|-------------------------|--|-----------------|-------------------------|-------------------------|------------------------|
| Parameter | Symbol | Pins | Conditions | | Min | Max | Unit |
| Supply Voltage | V _{DD} | | f _c = 8 MHz | NORMAL1, 2 mode | 4.5 | 5.5 | V |
| | | | | IDLE1, 2 mode | | | |
| | | | f _c = 4.2 MHz | NORMAL1, 2 mode | 2.2 | | |
| | | | | IDLE1, 2 mode | | | |
| | | | f _s = 32.768 kHz | SLOW mode | 2.0 | | |
| | | | | SLEEP mode | | | |
| | STOP mode | | | | | | |
| Input High Voltage | V _{IH1} | Except hysteresis input | V _{DD} ≥ 4.5 V | | V _{DD} × 0.70 | V _{DD} | |
| | V _{IH2} | Hysteresis input | | | V _{DD} × 0.75 | | |
| | V _{IH3} | | | | V _{DD} < 4.5 V | | V _{DD} × 0.90 |
| Input Low Voltage | V _{IL1} | Except hysteresis input | V _{DD} ≥ 4.5 V | | 0 | V _{DD} × 0.30 | |
| | V _{IL2} | Hysteresis input | | | | V _{DD} × 0.25 | |
| | V _{IL3} | | | | | V _{DD} < 4.5 V | |
| Clock Frequency | f _c | XIN, XOUT | V _{DD} = 4.5 to 5.5 V | | 0.4 | 8.0 | MHz |
| | | | V _{DD} = 2.2 to 5.5 V | | | 4.2 | |
| | f _s | XTIN, XTOUT | | | 30.0 | 34.0 | kHz |

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL1/2 mode and IDLE1/2 mode.

DC Characteristics

(V_{SS} = 0 V, T_{opr} = -10 to 70°C)

| Parameter | Symbol | Pins | Conditions | Min | Typ. | Max | Unit |
|------------------------------------|-------------------|--------------------------------------|--|-----------------------|------|------|------|
| Hysteresis Voltage | V _{HS} | Hysteresis inputs | | — | 0.9 | — | V |
| Input Current | I _{IN1} | TEST | V _{DD} = 5.5 V, V _{IN} = 5.5 V/0 V | — | — | ± 2 | μA |
| | I _{IN2} | Open-drain ports and tri-state ports | | | | | |
| | I _{IN3} | RESET, STOP | | | | | |
| Input Low Current | I _{IL} | Push-pull ports | V _{DD} = 5.5 V, V _{IN} = 0.4 V | — | — | – 2 | mA |
| Input Resistance | R _{IN2} | RESET | | 100 | 220 | 450 | kΩ |
| Output Leakage Current | I _{LO1} | Open drain ports | V _{DD} = 5.5 V, V _{OUT} = 5.5 V | — | — | 2 | μA |
| | I _{LO2} | Tri-state ports | V _{OUT} = 5.5 V/0 V | — | — | ± 2 | |
| Segment/Common Output Voltage | V _{LCD1} | SEG39 to SEG0 and COM3 to COM0 | | 0.75 | 1.0 | 1.33 | V |
| | V _{LCD2} | | | V _{LCD1} × 2 | | | |
| | V _{LCD3} | | | V _{LCD1} × 3 | | | |
| Output High Voltage | V _{OH1} | Push-pull ports (P4 port) | V _{DD} = 4.5 V, I _{OH} = – 200 μA | 2.4 | — | — | V |
| | V _{OH2} | Tri- state ports (P0, P1, P5 ports) | V _{DD} = 4.5 V, I _{OH} = – 0.7 mA | 4.1 | — | — | |
| Output Low Voltage | V _{OL} | Except XOUT and P41 | V _{DD} = 4.5 V, I _{OL} = 1.6 mA | — | — | 0.4 | |
| Output Low Current | I _{OL3} | P41 | V _{DD} = 4.5 V, V _{OL} = 1.0 V | — | 20 | — | |
| Supply Current in NORMAL 1, 2 mode | I _{DD} | | V _{DD} = 5.5 V f _c = 8 MHz f _s = 32.768 kHz V _{IN} = 5.3 V/0.2 V | — | 10 | 16 | mA |
| Supply Current in IDLE 1, 2 mode | | | | — | 6 | 10 | |
| Supply Current in SLOW mode | | | V _{DD} = 3.0 V f _s = 32.768 kHz V _{IN} = 2.8 V/0.2 V Voltage boost frequency = 1 kHz | — | 30 | 70 | μA |
| Supply Current in SLEEP mode | | | | — | 15 | 40 | |
| Supply Current in STOP mode | | | V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V | — | 0.5 | 10 | |

Note 1: Typical values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input Current; The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD}; Except for I_{REF}Note 4: V_{LCD2} indicates an output voltage at the 2/3 level when operating in the 1/4 or 1/3 duty mode.Note 5: V_{LCD1} indicates an output voltage at the 1/3 level when operating in the 1/4 or 1/3 duty mode.

Note 6: SEG/COM output voltage indicates an output voltage at no local.

| Topr [°C] | V _{LCD1} | | | Unit |
|-----------|-------------------|------|------|------|
| | Min | typ. | Max | |
| -10 | 1.03 | — | 1.33 | V |
| 25 | 0.85 | 1.0 | 1.15 | |
| 70 | 0.75 | — | 1.00 | |

AD Conversion Characteristics (I)

(Topr = - 10 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|--------------------------|-------------------|--|-----------|------|------------|------|
| Analog Reference Voltage | V_{AREF} | $V_{AREF} - V_{ASS} \geq 2.5 \text{ V}$ | 2.7 | — | V_{DD} | V |
| | V_{ASS} | | V_{SS} | — | 1.5 | |
| Analog Input Voltage | ΔV_{AREF} | | 2.5 | — | — | |
| Analog Input Voltage | V_{AIN} | | V_{ASS} | — | V_{AREF} | |
| Analog Supply Current | I_{REF} | $V_{AREF} = 5.5 \text{ V}, V_{ASS} = 0.0 \text{ V}$ | — | 0.5 | 1.0 | mA |
| Nonlinearity Error | | $V_{DD} = 2.7 \text{ V to } 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 5.000 \text{ V}, 2.700 \text{ V}$ $V_{ASS} = 0.000 \text{ V}$ | — | — | ± 1 | LSB |
| Zero Point Error | | | — | — | ± 1 | |
| Full Scale Error | | | — | — | ± 1 | |
| Total Error | | | — | — | ± 2 | |

Note: Quantizing error is not contained in those errors.

AD Conversion Characteristics (II)

(Topr = - 10 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|--------------------------|--------------------|---|------------------|------|-------------------|------|
| Analog Reference Voltage | V _{AREF} | | 2.2 | — | V _{DD} | V |
| | V _{ASS} | | V _{SS} | | | |
| Analog Input Voltage | △V _{AREF} | | 2.2 | — | — | |
| Analog Input Voltage | V _{AIN} | | V _{ASS} | — | V _{AREF} | |
| Analog Supply Current | I _{REF} | V _{AREF} = 5.5 V, V _{ASS} = 0.0 V | — | 0.5 | 1.0 | mA |
| Nonlinearity Error | | V _{DD} = 2.2 V, V _{SS} = 0.0 V V _{AREF} = 2.200 V V _{ASS} = 0.000 V | — | — | ± 2 | LSB |
| Zero Point Error | | | — | — | ± 2 | |
| Full Scale Error | | | — | — | ± 2 | |
| Total Error | | | — | — | ± 4 | |

Note: Quantizing error is not contained in those errors.

AC Characteristics (I)

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 10 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|------------------------------|------------------|---|-------|------|-------|------|
| Machine Cycle Time | t _{cy} | In NORMAL1, 2 modes | 0.5 | – | 10 | μs |
| | | In IDLE 1, 2 modes | | | | |
| | | In SLOW mode | 117.6 | – | 133.3 | |
| | | In SLEEP mode | | | | |
| High Level Clock Pulse Width | t _{WCH} | For external clock operation (XIN input), f _c = 8 MHz | 50 | – | – | ns |
| Low Level Clock Pulse Width | t _{WCL} | | | | | |
| High Level Clock Pulse Width | t _{WSH} | For external clock operation (XTIN input), f _s = 32.768 kHz | 14.7 | – | – | μs |
| Low Level Clock Pulse Width | t _{WSL} | | | | | |

AC Characteristics (II)

(V_{SS} = 0 V, V_{DD} = 2.2 to 5.5 V, T_{opr} = – 10 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|------------------------------|------------------|--|-------|------|-------|------|
| Machine Cycle Time | t _{cy} | In NORMAL1, 2 modes | 0.95 | – | 10 | μs |
| | | In IDLE 1, 2 modes | | | | |
| | | In SLOW mode | 117.6 | – | 133.3 | |
| | | In SLEEP mode | | | | |
| High Level Clock Pulse Width | t _{WCH} | For external clock operation (XIN input), f _c = 4.2 MHz | 110 | – | – | ns |
| Low Level Clock Pulse Width | t _{WCL} | | | | | |
| High Level Clock Pulse Width | t _{WSH} | For external clock operation (XTIN input), f _s = 32.768 kHz | 14.7 | – | – | μs |
| Low Level Clock Pulse Width | t _{WSL} | | | | | |

Recommended Oscillating Condition (I)

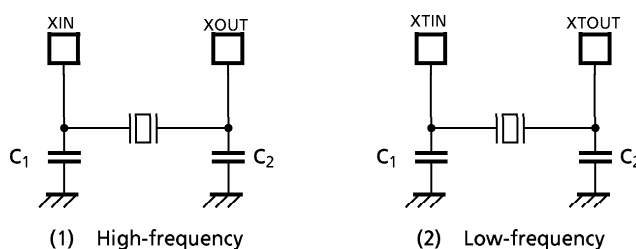
 $(V_{SS} = 0\text{ V}, V_{DD} = 4.5\text{ to }5.5\text{ V}, T_{opr} = -10\text{ to }70^{\circ}\text{C})$

| Parameter | Oscillator | Frequency | Recommender Oscillator | Recommended Condition | |
|----------------|--------------------|------------|---|-----------------------|----------------|
| | | | | C ₁ | C ₂ |
| High-frequency | Ceramic Resonator | 8 MHz | KYOCERA KBR8.0M | 30 pF | 30 pF |
| | | | Standard/Lead Type (MURATA) CSA8.00MTZ CST8.00MTW | built-in 30 pF | built-in 30 pF |
| | | | Standard/SMP Type (MURATA) CSAC58.00MT | 30 pF | 30 pF |
| | | | Standard/Small Chip Type (MURATA) CSTCS8.00MT | built-in 30 pF | built-in 30 pF |
| | Crystal Oscillator | 4 MHz | KYOCERA KBR4.0M5 | 30 pF | 30 pF |
| | | 8 MHz | TOYOCOM 210B 8.0000 | 20 pF | 20 pF |
| Low-frequency | Crystal Oscillator | 4 MHz | TOYOCOM 204B 4.0000 | 20 pF | 20 pF |
| | | 32.768 kHz | NDK MX-38T | 15 pF | 15 pF |

Recommended Oscillating Condition (II)

 $(V_{SS} = 0\text{ V}, V_{DD} = 2.2\text{ to }5.5\text{ V}, T_{opr} = -10\text{ to }70^{\circ}\text{C})$

| Parameter | Oscillator | Frequency | Recommender Oscillator | Recommended Condition | |
|----------------|-------------------|-----------|---|-----------------------|----------------|
| | | | | C ₁ | C ₂ |
| High-frequency | Ceramic Resonator | 4 MHz | Standard/Lead Type (MURATA) CSA4.00MG | 30 pF | 30 pF |
| | | | CST4.00MGW | built-in 30 pF | built-in 30 pF |
| | | | Standard/SMD Type (MURATA) CSA4.00MGC CSAC4.00MGCM CSTC4.00MG | 30 pF | 30 pF |
| | | | | built-in 30 pF | built-in 30 pF |
| | | | Standard/Small Chip Type CSTCS4.00MG | built-in 10 pF | built-in 10 pF |



Note1: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

Note2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
<http://www.murata.co.jp/search/index.html>

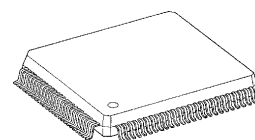
CMOS 8-Bit Microcontroller

TMP87PP24AF

The TMP87PP24A is a One-Time PROM microcontroller with low-power 384 Kbits electrically programmable read only memory for the TMP87CM24A/CP24A system evaluation. The TMP87PP24A is pin compatible with the TMP87CM24A/CP24A. The operations possible with the TMP87CM24A/CP24A can be performed by writing programs to PROM. The TMP87PP24A can write and verify in the same way as the TMM571000D using an adaptor socket BM11127 and an EPROM programmer.

| Product No. | OTP | RAM | Package | OTP Adapter |
|-------------|---------------|--------------|----------------------|-------------|
| TMP87PP24AF | 48 K × 8 bits | 2 K × 8 bits | P-LQFP100-1414-0.50C | BM11127 |

P-LQFP100-1414-0.50C



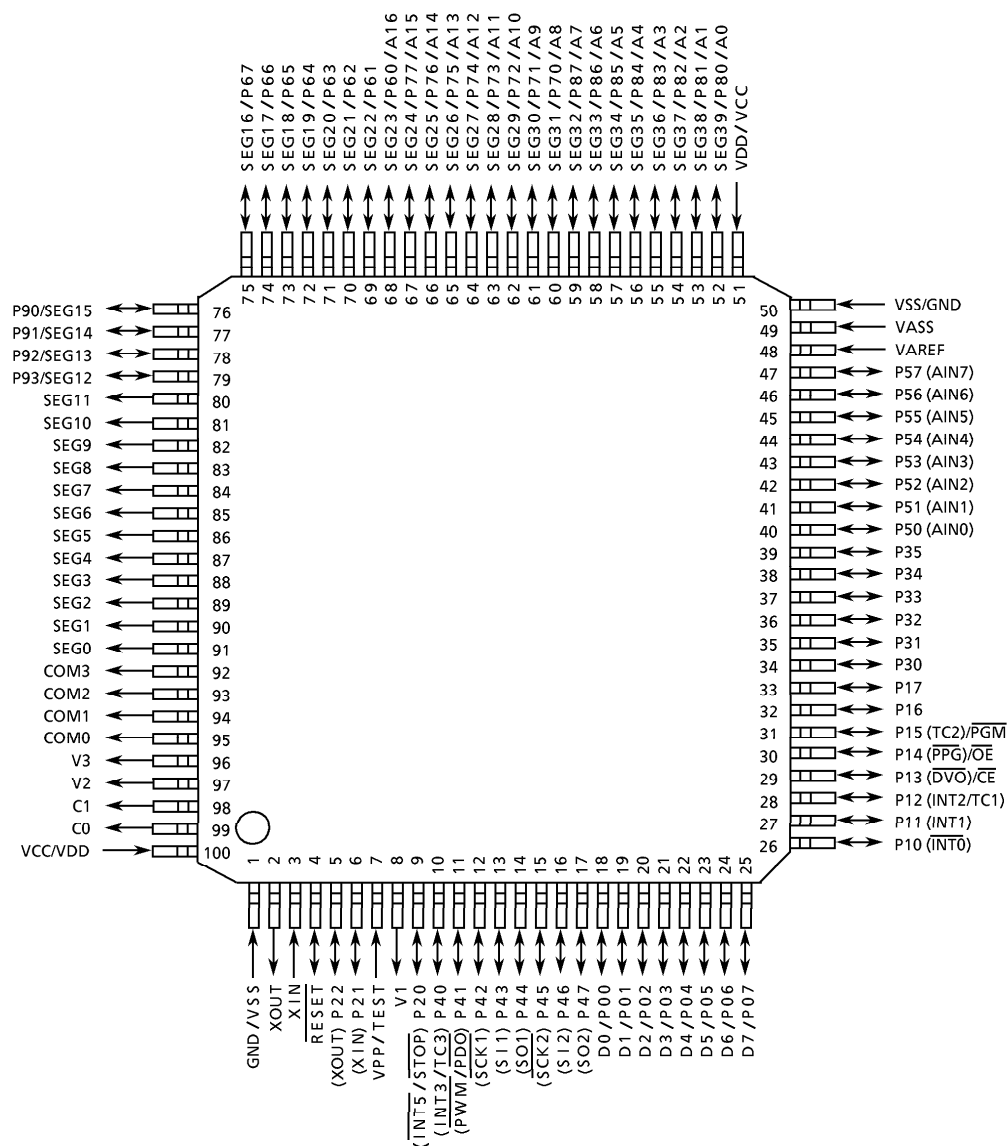
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Pin Assignments (Top View)

P-LQFP100-1414-0.50C



Pin Function

The TMP87PP24A has two modes: MCU and PROM.

(1) MCU mode

In this mode, the TMP87PP24A is pin compatible with the TMP87CM24A/CP24A (fix the TEST pin at low level.)

(2) PROM mode

| Pin Name (PROM mode) | Input/Output | Function | Pin Name (MCU mode) |
|----------------------|--------------|--|---------------------|
| A16 | Input | PROM address inputs | P60 |
| A15 to A8 | | | P77 to P70 |
| A7 to A0 | | | P87 to P80 |
| D7 to D0 | I/O | PROM data input/outputs | P07 to P00 |
| \overline{CE} | Input | Chip enable signal input (active low) | P13 |
| \overline{OE} | | Output enable signal input (active low) | P14 |
| \overline{PGM} | | Program mode signal input | P15 |
| VPP | Power supply | + 12.75 V/5 V (Program supply voltage) | TEST |
| VCC | | + 6.25 V/5 V | VDD |
| GND | | 0 V | VSS |
| P35 to P30 | I/O | Pull-up with resistance for input processing. | |
| P47 to P40 | | | |
| P57 to P50 | | | |
| P67 to P62 | | | |
| P93 to P90 | | | |
| P11 | | PROM mode setting pin. Be fixed at high level. | |
| P21 | | | |
| P31 | | | |
| P61 | | PROM mode setting pin. Be fixed at low level. | |
| P17, P16, P12, P10 | | | |
| P22, P20 | | | |
| \overline{RESET} | | | |
| XIN | Input | Connect an 8 MHz oscillator to stabilize the internal state. | |
| XOUT | Output | | |
| VAREF | Power supply | 0 V (GND) | |
| VASS | | | |
| COM3 to COM0 | Output | Open | |
| SEG11 to SEG0 | | | |
| C0, C1, V1, V2, V3 | Power supply | | |

Operational Description

The following explains the TMP87PP24A hardware configuration and operation. The configuration and functions of the TMP87PP24A are the same as those of the TMP87CM24A/CP24A, except in that a one-time PROM is used instead of an on-chip mask ROM.

The TMP87PP24A is placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. Operating Mode

The TMP87PP24A has two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST/VPP pin at low level.

In the MCU mode, operation is the same as with the TMP87CM24A/CP24A (the TEST/VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The TMP87PP24A has a 48K × 8-bit (addresses 4000_H to FFFF_H in the MCU mode, addresses 14000_H to 1FFFF_H in the PROM mode) of program memory (OTP).

When the TMP87PP24A is used as a system evaluation of the TMP87CM24A/CP24A, the data is written to the program storage area show in Figure 1-1.

Note : Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

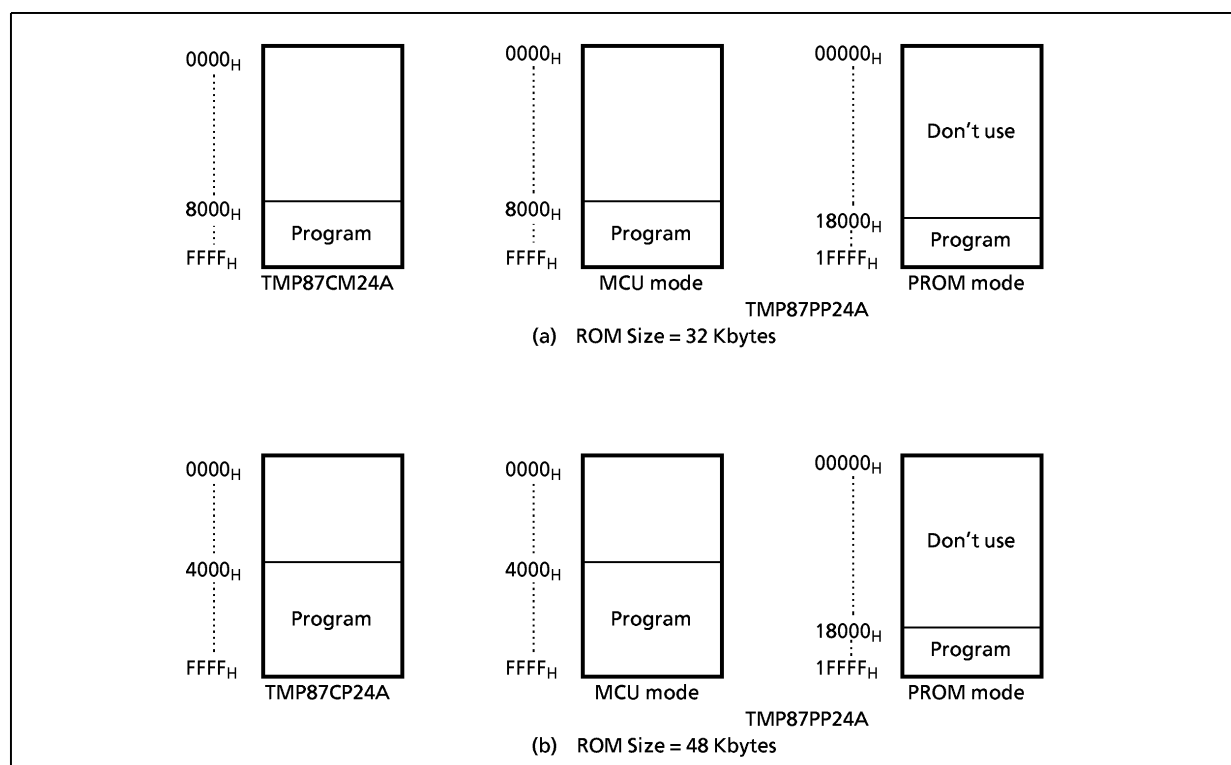


Figure 1-1. Program Memory Area

1.1.2 Data Memory

The TMP87PP24A has an on-chip 2K × 8-bit data memory (static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the TMP87PP24A are the same as those of the TMP87CM24A/CP24A except that the TEST pin has no built-in pull-down resistance.

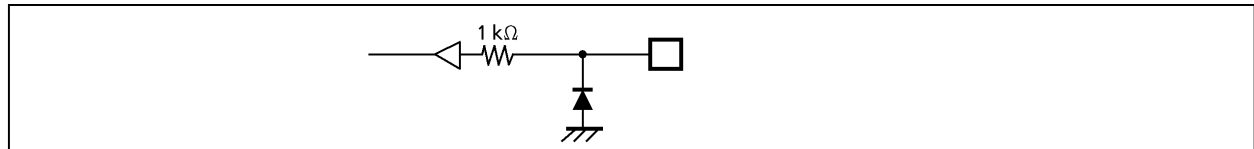


Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuits of TMP87PP24A I/O ports are the same as those of TMP87CM24A/CP24A.

1.2 PROM Mode

The PROM mode is activated by setting the TEST, $\overline{\text{RESET}}$ pin and the ports P17 to P10, P22 to P20 and P61 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

Note: The high-speed programming mode can be used for program operation.

The TMP87PP24A is not supported an electric signature mode, so the ROM type must be set to TC571000D.

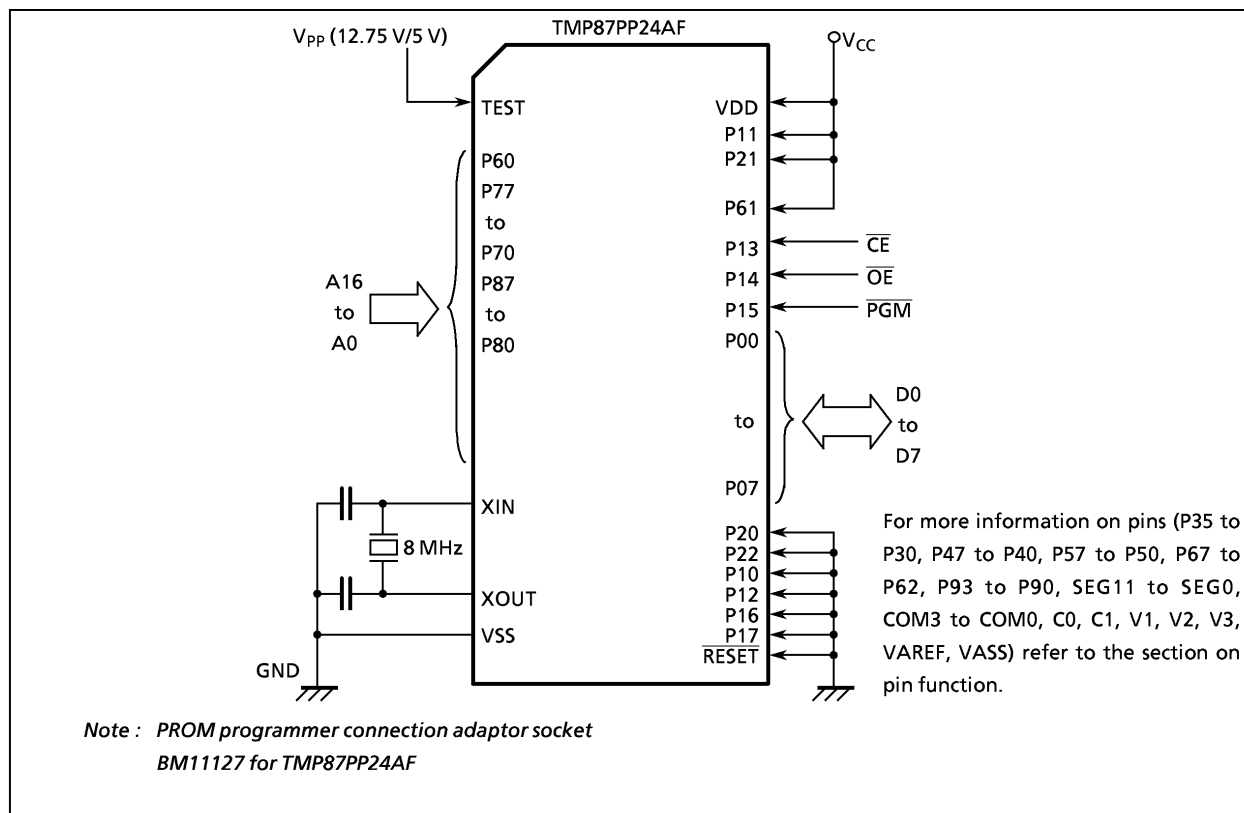


Figure 1-3. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed Programming Mode)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the VPP pin when $V_{CC} = 6.25$ V. After the address and input data are stable, the data is programmed by applying a single 0.1 ms program pulse to the \overline{PGM} input. The programmed data is verified. If incorrect, another 0.1 ms program pulse is applied. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5$ V.

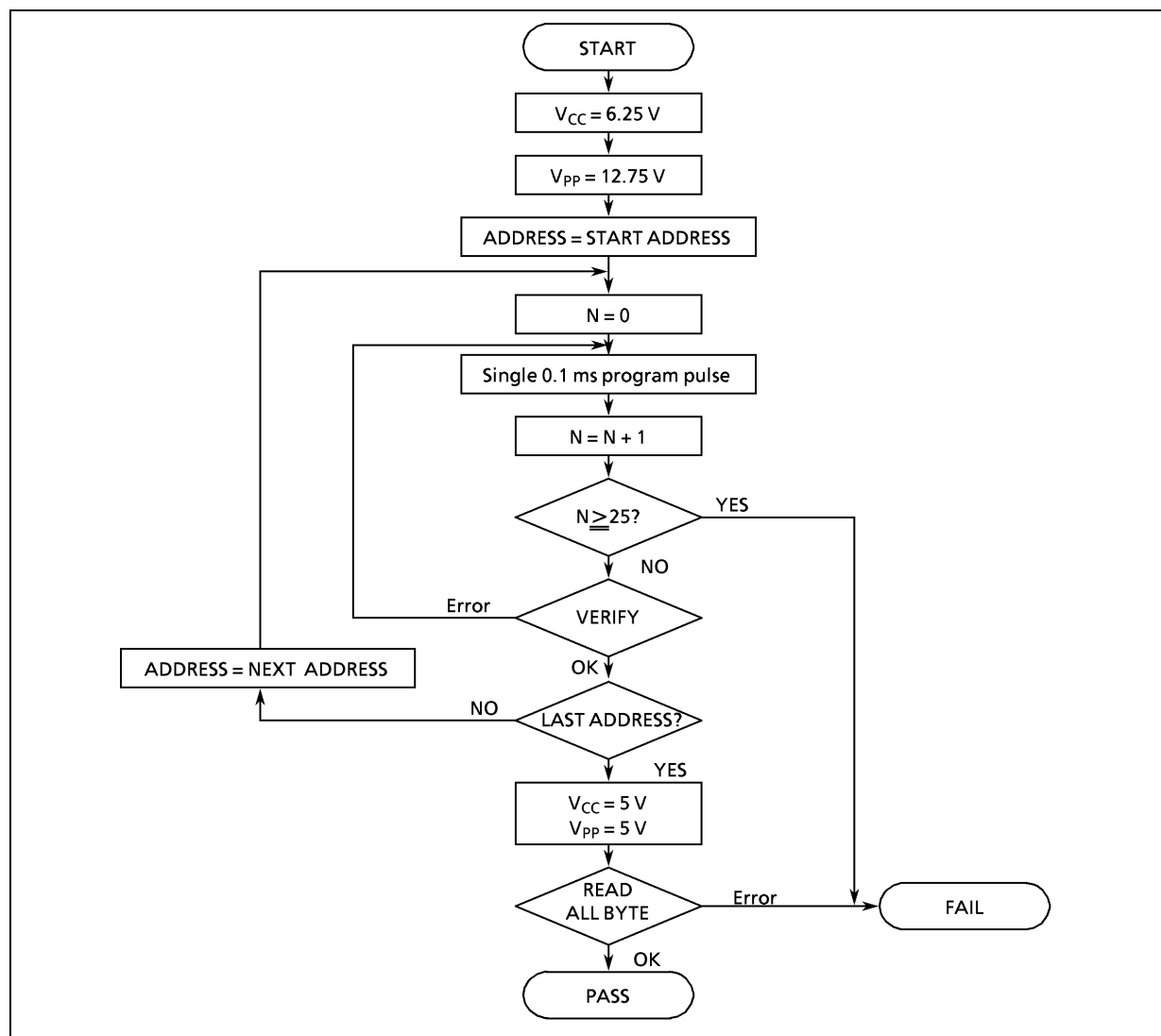


Figure 1-4. Flow Chart of High-speed Programming

1.2.2 Writing Method for General-purpose PROM Program

- (1) Adapters
BM11127 : TMP87PP24AF
- (2) Adapter setting
Switch (SW1) is set to side N.
- (3) PROM programmer specifying
 - i) PROM type is specified to TC571000D.
Writing voltage: 12.75 V (high-speed program mode)
 - ii) Data transfer (copy) (note 1)
In the TMP87PP24A, EPROM is within the addresses 14000_H to 1FFFF_H. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.
ROM capacity of 48KB : transferred addresses 04000_H to 0FFFF_H to addresses 14000 to 1FFFF_H
 - iii) Writing address is specified. (Note 1)
Start address : 14000_H
End address : 1FFFF_H
- (4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1 : The specifying method is referred to the PROM programmer description. Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

Note 2 : When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.

Note 3 : The TMP87PP24A does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12V ± 0.5V to the address pin 9 (A9). The signature must not be used.

Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

| Parameter | Symbol | Pins | Ratings | Unit |
|---------------------------------|---------------------|---|--------------------------------|------|
| Supply Voltage | V _{DD} | | – 0.3 to 6.5 | V |
| Program Voltage | V _{PP} | TEST/V _{PP} | – 0.3 to 13.0 | |
| Input Voltage | V _{IN} | | – 0.3 to V _{DD} + 0.3 | |
| Output Voltage | V _{OUT1} | Except P20 and P3 ports | – 0.3 to V _{DD} + 0.3 | |
| | V _{OUT2} | Ports P20, P3 | – 0.3 to 5.5 | |
| Output Current (Per 1 pin) | I _{OUT1} | Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41) | 3.2 | mA |
| | I _{OUT2} | P41 | 30 | |
| Output Current (Total) | Σ I _{OUT1} | Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41) | 120 | |
| | Σ I _{OUT2} | P41 | 30 | |
| Power Dissipation [Topr = 70°C] | PD | | 350 | mW |
| Soldering Temperature (time) | Tsld | | 260 (10 s) | °C |
| Storage Temperature | Tstg | | – 55 to 125 | |
| Operating Temperature | Topr | | – 10 to 70 | |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

(V_{SS} = 0V, Topr = – 10 to 70°C)

| Parameter | Symbol | Pins | Conditions | | Min | Max | Unit |
|--------------------|------------------|-------------------------|--------------------------------|------------------------|------------------------|------------------------|------|
| Supply Voltage | V _{DD} | | f _c = 8 MHz | NORMAL1, 2 mode | 4.5 | 5.5 | V |
| | | | | IDLE1, 2 mode | | | |
| | | | f _c = 4.2 MHz | NORMAL1, 2 mode | 2.2 | | |
| | | | | IDLE1, 2 mode | | | |
| | | | f _s = 32.768 kHz | SLOW mode | | | |
| | | | | SLEEP mode | | | |
| | STOP mode | 2.0 | | | | | |
| Input High Voltage | V _{IH1} | Except hysteresis input | V _{DD} ≥ 4.5 V | | V _{DD} × 0.70 | V _{DD} | |
| | V _{IH2} | Hysteresis input | | | V _{DD} × 0.75 | | |
| | V _{IH3} | | V _{DD} < 4.5 V | V _{DD} × 0.90 | | | |
| Input Low Voltage | V _{IL1} | Except hysteresis input | V _{DD} ≥ 4.5 V | | 0 | V _{DD} × 0.30 | |
| | V _{IL2} | Hysteresis input | | | | V _{DD} × 0.25 | |
| | V _{IL3} | | V _{DD} < 4.5 V | V _{DD} × 0.10 | | | |
| Clock Frequency | f _c | XIN, XOUT | V _{DD} = 4.5 to 5.5 V | | 0.4 | 8.0 | MHz |
| | | | V _{DD} = 2.2 to 5.5 V | | | 4.2 | |
| | f _s | XTIN, XTOUT | | | 30.0 | 34.0 | kHz |

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL1/2 mode and IDLE1/2 mode.

DC Characteristics

(V_{SS} = 0 V, T_{opr} = – 10 to 70°C)

| Parameter | Symbol | Pins | Conditions | Min | Typ. | Max | Unit |
|------------------------------------|-------------------|--------------------------------------|--|-----------------------|------|------|------|
| Hysteresis Voltage | V _{HS} | Hysteresis inputs | | — | 0.9 | — | V |
| Input Current | I _{IN1} | TEST | V _{DD} = 5.5 V, V _{IN} = 5.5 V/0 V | — | — | ± 2 | μA |
| | I _{IN2} | Open drain ports and tri-state ports | | | | | |
| | I _{IN3} | RESET, STOP | | | | | |
| Input Resistance | R _{IN2} | RESET | | 100 | 220 | 450 | kΩ |
| Output Leakage Current | I _{LO1} | Open drain ports | V _{DD} = 5.5 V, V _{OUT} = 5.5 V | — | — | 2 | μA |
| | I _{LO2} | Tri-state ports | V _{OUT} = 5.5 V/0 V | — | — | ± 2 | |
| Segment/Common Output Voltage | V _{LCD1} | SEG39 to SEG0 and COM3 to COM0 | | 0.75 | 1.0 | 1.33 | V |
| | V _{LCD2} | | | V _{LCD1} × 2 | | | |
| | V _{LCD3} | | | V _{LCD1} × 3 | | | |
| Output High Voltage | V _{OH1} | Push-pull ports (P4 port) | V _{DD} = 4.5 V, I _{OH} = – 200 μA | 2.4 | — | — | |
| | V _{OH2} | Tri-state ports (P0, P1, P5 ports) | V _{DD} = 4.5 V, I _{OH} = – 0.7 mA | 4.1 | — | — | |
| Output Low Voltage | V _{OL} | Except XOUT and P41 | V _{DD} = 4.5 V, I _{OL} = 1.6 mA | — | — | 0.4 | |
| Output Low Current | I _{OL3} | P41 | V _{DD} = 4.5 V, V _{OL} = 1.0 V | — | 20 | — | mA |
| Supply Current in NORMAL 1, 2 mode | I _{DD} | | V _{DD} = 5.5 V f _c = 8 MHz f _s = 32.768 kHz V _{IN} = 5.3 V/0.2 V | — | 12 | 18 | |
| Supply Current in IDLE 1, 2 mode | | | | — | 6 | 10 | |
| Supply Current in SLOW mode | | | V _{DD} = 3.0 V f _s = 32.768 kHz V _{IN} = 2.8 V/0.2 V Voltage boost frequency = 1 kHz | — | 31 | 70 | μA |
| Supply Current in SLEEP mode | | | | — | 16 | 40 | |
| Supply Current in STOP mode | | | V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V | — | 0.5 | 10 | |

Note 1: Typical values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input Current ; The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} ; Except for I_{REF}

Note 4: V_{LCD2} indicates an output voltage at the 2/3 level when operating in the 1/4 or 1/3 duty mode.

Note 5: V_{LCD1} indicates an output voltage at the 1/3 level when operating in the 1/4 or 1/3 duty mode.

AD Conversion Characteristics (I)

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, T_{opr} = – 10 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|--------------------------|-------------------|--|------------------|------|-------------------|------|
| Analog Reference Voltage | V _{AREF} | | 2.7 | – | V _{DD} | V |
| | V _{ASS} | | V _{SS} | – | 1.5 | |
| Analog Input Voltage | V _{AIN} | | V _{ASS} | – | V _{AREF} | |
| Analog Supply Current | I _{REF} | V _{AREF} = 5.5 V, V _{ASS} = 0.0 V | – | 0.5 | 1.0 | mA |
| Nonlinearity Error | | V _{DD} = 5.0 V, V _{SS} = 0.0 V V _{AREF} = 5.000 V V _{ASS} = 0.000 V or V _{DD} = 2.7 V, V _{SS} = 0.0 V V _{AREF} = 2.700 V V _{ASS} = 0.000 V | – | – | ± 1 | LSB |
| Zero Point Error | | | – | – | ± 1 | |
| Full Scale Error | | | – | – | ± 1 | |
| Total Error | | | – | – | ± 2 | |

Note: Quantizing error is not contained in those errors.

AD Conversion Characteristics (II)

(V_{SS} = 0V, V_{DD} = 2.2 to 2.7V, T_{opr} = – 10 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|--------------------------------|---------------------|---|------------------|------|-------------------|------|
| Analog Reference Voltage | V _{AREF} | | 2.2 | – | V _{DD} | V |
| | V _{ASS} | | V _{SS} | | | |
| Analog Reference Voltage Range | Δ V _{AREF} | | 2.2 | – | – | |
| Analog Input Voltage | V _{AIN} | | V _{ASS} | – | V _{AREF} | |
| Analog Supply Current | I _{REF} | V _{AREF} = 5.5 V, V _{ASS} = 0.0 V | – | 0.5 | 1.0 | mA |
| Nonlinearity Error | | V _{DD} = 2.2 V, V _{SS} = 0.0 V V _{AREF} = 2.200 V V _{ASS} = 0.000 V | – | – | ± 2 | LSB |
| Zero Point Error | | | – | – | ± 2 | |
| Full Scale Error | | | – | – | ± 2 | |
| Total Error | | | – | – | ± 4 | |

Note: Quantizing error is not contained in those errors.

AC Characteristics (I)

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 10 to 70°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|------------------------------|------------------|---|-------|------|-------|------|
| Machine Cycle Time | t _{cy} | In NORMAL 1, 2 mode | 0.95 | — | 10 | μs |
| | | In IDLE 1, 2 mode | | | | |
| | | In SLOW mode | 117.6 | — | 133.3 | |
| | | In SLEEP mode | | | | |
| High Level Clock Pulse Width | t _{WCH} | For external clock operation (XIN input), f _c = 8 MHz | 50 | — | — | ns |
| Low Level Clock Pulse Width | t _{WCL} | | | | | |
| High Level Clock Pulse Width | t _{WSH} | For external clock operation (XTIN input), f _s = 32.768 kHz | 14.7 | — | — | μs |
| Low Level Clock Pulse Width | t _{WSL} | | | | | |

AC Characteristics (II)

(V_{SS} = 0V, V_{DD} = 2.2 to 5.5V, T_{opr} = – 10 to 70°C)

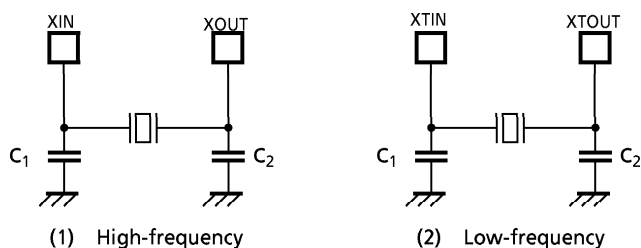
| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|------------------------------|------------------|--|-------|------|-------|------|
| Machine Cycle Time | t _{cy} | In NORMAL 1, 2 mode | 0.95 | — | 10 | μs |
| | | In IDLE 1, 2 mode | | | | |
| | | In SLOW mode | 117.6 | — | 133.3 | |
| | | In SLEEP mode | | | | |
| High Level Clock Pulse Width | t _{WCH} | For external clock operation (XIN input), f _c = 4.2 MHz | 110 | — | — | ns |
| Low Level Clock Pulse Width | t _{WCL} | | | | | |
| High Level Clock Pulse Width | t _{WSH} | For external clock operation (XTIN input), f _s = 32.768 kHz | 14.7 | — | — | μs |
| Low Level Clock Pulse Width | t _{WSL} | | | | | |

Recommended Oscillating Condition (I) ($V_{SS} = 0\text{ V}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$, $T_{opr} = -10\text{ to }70^{\circ}\text{C}$)

| Parameter | Oscillator | Frequency | Recommender Oscillator | Recommended Condition | |
|----------------|--------------------|------------|---|--------------------------|------------------|
| | | | | C ₁ | C ₂ |
| High-frequency | Ceramic Resonator | 8 MHz | KYOCERA KBR8.0M | 30pF | 30pF |
| | | | Standard/Lead Type (MURATA) CSA8.00MTZ CST8.00MTW | built-in 30pF | built-in 30pF |
| | | | Standard/SMP Type (MURATA) CSAC8.00MT | 30pF | 30pF |
| | | | Standard/Small ChipType (MURATA) CSTC8.00MT | built-in 30pF | built-in 30pF |
| | Crystal Oscillator | 4 MHz | KYOCERA KBR4.0MS | 30pF | 30pF |
| | | 8 MHz | TOYOCOM 210B 8.0000 | 20pF | 20pF |
| Low-frequency | Crystal Oscillator | 4 MHz | TOYOCOM 204B 4.0000 | | |
| | | 32.768 kHz | NDK MX-38T | 15pF | 15pF |

Recommended Oscillating Condition (II) ($V_{SS} = 0\text{ V}$, $V_{DD} = 2.2\text{ to }5.5\text{ V}$, $T_{opr} = -10\text{ to }70^{\circ}\text{C}$)

| Parameter | Oscillator | Frequency | Recommender Oscillator | Recommended Condition | |
|----------------|-------------------|-----------|--|--------------------------|------------------|
| | | | | C ₁ | C ₂ |
| High-frequency | Ceramic Resonator | 4 MHz | Standard/Lead Type (MURATA) CSA4.00MG | 30pF | 30pF |
| | | | CST4.00MGW | built-in 30pF | built-in 30pF |
| | | | Standard/SMD Type (MURATA) CSA4.00MGC CSAC4.00MGCM CSTC4.00MG | 30pF | 30pF |
| | | | | built-in 30pF | built-in 30pF |
| | | | Standard/Small Chip Type CSTCS4.00MG | built-in 10pF | built-in 10pF |



Note1: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

Note2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
<http://www.murata.co.jp/search/index.html>

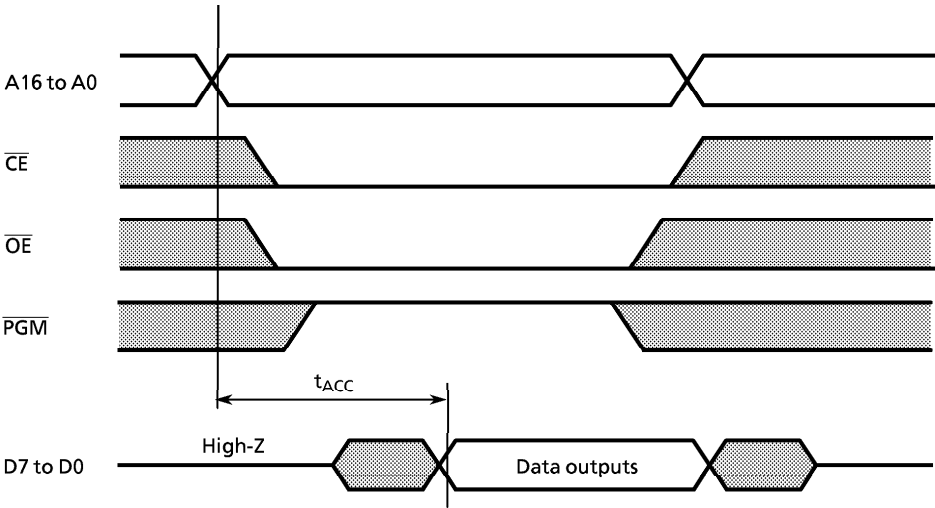
DC/AC Characteristics (PROM mode)

(V_{SS} = 0 V)

(1) Read Operation

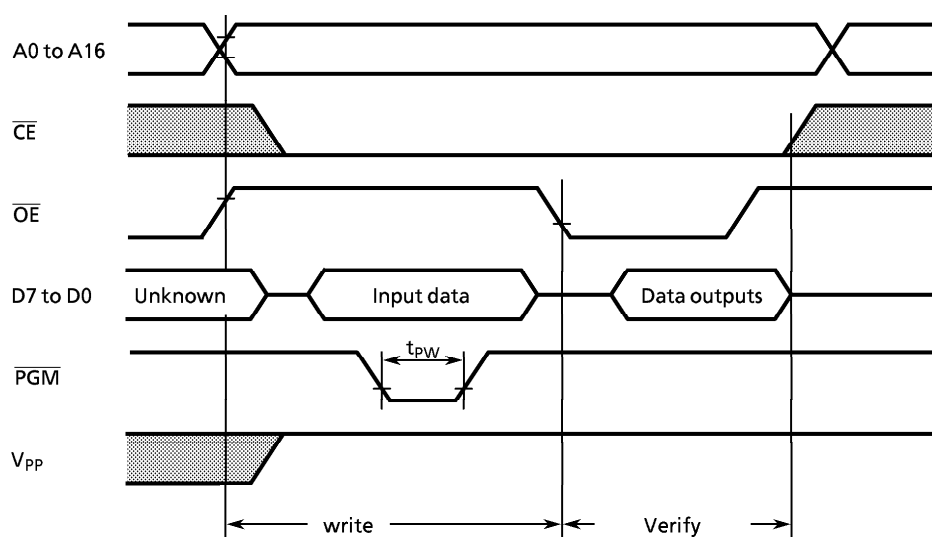
| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|------------------------------|------------------|-------------------------------|-----------------------|---------------------------|------------------------|------|
| Input High Voltage | V _{IH4} | | V _{CC} × 0.7 | — | V _{CC} | V |
| Input Low Voltage | V _{IL4} | | 0 | — | V _{CC} × 0.12 | |
| Power Supply Voltage | V _{CC} | | 4.75 | 5.0 | 5.25 | |
| Program Power Supply Voltage | V _{PP} | | | | | |
| Address Access Time | t _{ACC} | V _{CC} = 5.0 ± 0.25V | — | 1.5t _{cyc} + 300 | — | ns |

Note: t_{cyc} = 500 ns at 8 MHz



(2) High-Speed Programming Operation ($T_{opr} = 25 \pm 5^{\circ}\text{C}$)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|------------------------------|-----------|-------------------------|---------------------|-------|----------------------|------|
| Input High Voltage | V_{IH4} | | $V_{CC} \times 0.7$ | – | V_{CC} | V |
| Input Low Voltage | V_{IL4} | | 0 | – | $V_{CC} \times 0.12$ | |
| Power Supply Voltage | V_{CC} | | 6.0 | 6.25 | 6.5 | |
| Program Power Supply Voltage | V_{PP} | | 12.5 | 12.75 | 13.0 | |
| Initial Program Pulse Width | t_{PW} | $V_{CC} = 6.0\text{ V}$ | 0.095 | 0.1 | 0.105 | ms |



Note 1: When V_{CC} power supply is turned on or after, V_{pp} must be increased.

When V_{CC} power supply is turned off or before, V_{pp} must be increased.

Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage ($12.5\text{ V} \pm 0.5\text{ V} = V$) to the V_{pp} pin as the device is damaged.

Note 3: Be sure to execute the recommended programming mode with the recommended programming adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

