CMOS 8-Bit Microcontroller

TMP87CH34BN, TMP87CK34BN, TMP87CM34BN

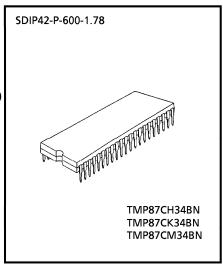
The 87CH34B/K34B/M34B is the high speed and high performance 8-bit single chip microcomputer. This MCU contains CPU core, ROM, RAM, input/output ports, six multi-function timer/counter, serial interface, on-screen display, PWM, 6-bit A/D conversion inputs and remote control signal processor on a chip.

The functions of the OSD circuit conform to the on-screen display functions of closed caption decoders based on FCC standards.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CH34BN	16 Kbytes			
TMP87CK34BN	24 Kbytes	1 Kbytes	SDIP42-P-600	TMP87PM34AN
TMP87CM34BN	32 Kbytes			

Features

- ◆8-bit single chip microcomputer TLCS-870 Series
- \blacklozenge Instruction execution time : 0.5 μ s (at 8 MHz)
- ◆412 basic instructions
 - Multiplication and Division (8 bits x 8 bits, 16 bits ÷ 8 bits)
 - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive Or)
 - 16-bit data operations
 - 1-byte jump/subroutine-call (Short relative jump / Vector call)
- ◆14 interrupt sources (External: 5, Internal: 9)
 - All sources have independent latches each, and nested interrupt control is available.
 - 4 edge-selectable external interrupts with noise reject
 - High-speed task switching by register bank changeover
- ◆Input/Output ports (33 pins)
 - High current output: 4pins (typ. 20 mA)
- ◆Two 16-bit Timer/Counters
- ◆Two 8-bit Timer/Counters
 - Timer, Event counter, Capture (Pulse width/duty measurement) modes
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
- **♦**Watchdog Timer
 - Interrupt source/reset output (programmable)



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- ◆Serial Interface
 - I²C-bus (Single master) / 8-bits SIO timeshared 2-ch
- ◆On-screen display circuit

Character patterns : 256 characters
 Character displayed : 32 column 8 lines

• Composition : 8 × 9 dots

• Size of character : 3kinds (line by line)

Color of character
 Variable display position
 Horizontal/Vertical 128/256 steps

- Fringing, Smoothing function
- Conform to US CLOSED CAPTION DECODER REGULATION
- **◆**PWM outputs
 - 14-bit PWM output (1 channel)
 - 7-bit PWM outputs (9 channels)
- ♦6-bit A/D conversion input (4 channels)
- ◆ Pulse output (Clock for PLL IC)
- ◆ Remote control signal processor
- ◆ Jitter elimination circuit
- ◆ Data slicer circuit
- ◆Two Power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port

output hold/high-impedance.

• IDLE mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.

◆Emulation Pod : BM87CM34AN0A

Pin Assignments (Top View) (PWM0) P40 ← 42 — VDD SDIP42-P-600-1.78 (PWM1) P41 ← 2 41 □ → P33 (TC4 / VIN0) (PWM2) P42 < 3 40 P32 (VIN1 / CSIN) (PWM3) P43 < 4 39 - vvss (PWM4) P44 ← →[5 38 □ → P35 (SI1 / SDA1) (PWM5) P45 ← → [6 □ → P34 (SCK1 / SCL1) 37 (PWM6) P46 ← → 7 36 □< > P31 (INT4 / TC3) (PWM7) P47 **← →**[8 35 □ → P30 (INT3 / RXIN) (SCK0 / SCL0 / INTO / PWM8) P50 ← 9 34 → P20 (INT5 / STOP) (SI0 / SDA0 / PWM9) P51 **← →** 10 33 □< → RESET (SO0 / TC2 / PULSE) P52 **← →** → XOUT 11 32 - XIN (INT2 / TC1) P53 < → 12 31 (CIN0) P54 < →[13 30 TEST (CIN1) P55 < →[29 □< > osc2 14 (CIN2) P56 < →[15 28 □<> osc1 (CIN3) P57 → □ 27 → P71 (VD) (Y/BLIN) P60 < 17 26 → P70 (HD) → P67 (Y / BL) (BIN) P61 < 18 25 (GIN/CSOUT) P62 ←→□ 19 24 P66 (B) I/O Ports (RIN/FIELD) P63 ← → 20 23 🗠 → P65 (G) P67 P71 VSS. 21 22 P64 (R) to P60 to P70 **Block Diagram** display Character Y/BLIN Y/BL memory ROM 먪 BIN, GIN, ★B,G,R Р6 Р7 RIN / FIELD (OCS1) Jitter € Eliminatio On-screen display circuit (OCS2) $\overline{\mathcal{M}}$ VDD Power Program Counter Р W Stack Pointer VSS S Data Memory Supply VVSS Flags RBS (RAM) Register Banks Reset I/O RESET System Controller Test pin TEST Interrupt Controller **Program Memory** (ROM) Standby Controller Serial Time Base 16-bit 8-bit **Timing Generator** Timer Timer/Counter Timer/Counter Interface TC1 TC2 TC3 TC4 SIO/I²Cbus Resonator XIN-Connecting \ XOUT◀ High Clock Watchdog Inst.Register Remote frequ. Generator Timer ntrol signa Inst. Decoder <u>不</u> Slicer 6-bit A/D P2 Р5 P4 Р3 PWM Converter VDR Slicer **A** CCLK Pulse CDATA P33 P47 P57 to P50 P20 P35 to P40 P30 Video signal I/O Ports

Pin Function

Pin Name	Input/Output	F	unction			
P20 (ĪNT5/STOP)	I/O (Input)	1-bit input / output port with latch. When used as an input port, or an interrupt input/STOP mode release signal input, the latch must be set to "1".	External intrrupt input 5 / STOP mode release signal input			
P35 (SI1/SDA1)	I/O (Input, I/O)		SIO1 serial data input/l ² Cbus2 serial data input/output			
P34 (SCK1/SCL1)	I/O (Input, I/O)	6-bit input/output port with latch.	SIO1 serial clock data input/l ² Cbus2 serial clock input/output			
P33 (TC4/VIN0)	I/O (Input, Input, Input)	When used as an input port, a serial interface input/output, a timer/counter	Timer/counter 4 input/Video signal input 0 Video signal input 1 /Composit sync input			
P32 (VIN1/CSIN)	I/O (Input, Input, Input)	input, a remote control signal processor input, data slicer input, or an intrrupt				
P31 (INT4/TC3)	I/O (Input, Input)	input, the latch must be set to "1".	External interrupt input 4/Timer/Counter 3 input			
P30 (INT3/RXIN)	I/O (Input, Input)		External intrrupt input 3 / remote control signal processor input			
P47 (PWM7) to P41 (PWM1)	I/O (Output)	8-bit programable input/output port (tri-state). Each bit of this port can be individually as an input or an output under software control. During reset,	7-bit PWM outputs			
P40 (PWM0)	(013613)	all bits are configured as inputs. When used as a PWM output, the latch must be set to "1".				
P57 (CIN3) to P54 (CIN0)	I/O (Input)	8-bit input/output port with latch. (P57~P54: tri-state)	Comparator inputs			
P53 (INT2 / TC1)	I/O (Input, Input)	Each bit of this port can be individually	External interrupt input 2/Timer/Counter 1 input			
P52 (SO0/TC2/PULSE)	I/O (Output, Input, Output)	as an input or an output under software control.	SIO1 serial data output/Timer/Counter 2 input/Pulse output			
P51 (PWM9/SI0/SDA0)	I/O (Output, Input, I/O)	When used as an input port, a PWM output, or a pluse output, the latch	7-bit PWM outputs/SIO1 serial data input /I ² Cbus 1 serial data input/output			
P50 (PWM8 / SCK0 / SCL0 / INTO)	I/O (Output, I/O, I/O, Input)	must be set to "1".	7-bit PWM outputs/SIO1 serial clock data input/l ² Cbus 1 serial clock input/output/External interrupt input 0			
OSC1, OSC2	Input, Output	Resonator connecting pin of on-screen display circuit				
P71 (VD)		2-bit input/output port with latch. When used as an input port, a vertical synchronous signal input,	Vertical synchronous signal input			
P70 (HD)	I/O (Input)	or a horizontal sychronous signal input, the latch must be set to "1".	Horizontal synchronous signal input			
P67 (Y/BL) P66 (B) P65 (G) P64 (R)	I/O (Output)	8-bit programable input/output port (P67 to P64: tri-state, P63 to P60: High current output). Each bit of this port can be individually as an input or an output under software control. During reset, all bits are configured as inputs.	R, G, B, Y/BL output			
P63 (RIN/FIELD) P62 (GIN/CSOUT) P61 (BIN) P60 (Y/BLIN)	1/0	When P67 to P64 ports are used as output port, bits 7 to 4 of address 0F91 _H must be set to "1". When P63 to P60 port used as RIN, GIN, BIN, Y/BLIN input, these ports must be set to "1".	R input/Field status input G input/Test video signal output B input Y/BL input			
XIN, XOUT	Input, Output	Resonator connecting pin (High frequency). For exte	ernal clock input, XIN is used and XOUT is opened.			
RESET	1/0	Reset signal input or watchdog timer output/address				
TEST	Input	Test pin for out-going test. Be tied to low.				
VDD, VSS, VVSS	Power Supply	+5 V, 0 V (GND)				

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87CH34B/K34B/M34B. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR / DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

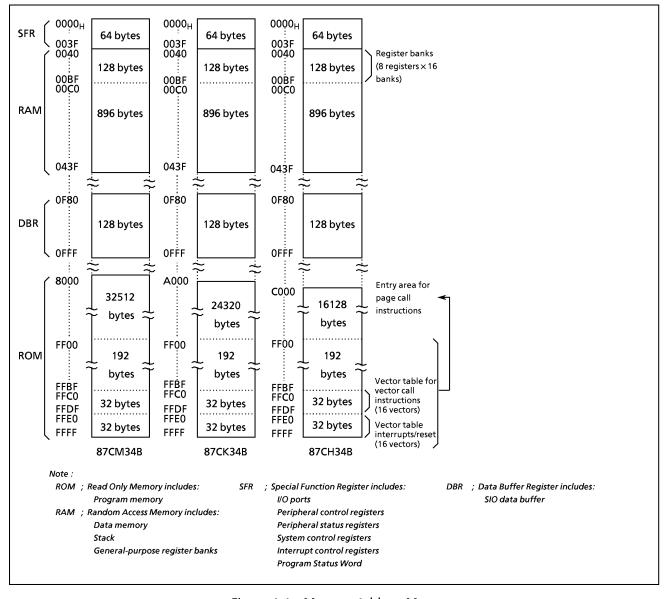


Figure 1-1. Memory Address Map

Electrical Characteristics

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$

Parameter	Symbol	Condition	Ratings	Unit	
Supply Voltage	V_{DD}		- 0.3 to 6.5	V	
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	V	
Output Voltage	V _{OUT1}		- 0.3 to V _{DD} + 0.3	V	
0.15.16	I _{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	3.2	4	
Output Current (Per 1 pin)	I _{OUT2}	Ports P60 to P63	30	mA	
0 1 16 17 18	Σl _{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	120		
Output Current (Total)	Σl _{OUT2}	Ports P60 to P63	120	mA	
Power Dissipation [Topr = 70°C]	PD		600	mW	
Soldering Temperature (time)	Tsld		260 (10 s)	°C	
Storage Temperature	Tstg		– 55 to 125	°C	
Operating Temperature	Topr		- 30 to 70	°C	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}	$V_{DD} \begin{tabular}{ll} f_C = & NORMAL mode \\ 8 \ MHz & IDLE mode \\ \end{tabular}$		IDLE mode	4.5	5.5	V
				STOP mode	2.0		
	V _{IH1}	Except hysteresis input					
Input High Voltage	V _{IH2}	Hysteresis input	,	V _{DD} ≥ 4.5 V	$V_{DD} \times 0.75$	V _{DD}	V
	V _{IH3}		V _{DD} < 4.5 V		$V_{DD} \times 0.90$		
	V _{IL1}	Except hysteresis input	$V_{DD} \ge 4.5 V$ $V_{DD} < 4.5 V$		0	V _{DD} × 0.30	
Input Low Voltage	V_{IL2}	Hysteresis input				V _{DD} × 0.25	V
	V _{IL3}					V _{DD} × 0.10	
	fc	XIN, XOUT	V _{DI}	_D = 4.5 to 5.5 V	4.0	8.0	
Clock Frequency				requency mode I, V _{DD} = 4.5 to 5.5 V)	2.0	$f_{OSC} \le fc \times 1.4 \le 6.0$	MHz
	f _{OSC} OSC1, OSC2		Normal freguency mode (FORS = 0, V_{DD} = 4.5 to 5.5 V) 4.0 $f_{OSC} \le fc \times f_{OSC}$		$f_{OSC} \le fc \times 2.8 \le 12.0$		

Note1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note2 : Clock Frequency fc ; The condition of supply voltage range is the value in NORMAL and IDLE mode.

Note3: When using test video signal circuit and data slicer circuit, high frequency must be 8 MHz.

D.C. Characteristics

 $(V_{SS} = 0 \text{ V}, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis inputs		-	0.9	-	V
	I _{IN1}	TEST	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V} / 0 \text{ V}$	_	_	± 2	
Innest Comment	I _{IN2}	Open drain ports	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	_	-	2	,
Input Current	I _{IN3}	Tri-state ports	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V} / 0 \text{ V}$ -		-	± 2	μΑ
	I _{IN4}	RESET, STOP	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V} / 0 \text{ V}$	_	_	± 2	
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
Output Leakage Current	I _{LO1}	Sink open drain ports	$V_{DD} = 5.5 \text{ V}, \ V_{OUT} = 5.5 \text{ V}$	-	-	2	_
	I _{LO2}	Tri-state ports	$V_{DD} = 5.5 \text{ V}, \ V_{OUT} = 5.5 \text{ V} / 0 \text{ V}$	-	-	± 2	μΑ
Output High Voltage	V _{OH2}	Tri- state port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	_	V
Output Low Voltage	V _{OL}	Except XOUT, OSC2 and ports P60 to P63	$V_{DD} = 4.5 \text{ V}, \ \ I_{OL} = 1.6 \text{ mA}$	-	-	0.4	٧
Output Low Current	I _{OL3}	Ports P60 to P63	$V_{DD} = 4.5 \text{ V}, \ V_{OL} = 1.0 \text{ V}$	-	20	_	mA
Supply Current in NORMAL mode			V _{DD} = 5.5 V fc = 8 MHz	-	15	25	mA
Supply Current in IDLE mode	I _{DD}		$V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$	-	10	18	mA
Supply Current in STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3 V / 0.2 V	_	0.5	10	μΑ

Note 1 : Typical values show those at $T_{opr} = 25$ °C , $V_{DD} = 5$ V.

Note 2 : Input Current $I_{IN1}\,I_{IN4}$; The current through pull-up or pull-down resistor is not included.

Note 3: Typical current consumption during A/D conversion is 1.2 mA.

A/D Conversion Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Analog Input Voltage Range	V_{AIN}	CIN3 to CIN0		V_{SS}	-	V_{DD}	٧
Conversion Error			V _{DD} = 5.0 V	-	_	± 1.5	LSB

A.C. Characteristics

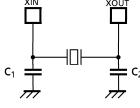
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$

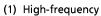
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Machine Cuele Time	tcy	In NORMAL mode	0.5	ı	1.0	
Machine Cycle Time	tcy	In IDLE mode	0.3			μS
High-Level Clock Pulse Width	t _{WCH}	For external clock operation	62.5	_	_	
Low-Level Clock Pulse Width	t_{WCL}	(XIN input) , fc = 8 MHz	02.3			ns

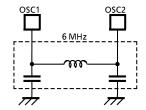
Recommended Oscillating Condition

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$$

Parameter	.	Frequency	Recommended	Recommended Conditions		
	Oscillator		Oscillator	C ₁	C ₂	
	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	30 pF	30 pF	
	Ceramic Resonator	4.044-	KYOCERA KBR4.0MS	30 pi	30 pi	
High-frequency		4 MHz	MURATA CSA4.00MG			
Oscillation	Crystal Oscillator	8 MHz	TOYOCOM 210B 8.0000			
		4 MHz	TOYOCOM 204B 4.0000	20 pF	20 pF	
OSD	LC Resonator	6 MHz	TOKO A285HCIS-13319			
		12 MHz	TOKO TA285HCIS-13306	_	_	







(2) LC Resonator for OSD

Note: On our OSD circuit, the horizontal display start position is determined by counting the clock from LC oscillator. So, the unstable start of oscillation after the rising edge of Horizontal Sync. Signal will be cause the OSD distortion.

Generally, smaller C and larger L make clearer wave from at the beginning of oscillation. We recommend that the value of LC oscillator should be equal and digger than 33 μ H.

Note: To keep reliable operation, shield the device electrically with the metal plate on its package mold surface against the high electric field, for example, by CRT (Cathode Ray Tube).