CMOS 8-Bit Microcontroller

TMP87CH29U/N, TMP87CK29U/N, TMP87CM29U/N

The 87CH29/K29/M29 are high-speed and high-performance 8-bit single chip microcomputers. These MCU contains CPU core, ROM, RAM, a LCD driver, multi-function timer/counters, an A/D converter, two clock generators and a serial interface (UART) on a chip.

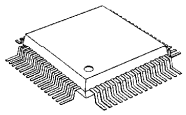
Part No.	ROM	RAM	Package	OTP MCU
TMP87CH29U	16 K × 8-bit	1 K × 8-bit	P-LQFP64-1010-0.50	TMP87PM29U
TMP87CH29N			P-SDIP64-750-1.78	* TMP87PM29N
TMP87CK29U	24 K × 8-bit		P-LQFP64-1010-0.50	TMP87PM29U
TMP87CK29N			P-SDIP64-750-1.78	* TMP87PM29N
TMP87CM29U	32 K × 8-bit		P-LQFP64-1010-0.50	TMP87PM29U
TMP87CM29N			P-SDIP64-750-1.78	* TMP87PM29N

* ; Under development

Features

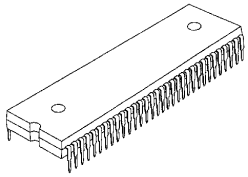
- ◆8-bit single chip microcomputer TLCS-870 Series
- ◆Instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
- ◆412 basic instructions
  - Multiplication and Division (8 bits × 8 bits, 16 bits ÷ 8 bits)
  - Bit manipulations (set/clear/complement/move/test /exclusive or)
  - 16-bit data operations
  - 1-byte jump/subroutine-call (Short relative jump / Vector call)
- ◆13 interrupt sources (External: 4, Internal: 9)
  - All sources have independent latches each, and nested interrupt control is available.
  - 2 edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆7 Input/Output ports (43 pins)
  - High current output: 3 pins (typ. 20 mA)
- ◆18-bit Timer/Counter
  - Timer, Event counter, Pulse width measurement, Frequency measurement modes
- ◆Four 8-bit Timer/Counters
  - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16384 Hz)
- ◆Divider output function (frequency: 1 kHz to 8 kHz)
- ◆Watchdog Timer
  - Interrupt source / reset output (programmable)
- ◆Universal asynchronous receiver and transmitter (UART)
  - With 8 bit transmit/receive data buffer
  - Transfer clock, Select of with/without parity bit.
- ◆LCD driver/Controller
  - LCD direct drive capability (max. 12-digit display at 1/4 duty LCD).
  - 1/4, 1/3, 1/2 duties or static drive are programmably selectable.
  - With display memory.

P-LQFP64-1010-0.50



TMP87CH29U
TMP87CK29U
TMP87CM29U
TMP87PM29U

P-SDIP64-750-1.78



TMP87CH29N
TMP87CK29N
TMP87CM29N
TMP87PM29N

980910EBP2

◆Dual clock operation
- Single/Dual-clock mode (option)

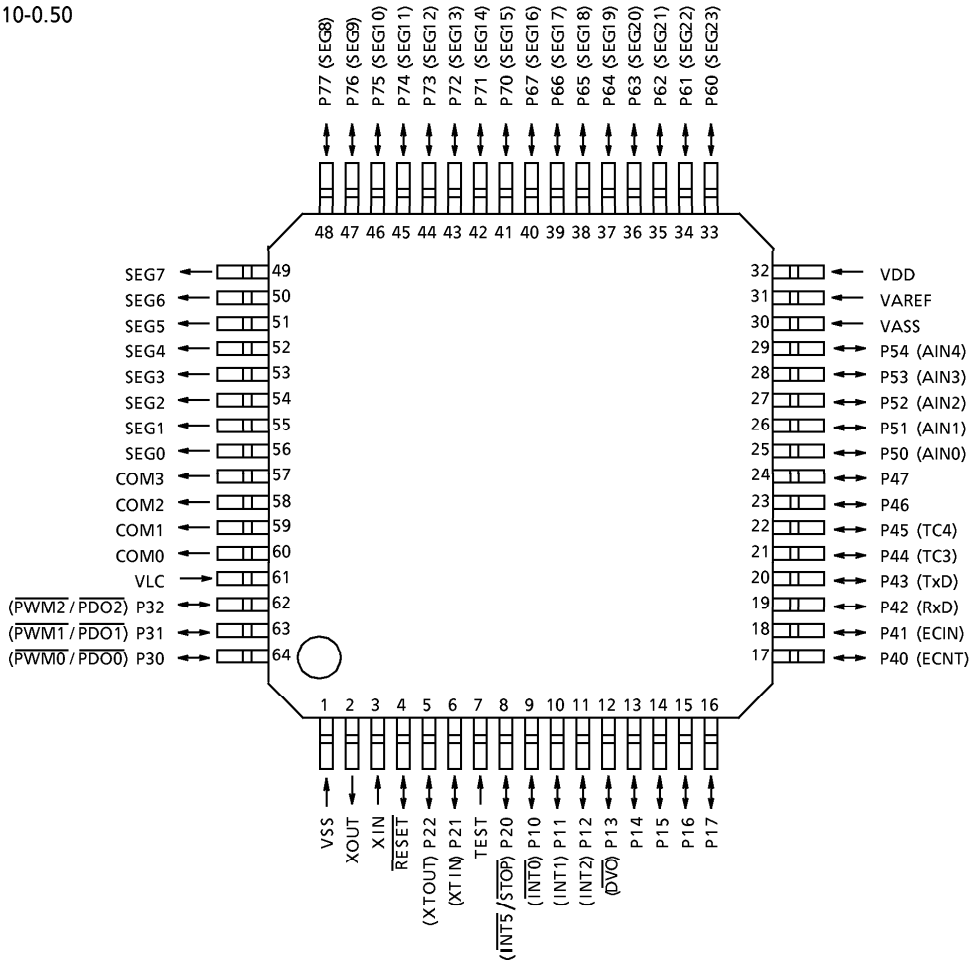
◆Five power saving operating modes
- STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
- SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
- IDLE1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
- IDLE2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- SLEEP mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.

◆Wide operating voltage: 2.7 to 5.5V at 4.19 MHz / 32.768 kHz, 4.5 to 5.5 V at 8 MHz / 32.768 kHz

◆Emulation Pod: BM87CM29U0A

Pin Assignments (Top View)

P-LQFP64-1010-0.50



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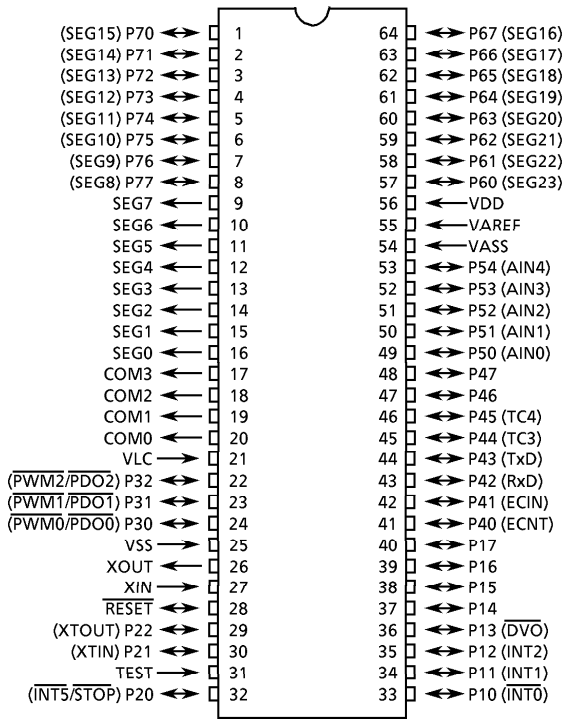
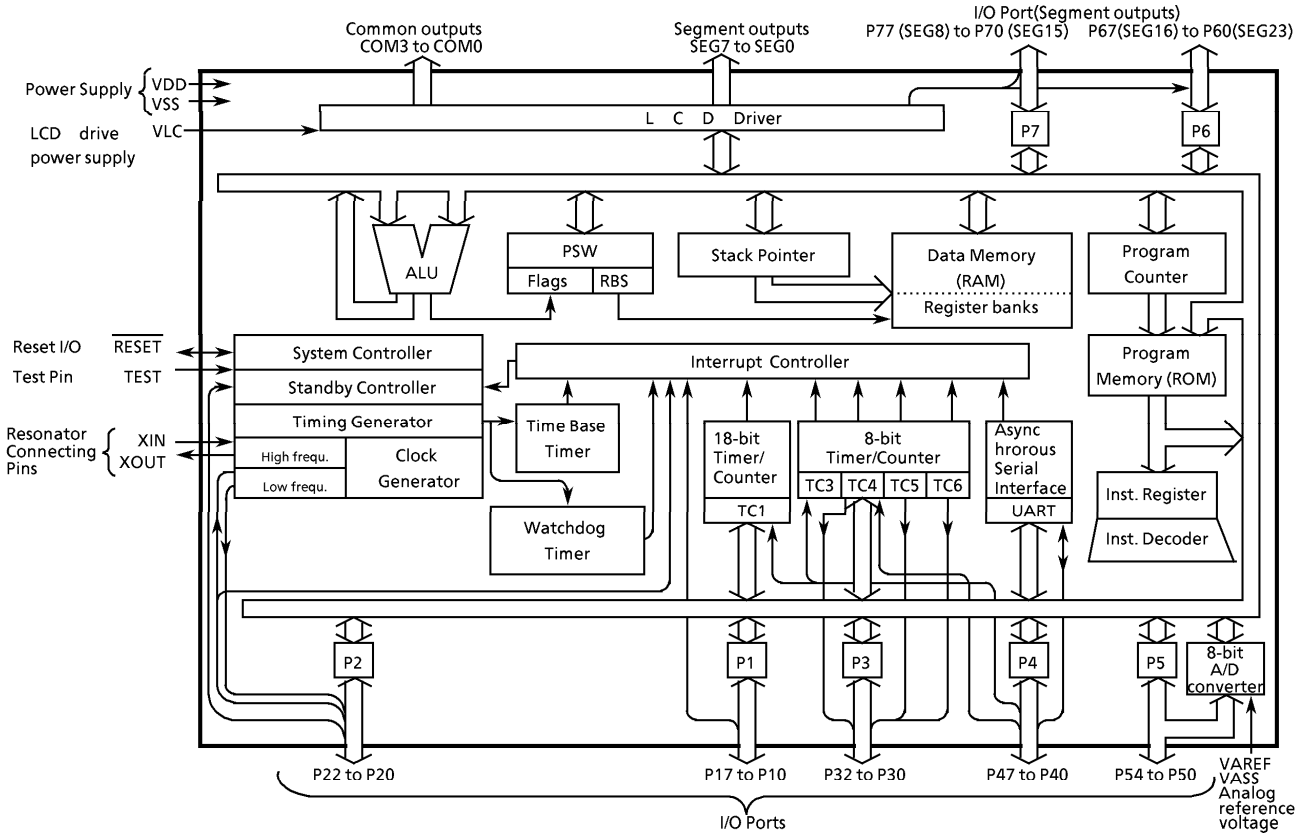


Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P17 to P14	I/O	8-bit programmable input/output ports (tri-state) . Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a divider output, the latch must be set to "1".	
P13 ($\overline{DVO}$)	I/O (Output)		Divider output
P12 (INT2)	I/O (Input)		External interrupt input 2
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the latch must be set to "1".	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$/$\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P32 ($\overline{PWM2}$ / $\overline{PDO2}$)	I/O (Output)	3-bit input/output port (high current output) with latch. When used as an input port, a PWM output, or a PDO output, the latch must be set to "1".	8-bit $\overline{PWM2}$ output or 8-bit $\overline{PDO2}$ output
P31 ($\overline{PWM1}$ / $\overline{PDO1}$)			8-bit $\overline{PWM1}$ output or 8-bit $\overline{PDO1}$ output
P30 ($\overline{PWM0}$ / $\overline{PDO0}$)			8-bit $\overline{PWM0}$ output or 8-bit $\overline{PDO0}$ output
P47	I/O	8-bit input/output port with latch. Each bit of these ports can be individually configured as a sink open drain or a push-pull output under software control. During reset, all bits are configured as sink open drain outputs. When used as an input port, a timer/counter input, a PWM output, a PDO output, or a UART input/output, the latch must be set to "1".	
P46			
P45 (TC4)	I/O (Input)		Timer / Counter 4 input
P44 (TC3)			Timer / Counter 3 input
P43 (TxD)	I/O (Output)		UART data output
P42 (RxD)	I/O (Input)		UART data input
P41 (ECIN)			Timer / Counter 1 inputs
P40 (ECNT)			
P54 (AIN4)	I/O (Input)	5-bit programmble input/output ports (tri-state) . Each bit of these ports can be individually configured as an input or an output under software control.	A/D converter analog inputs
P53 (AIN3)			
P52 (AIN2)			
P51 (AIN1)			
P50 (AIN0)			
P67 (SEG16) to P60 (SEG23)	I/O (Output)	8-bit input/output port with latch. When used as an input port, the latch must be set to "1".	LCD Segment outputs. When used as a segment output, the P6 control register (P6CR) must be set to "1".
P77 (SEG8) to P70 (SEG15)	I/O (Output)	8-bit input/output port with latch. When used as an input port, the latch must be set to "1".	LCD Segment outputs. When used as a segment output, the P7 control register (P7CR) must be set to "1".
SEG7 to SEG0	Output	LCD Segment outputs	
COM3 to COM0		LCD Common outputs	
XIN , XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VAREF, VASS		Analog reference voltage inputs (High, Low)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87CH29/K29/M29.

In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

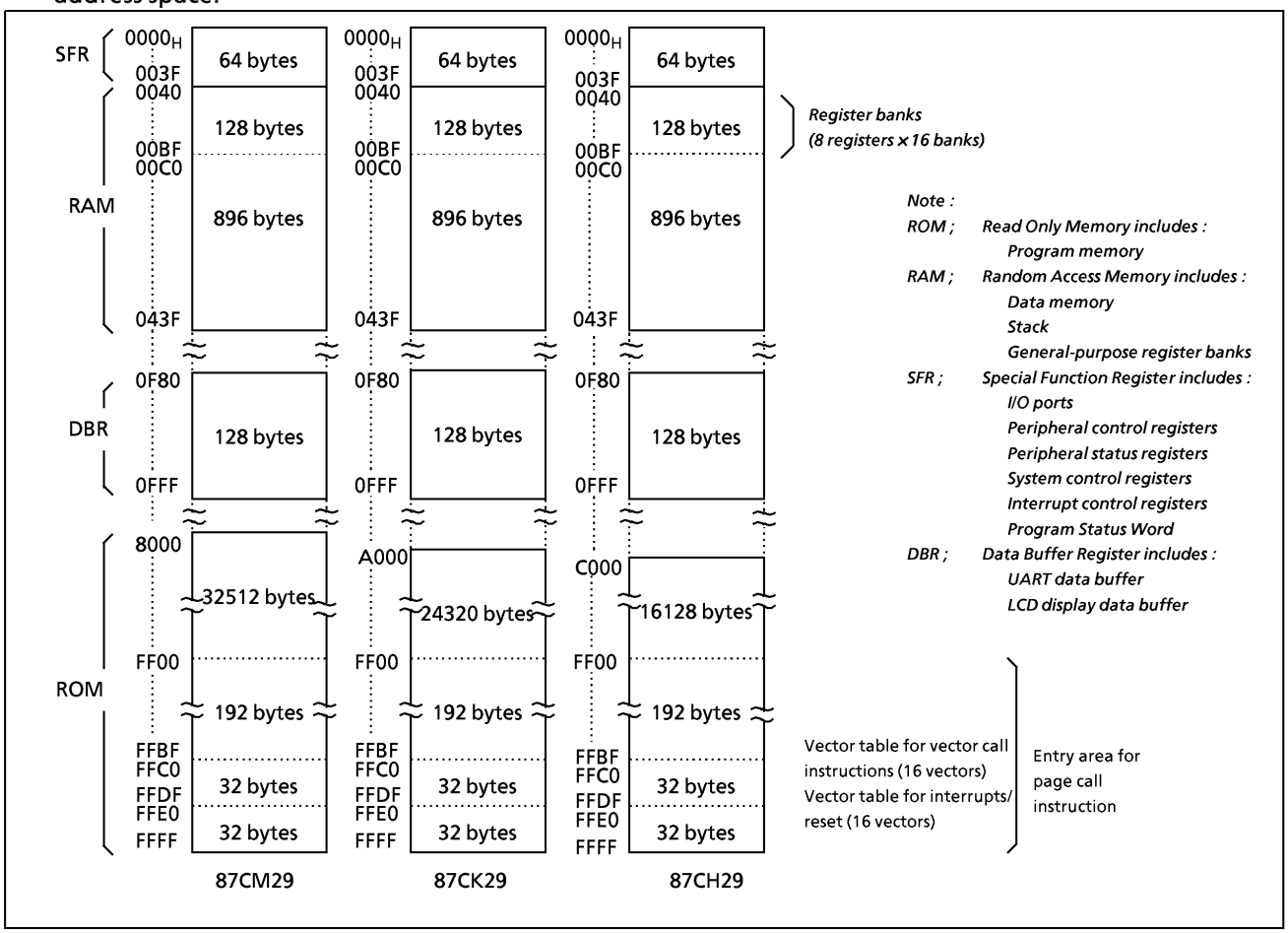


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The 87CH29 has a 16K × 8-bit (addresses $C000_H$-$FFFF_H$), the 87CK29 has a 24K × 8-bit (addresses $A000_H$-$FFFF_H$), and the 87CM29 has a 32K × 8-bit (addresses 8000_H-$FFFF_H$) of program memory (mask programmed ROM).

Addresses $FF00_H$-$FFFF_H$ in the program memory can also be used for special purposes.

(1) **Interrupt/Reset** vector table (addresses $FFE0_H$-$FFFF_H$)

This table consists of a reset vector and 16 interrupt vectors (2 bytes/vector). These vectors store a reset start address and interrupt service routine entry addresses.

Electrical Characteristics

(1) 87CH29/K29/M29

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	P21, P22, $\overline{RESET}$, Tri-state port, and Push-pull port	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	P20, Port P3 and Segment port	– 0.3 to 5.5	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2, P4, P5, P6, P7	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2, P4, P5, P6, P7	120	mA
	ΣI_{OUT2}	Port P3	60	
Power Dissipation [Topr = 70°C]	PD	TMP87CH29N/CK29N/CM29N	600	mW
		TMP87CH29U/CK29U/CM29U	350	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc ; The supply voltage range of the conditions shows the value in NORMAL 1, 2 modes and IDLE 1, 2 modes.

D.C.Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			—	0.9	—	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V		—	—	± 2	μA
	I_{IN2}	Sink open drain port and tri-state port						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input Low Current	I_{IL}	Push-pull port	V_{DD} = 5.5 V, V_{IN} = 0.4 V		—	—	– 2	mA
Input Resistance	R_{IN}	$\overline{RESET}$			100	220	450	kΩ
Output Leakage Current	I_{LO}	Sink open drain port and tri-state port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		—	—	2	μA
Output High Voltage	V_{OH1}	Push-pull port	V_{DD} = 4.5 V, I_{OH} = – 200 μA		2.4	—	—	V
	Vo_{H2}	Tri- state port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA		4.1	—	—	
Output Low Voltage	V_{OL}	Except XOUT and port P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		—	—	0.4	V
Output Low Current	I_{OL}	Only P30, P31, P32	V_{DD} = 4.5 V, V_{OL} = 1.0 V		—	20	—	mA
Supply Current in NORMAL 1 , 2 mode	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3 V / 0.2 V		—	10	16	mA
Supply Current in IDLE 1, 2 mode					—	4.5	6	mA
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V / 0.2 V LCD driver is not enable		—	30	60	μA
Supply Current in SLEEP mode					—	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V		—	0.5	10	μA
Segment Output Low Resistance	R_{OS1}	SEG23 to SEG0 pins	V_{DD} = 5 V V_{DD} – V_{LC} = 3 V	RESL = 0 (Note 11)	—	20	—	kΩ
				RSEL = 1		7		
Common Output Low Resistance	R_{OC1}	COM3 to COM0 pins		RESL = 0		20		
				RSEL = 1		7		
Segment Output High Resistance	R_{OS2}	SEG23 to SEG0 pins		RESL = 0		200		
				RSEL = 1		70		
Common Output High Resistance	R_{OC2}	COM3 to COM0 pins		RESL = 0		200		
				RSEL = 1		70		
Segment /Common Output Voltage	$V_{O\ 2/3}$	SEG23 to SEG0 and COM3 to COM0 pins			3.8	4.0	4.2	V
	$V_{O\ 1/2}$				3.3	3.5	3.7	
	$V_{O\ 1/3}$				2.8	3.0	3.2	

Note 1: Typical values show those at Topr = 25°C , V_{DD} = 5 V.
Note 2: Input Current ; The current through pull-up or pull-down resistor is not included.
Note 3: IDD ; Except for I_{REF}.
Note 4: Output resustance R_{OS} and R_{OC} indicate "on" when switching levels.
Note 5: $V_{O2/3}$ indicates an output current at the 2/3 level when operating in the 1/4 or 1/3 duty mode.
Note 6: $V_{O1/2}$ indicates an output current at the 1/2 level when operating in the 1/2 duty or static mode.
Note 7: $V_{O1/3}$ indicates an output current at the 1/3 level when operating in the 1/4 or 1/3 duty mode.
Note 8: When you use a liquid crystal display (LCD), it is necessary to give careful consideration to the value of the output resistor $R_{OS\ 1/2}$, $R_{OC\ 1/2}$.
Note 9: R_{OS1}, R_{OC1}: On time of the lower output resistor is 2^7/fc, 1/(2·fs) [s].
Note 10: R_{OS2}, R_{OC2}: On time of the higher output resistor is 1/(n·f_F). (1/n duty, f_F: frame frequency)
Note 11: RSEL ; Bit 6 in LCDCR

A / D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	2.7	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7 V, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
			–	–	± 2	

Note : Quantizing error is not contained in those errors.

A.C. Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL 1, 2 mode	0.5	–	10	μs
		In IDLE 1, 2 mode				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

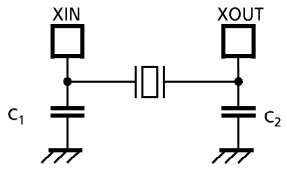
(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
TC1 input (ECIN input)	t_{TC1}	Frequency medsurement mode V_{DD} = 4.5 to 5.5 V	Single edge count	–	–	8	MHz
			Both edge count	–	–	4	
		Frequency medsurement mode V_{DD} = 2.7 to 5.5 V	Single edge count	–	–	4.2	
			Both edge count	–	–	3	

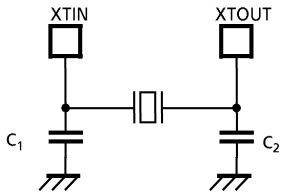
Recommended Oscillating Condition

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Frequency	Recommended Oscillator		Recommended Condition	
					C_1	C_2
High-frequency	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30pF	30pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20pF	20pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15pF	15pF



(1) High-frequency



(2) Low-frequency

Note: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.