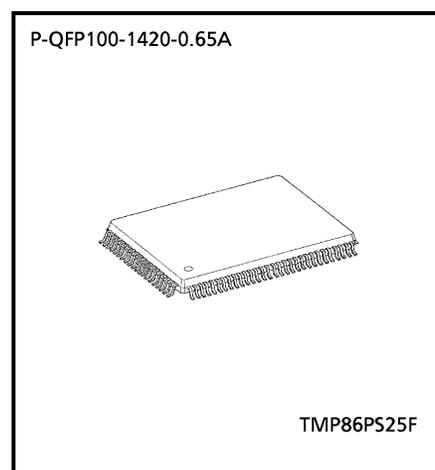


CMOS 8-Bit Microcontroller

TMP86PS25F

The TMP86PS25 is a OTP type MCU which includes 60-Kbyte one-time PROM. It is a pin compatible with a mask ROM product of the TMP86CM25/S25. Writing the program to built-in PROM, the TMP86PS25 operates as the same way as the TMP86CM25/S25. Using the Adapter socket, you can write and verify the data for the TMP86PS25 with a general-purpose PROM programmer same as TC571000D/AD.

Product No.	OTP	RAM	Package	Adapter Socket
TMP86PS25F	60 K × 8 bits	2 K × 8 bits	P-QFP100-1420-0.65A	BM11172

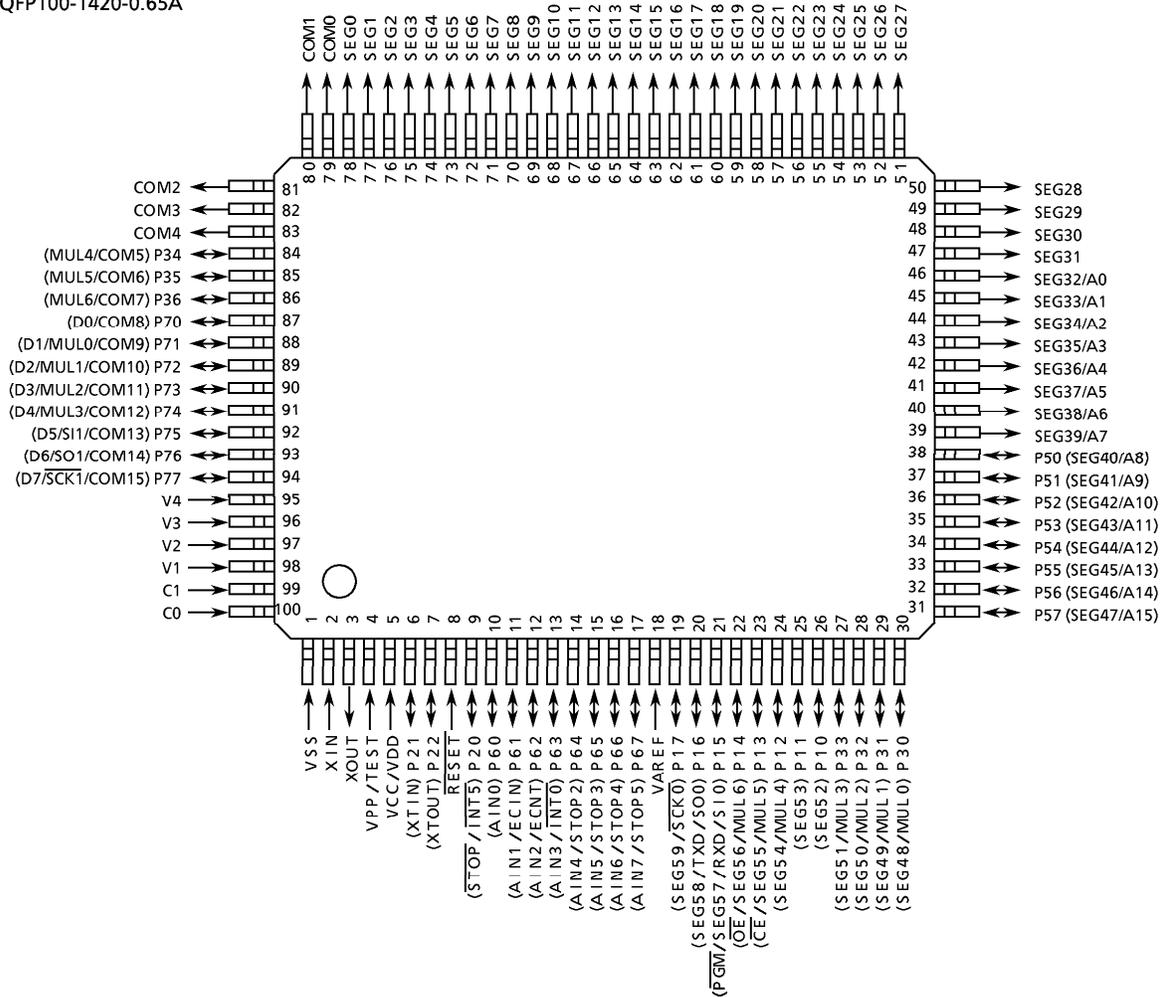


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Pin Assignments (Top View)

P-QFP100-1420-0.65A



Note: Ports assigned as MUL6 to MUL0 can switch pin assignment by the multifunction register (MULSEL). For functions assigned to each pin, see the table below.

Pin name	Function	Pin assignment
MUL0	DVO	P30 or P71
MUL1	PWM3, PDO3, TC3	P31 or P72
MUL2	PPG4, PWM4, PDO4, TC4	P32 or P73
MUL3	PPG6, PWM6, PDO6, TC6	P33 or P74
MUL4	INT1	P12 or P34
MUL5	INT2	P13 or P35
MUL6	INT3	P14 or P36

Pin Function

The TMP86PS25 has MCU mode and PROM mode.

(1) MCU mode

In the MCU mode, the TMP86PS25 is a pin compatible with the TMP86CM25/S25 (Make sure to fix the TEST pin to low level).

(2) PROM mode

Pin Name	Input/Output	Function	Pin Name (MCU mode)
A15 to A8 A7 to A0	Input	Input of Memory address for program	P57 to P50 SEG39 to SEG32
D7 to D0	I/O	Input/Output of Memory data for program	P77 to P70
\overline{CE}	Input	Chip enable	P13
\overline{OE}		Output enable	P14
PGM		Program control	P15
VPP	Power supply	+ 12.75 V/5 V (Power supply of program)	TEST
VCC		+ 6.25 V/5 V	VDD
GND, VAREF		0 V	VSS, VAREF
P11, P21	I/O	PROM mode setting pin. Fix to high.	
P10, P22, P20, P61		PROM mode setting pin. Fix to low.	
RESET			
P64, P65, P67	Output	Output pin for PROM operation test. Open or release.	
P17, P16, P12 P66, P63, P62, P60 P36 to P30 COM4 to COM0 SEG31 to SEG0 V4 to V1 C1, C0	I/O	Open	
XIN	Input	Self oscillation with resonator (8 MHz).	
XOUT	Output		

Note: No pin is applied to A16 input.

Operation

This section describes the functions and basic operational blocks of TMP86PS25.

The TMP86PS25 has PROM in place of the mask ROM which is included in the TMP86CM25/S25. The configuration and function are the same as the TMP86CM25/S25. For the functions of TMP86PS25 in details, see the section of TMP86CM25/S25.

In addition, TMP86PS25 operates as the single clock mode when releasing reset.

When using the dual clock mode, oscillate a low-frequency clock by SET. XTEN command at the beginning of program.

1. Operating Mode

The TMP86PS25 has MCU mode and PROM mode.

1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level.

In the MCU mode, the operation is the same as the TMP86CM25/S25 (TEST/VPP pin cannot be used open because it has no built-in pull-down resistor).

1.1.1 Program Memory

The TMP86PS25 has a 60-Kbyte built-in one time PROM (addresses 1000H to FFFFH in the MCU mode, addresses 0000H to EFFFH in the PROM mode).

When using TMP86PS25 for evaluation of TMP86CM25/S25, the program is written in the program storing area shown in Figure 1-1.

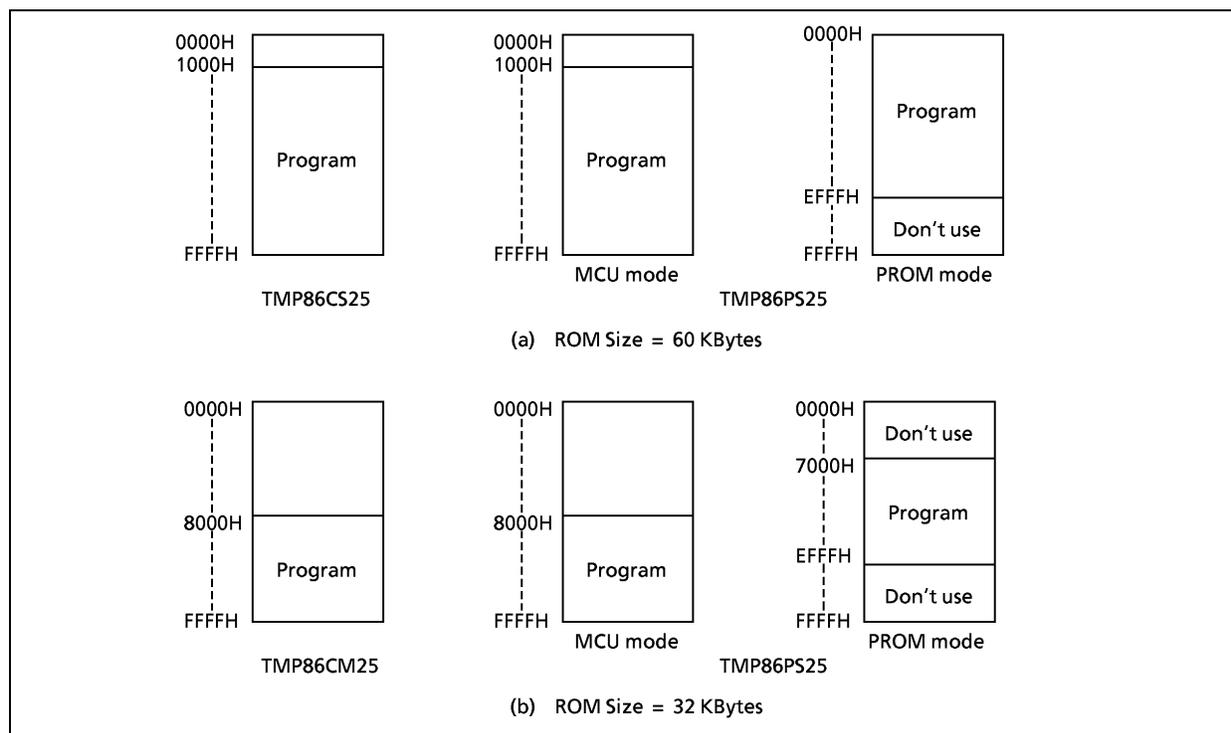


Figure 1-1. Program Memory Area

Note: The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

Electrical Characteristics

Absolute Maximum Ratings	($V_{SS} = 0\text{ V}$)
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Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		- 0.3 to 6.5	V
Program Voltage	V_{PP}	TEST/ V_{PP}	- 0.3 to 13.0	
Input Voltage	V_{IN}		- 0.3 to $V_{DD} + 0.3$	
Output Voltage	V_{OUT1}		- 0.3 to $V_{DD} + 0.3$	
Output Current (Per 1 pin)	I_{OUT1}	P6 Port	- 1.8	mA
	I_{OUT2}	P1, P2, P34 to P36, P5, P6, P7 Port	3.2	
	I_{OUT3}	P30 to P33 Port	30	
Output Current (Total)	ΣI_{OUT1}	P1, P2, P34 to P36, P5, P6, P7 Port	60	
	ΣI_{OUT2}	P30 to P33 Port	80	
Power Dissipation [$T_{opr} = 85^{\circ}\text{C}$]	PD		350	mW
Soldering Temperature (time)	T_{sld}		260 (10 μ)	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		- 55 to 125	
Operating Temperature	T_{opr}		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition	($V_{SS} = 0\text{ V}$, $T_{opr} = -40\text{ to }85^{\circ}\text{C}$)
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Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply Voltage	V_{DD}		$f_c = 16\text{ MHz}$	NORMAL1, 2 mode	4.5	5.5
				IDLE0, 1, 2 mode		
			$f_c = 8\text{ MHz}$	NORMAL1, 2 mode	2.7	
				IDLE0, 1, 2 mode		
			$f_c = 4.2\text{ MHz}$	NORMAL1, 2 mode	1.8	
				IDLE0, 1, 2 mode		
$f_s = 32.768\text{ kHz}$	SLOW1, 2 mode	1.8				
	SLEEP0, 1, 2 mode					
		STOP mode				
Input high Level	V_{IH1}	Except Hysteresis input	$V_{DD} \geq 4.5\text{ V}$	$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}			$V_{DD} < 4.5\text{ V}$		
Input low Level	V_{IL1}	Except Hysteresis input	$V_{DD} \geq 4.5\text{ V}$	0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}				$V_{DD} < 4.5\text{ V}$	
LCD reference voltage range	$V1_{IN}$	V1	$\text{LCDCTL1} < \text{REFV} > = "1"$	1.0	1.375	
	$V2_{IN}$	V2		2.0	2.750	
	$V3_{IN}$	V3		$V_{DD} < V4$ (Note 2)	3.0	4.125
	$V4_{IN}$	V4		4.0	5.500	
	$V4_{IN}$	V4 (Note 3)		$\text{LCDCTL1} < \text{REFV} > = "0"$	–	V_{DD}
Clock Frequency	f_c	XIN, XOUT	$V_{DD} = 1.8\text{ to }5.5\text{ V}$	1.0	4.2	MHz
			$V_{DD} = 2.7\text{ to }5.5\text{ V}$		8.0	
			$V_{DD} = 4.5\text{ to }5.5\text{ V}$		16.0	
	f_s	XTIN, XTOUT	30.0	34.0	kHz	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: When $\text{LCDCTL1} < \text{REFV} >$ is set to "1", always keep the condition of $V_{DD} < V4$.

Note 3: When $\text{LCDCTL1} < \text{REFV} >$ is set to "0", always supply the reference voltage from V4 pin.

DC Characteristics

 $(V_{SS} = 0\text{ V}, T_{opr} = -40\text{ to }85^{\circ}\text{C})$

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	$V_{DD} = 5.5\text{ V}, V_{IN} = 5.5\text{ V}/0\text{ V}$	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state					
	I_{IN3}	$\overline{\text{RESET}}, \overline{\text{STOP}}$					
Input Resistance	R_{IN2}	$\overline{\text{RESET}}$ Pull-Up		100	220	450	$\text{k}\Omega$
Output Leakage Current	I_{LO}	Sink Open Drain, Tri-state	$V_{DD} = 5.5\text{ V}, V_{OUT} = 5.5\text{ V}/0\text{ V}$	–	–	± 2	μA
Output High Voltage	V_{OH2}	Tri-st Port	$V_{DD} = 4.5\text{ V}, I_{OH} = -0.7\text{ mA}$	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT P30 to P33 Port	$V_{DD} = 4.5\text{ V}, I_{OL} = 1.6\text{ mA}$	–	–	0.4	
Output Low Current	I_{OL}	High Current Port (P30 to P33 Port)	$V_{DD} = 4.5\text{ V}, V_{OL} = 1.0\text{ V}$	–	20	–	mA
Supply Current in NORMAL 1, 2 mode	V_{DD}		$V_{DD} = 5.5\text{ V}$ $V_{IN} = 5.3/0.2\text{ V}$ $f_c = 16\text{ MHz}$ $f_s = 32.768\text{ kHz}$	–	6.2	9.0	
Supply Current in IDLE 0, 1, 2 mode				–	3.7	6.5	
Supply Current in SLOW 1 mode			–	10	25		
Supply Current in SLEEP 1 mode			–	4.5	15		
Supply Current in SLEEP 0 mode			–	3.5	13		
Supply Current in STOP mode			$V_{DD} = 5.5\text{ V}$ $V_{IN} = 5.3\text{ V}/0.2\text{ V}$	–	0.5	10	

Note 1: Typical values show those at $T_{opr} = 25^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$

Note 2: Input current (I_{IN1} , I_{IN2}); The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

AD Conversion Characteristics

($V_{SS} = 0.0 \text{ V}$, $4.5 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$, $T_{opr} = -40 \text{ to } 85^\circ\text{C}$)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		$V_{DD} - 1.5$	–	V_{DD}	V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}		3.0	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = V_{AREF} = 5.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	–	0.6	1.0	mA
Non linearity Error		$V_{DD} = 5.0 \text{ V}$, $V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 5.0 \text{ V}$	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

($V_{SS} = 0.0 \text{ V}$, $2.7 \text{ V} \leq V_{DD} < 4.5 \text{ V}$, $T_{opr} = -40 \text{ to } 85^\circ\text{C}$)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		$V_{DD} - 1.5$	–	V_{DD}	V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}		2.5	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = V_{AREF} = 4.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	–	0.5	0.8	mA
Non linearity Error		$V_{DD} = 2.7 \text{ V}$, $V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 2.7 \text{ V}$	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

($V_{SS} = 0.0 \text{ V}$, $2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}$, $T_{opr} = -40 \text{ to } 85^\circ\text{C}$) Note 5
 ($V_{SS} = 0.0 \text{ V}$, $1.8 \text{ V} \leq V_{DD} < 2.0 \text{ V}$, $T_{opr} = -10 \text{ to } 85^\circ\text{C}$) Note 5

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		$V_{DD} - 0.9$	–	V_{DD}	V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}	$1.8 \text{ V} \leq V_{DD} < 2.0 \text{ V}$	1.8	–	–	
		$2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}$	2.0	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = V_{AREF} = 2.7 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	–	0.3	0.5	mA
Non linearity Error		$V_{DD} = 1.8 \text{ V}$, $V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 1.8 \text{ V}$	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

Note 1: The total error includes all errors except a quantization error, and is defined as maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".

Note 3: Please use input voltage to AIN input Pin in limit of $V_{AREF} - V_{SS}$. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: $\Delta V_{AREF} = V_{AREF} - V_{SS}$

Note 5: When AD is used with $V_{DD} < 2.7 \text{ V}$, the guaranteed temperature range varies with the operating voltage.

AC Characteristics

 $(V_{SS} = 0\text{ V}, V_{DD} = 4.5\text{ to }5.5\text{ V}, T_{opr} = -40\text{ to }85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	NORMAL 1, 2 mode	0.25	-	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	-	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	tw _{CH}	For external clock operation (XIN input)	-	31.25	-	ns
Low Level Clock Pulse Width	tw _{CL}	fc = 16 MHz	-	31.25	-	ns
High Level Clock Pulse Width	tw _{CH}	For external clock operation (XTIN input)	-	15.26	-	μs
Low Level Clock Pulse Width	tw _{CL}	fc = 32.768 kHz	-	15.26	-	μs

 $(V_{SS} = 0\text{ V}, V_{DD} = 2.7\text{ to }4.5\text{ V}, T_{opr} = -40\text{ to }85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	NORMAL 1, 2 mode	0.5	-	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	-	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	tw _{CH}	For external clock operation (XIN input)	-	62.5	-	ns
Low Level Clock Pulse Width	tw _{CL}	fc = 8 MHz	-	62.5	-	ns
High Level Clock Pulse Width	tw _{CH}	For external clock operation (XTIN input)	-	15.26	-	μs
Low Level Clock Pulse Width	tw _{CL}	fc = 32.768 kHz	-	15.26	-	μs

 $(V_{SS} = 0\text{ V}, V_{DD} = 1.8\text{ to }2.7\text{ V}, T_{opr} = -40\text{ to }85^{\circ}\text{C})$

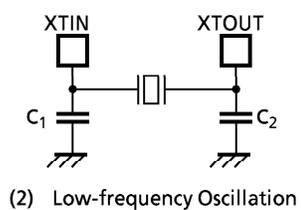
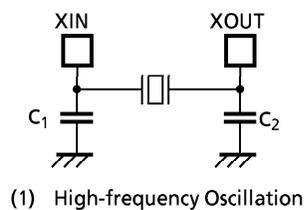
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	NORMAL 1, 2 mode	0.95	-	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	-	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	tw _{CH}	For external clock operation (XIN input)	-	119.05	-	ns
Low Level Clock Pulse Width	tw _{CL}	fc = 4.2 MHz	-	119.05	-	ns
High Level Clock Pulse Width	tw _{CH}	For external clock operation (XTIN input)	-	15.26	-	μs
Low Level Clock Pulse Width	tw _{CL}	fc = 32.768 kHz	-	15.26	-	μs

Timer Counter 1 input (ECIN) Characteristics

 $(V_{SS} = 0\text{ V}, T_{opr} = -40\text{ to }85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Typ.	Max	Unit	
TC1 input (ECIN input)	t _{TC1}	Frequency measurement mode V _{DD} = 4.5 to 5.5 V	Single edge count	-	-	1.0	MHz
		Frequency measurement mode V _{DD} = 2.7 to 4.5 V	Single edge count	-	-	0.5	
		Frequency measurement mode V _{DD} = 1.8 to 2.7 V	Single edge count	-	-	0.262	

Recommended Oscillating Conditions



Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: TOYAMA MURATA MFG. CO., LTD. (JAPAN)

These product numbers and the corresponding specifications are subject to change.

For up-to-date information, please refer to the following URL;

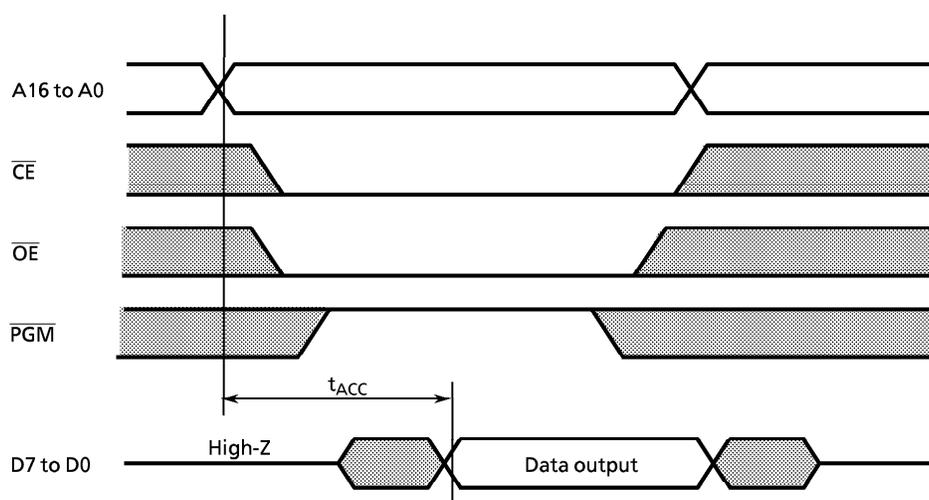
<http://www.murata.co.jp/search/index.html>

DC Characteristics, AC Characteristics (PROM Mode) ($V_{SS} = 0\text{ V}$, $T_{opr} = -40\text{ to }85^{\circ}\text{C}$)

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH4}		2.2	–	V_{CC}	V
Low level input voltage (TTL)	V_{IL4}		0	–	0.8	
Power supply	V_{CC}		4.75	5.0	5.25	
Power supply of program	V_{PP}					
Address access time	t_{ACC}	$V_{CC} = 5.0 \pm 0.25\text{ V}$	–	$1.5t_{cyc} + 300$	–	ns

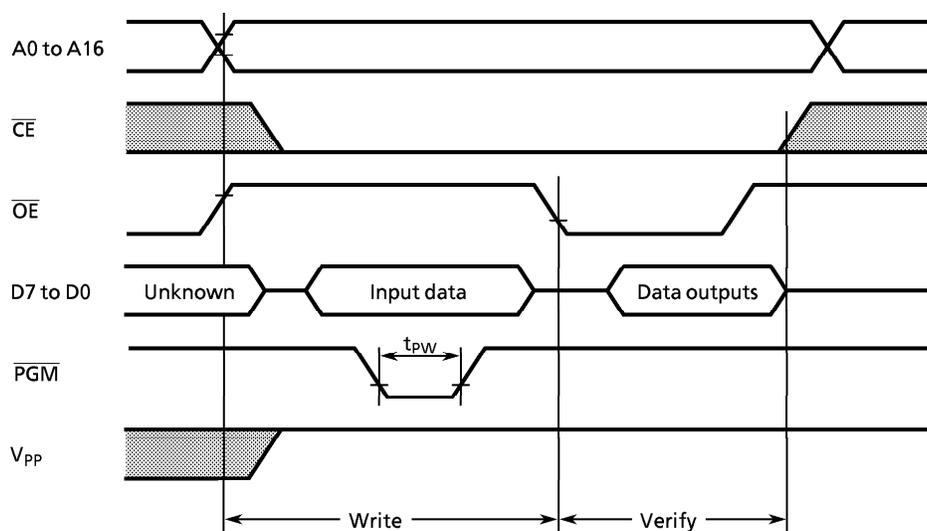
Note: $t_{cyc} = 500\text{ ns}$ at 8 MHz



(2) Program operation (High-speed) ($T_{opr} = 25 \pm 5^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH4}		2.2	–	V_{CC}	V
Low level input voltage (TTL)	V_{IL4}		0	–	0.8	
Power supply	V_{CC}		6.0	6.25	6.5	
Power supply of program	V_{PP}		12.5	12.75	13.0	
Pulse width of initializing program	t_{PW}	$V_{CC} = 6.0\text{ V}$	0.095	0.1	0.105	ms

High-speed program writing



Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC} .

Note 2: The pulling up/down device on the condition of $V_{PP} = 12.75\text{ V} \pm 0.25\text{ V}$ causes a damage for the device. Do not pull up/down at programming.

Note 3: Use the recommended adapter (see 1.2.2 (1)) and mode (see 1.2.2 (3) i).

Using other than the above condition may cause the trouble of the writing.