CMOS 4-Bit Microcontroller

TMP47C102P, TMP47C202P TMP47C102M, TMP47C202M

The TMP47C102/202 are high speed and high performance 4-bit single chip microcomputers, integrating ROM, RAM, input / output ports and timer / counters on a chip. The TMP47C102/202 are the standard LSI in the TLCS-47E series.

In addition, they have the output port with LED direct drive capability.

| Part No. | ROM | RAM | Package | OTP |
|------------|--------------|-------------|-------------------|-------------|
| TMP47C102P | 1024 × 8-bit | C44 hit | P-DIP20-300-2.54A | TMP47P202VP |
| TMP47C102M | 1024 X 8-DIT | 64 × 4-bit | P-SOP20-300-1.27 | TMP47P202VM |
| TMP47C202P | 20400 hit | 120 4 hit | P-DIP20-300-2.54A | TMP47P202VP |
| TMP47C202M | 2048 × 8-bit | 128 × 4-bit | P-SOP20-300-1.27 | TMP47P202VM |

Features

4-bit single chip microcomputer

 \blacklozenge Instruction execution time: 1.3 μ s (at 6 MHz) ◆Low voltage operation: 2.2 V (at 2 MHz RC)

◆89 basic instructions

ROM table look-up instructions

Subroutine nesting: 15 levels max

◆5 interrupt sources (External: 2, Internal: 3) All sources have independent latches each, and multiple

interrupt control is available.

♦ I/O port (15 pins)

◆Two 12-bit Timer / Counters

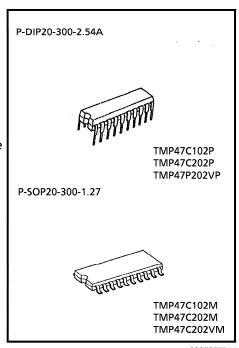
Timer, event counter, and pulse width mea-surement mode

- ◆Interval Timer
- Watchdog timer
- High current outputs

LED direct drive capability: typ. 20 mA × 4 bits (port R4) typ. $7 \text{ mA} \times 4 \text{ bits (port R5)}$

Hold function

Battery / Capacitor back-up Real Time Emulator: BM47C203



For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA

products could cause loss of human life, bodily injury or damage to property.

In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..

The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, applications) of the products of the products applications (computer, applications) of the products applications (computer, applications) of the products is applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer, applications) of the products are used within specified operating applications (computer) applications (computer) of the products are used within specified operating applications (computer).

personal equipment, office equipment, measuring equipment, industrial robotics, domestic applications (colingular, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's

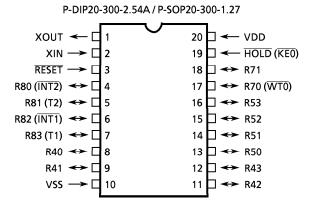
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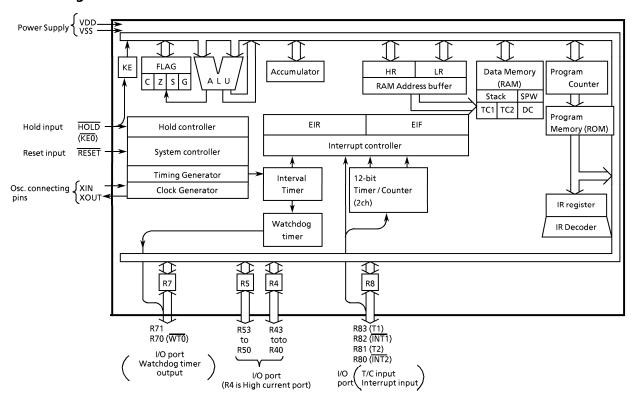
The information contained herein is subject to change without notice.

6-02-1 2000-10-19

Pin Assignment (Top View)



Block Diagram



Pin Function

| Pin Name | Input / Output | Functions | | | | |
|---|----------------|--|--|--|--|--|
| R43 to R40 R53 to R50 R71 | I/O | 4-bit I/O port with latch (R7 port has only 2-bit). When used as input port, the latch must be set to "1". Every bit data is possible to be set, cleared and | | | | |
| R70 (WTO) | I/O (Output) | tested by the bit manipulation instruction of the L-register indirect addressing. | Watchdog timer output | | | |
| R83 (T1) R82 (ĪNT1) R81 (T2) R80 (ĪNT2) | I/O (Input) | 4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1". | Timer / Counter 1 external input External interrupt 1 input Timer / Counter 2 external input External interrupt 2 input | | | |
| XIN | Input | Resonator connecting pins. | | | | |
| хоит | Output | For inputting external clock, XIN is used and XOUT is opened. | | | | |
| RESET | Input | Reset signal input | | | | |
| HOLD (KEO) | Input (Input) | Hold request / release signal input | Sense input | | | |
| VDD VSS | Power Supply | + 5 V 0 V (GND) | | | | |

Operational Description

Concerning the above component parts, the configuration and functions of hardware are described. The basic instruction of configuration in the TMP47C102/202 is the same as those of TLCS-470 series.

1. System Configuration

- ◆ Internal CPU Function
 - 2.1 Program Counter (PC)
 - 2.2 Program Memory (ROM)
 - 2.3 H Register, L Register
 - 2.4 Data Memory (RAM)
 - Stack
 - Stack Pointer Word (SPW)
 - Data Counter (DC)
 - 2.5 ALU, Accumulator
 - 2.6 Flags
 - 2.7 System Controller
 - 2.8 Interrupt Controller
 - 2.9 Reset Circuit

◆ Peripheral Hardware Function

- 3.1 I/O Ports
- 3.2 Interval Timer
- 3.3 Timer / Counters (TC1, TC2)
- 3.4 Watchdog Timer

2. Internal CPU Function

2.1 Program Counter (PC)

The program counter is a 11-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

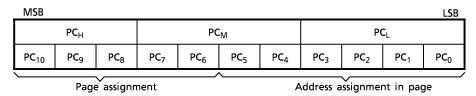


Figure 2-1. Configuration of Program Counter

The PC can directly address a 2048-byte address space. However, with the short branch, the following points must be considered:

• Short branch instruction [BSS a]

In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 5 bits of the PC point the next page, so that branch is made to the next page.

| In | Instruction or Condition | | | | | | _ | n Count | | | _ | | l | | | |
|----------|--------------------------|--|---|---|-----------------|-----------------|---|-----------------|--------------------------|-----------------|----------|-----------------|-----------------|-----------------|----------|--------|
| | peration | | | PC ₁₀ | PC ₉ | PC ₈ | PC ₇ | PC ₆ | PC ₅ | PC ₄ | PC3 | PC ₂ | PC ₁ | PC ₀ | | |
| 0 | BS a | SF = 1 (Branch condition is satisfied) SF = 0 (Branch condition is not satisfied) | | Immediate data specified by the instruction | | | | | | | | | | | | |
| c t | 3 | | | | + 2 | | | | | | | | | | | |
| ם ב | | Lower 6-bit address ≠ 111111 | | ≠ 111111 | | | Н | old | | lmr | mediate | data s | pecifie | d by th | e instru | ıction |
| l n s t | BSS a | | Lower 6-bit address = 111111 (last address in page) | + 1 | | | Immediate data specified by the instruction | | | | | ıction | | | | |
| | | SF = 0 | | | | | | + 1 | | | | | | | | |
| 0 | CALL a | | Immediate data specified by the instruction | | | | | | | | | | | | | |
| 0 | CALLS a | | | 0 | 0 | 0 | | | ated by th y the inst | | liate | 1 | 1 | 0 | | |
| ت ب | RET | The return address restored from stack | | | | | | | | | | | | | | |
| e × | RETI | The return address restored from st. | | | | | | om stac | :k | | | | | | | |
| Гû | Others | | | Incremented by the number of bytes in the instruction | | | | | | | | | | | | |
| | errupt eptance | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Inte | rrupt ve | ector | 0 | | |
| | Reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

Table 2-1. Status Change of Program Counter

2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC.

The fixed data can be read by using the table look-up instructions.

Table look-up instructions

[LDL A, @DC], [LDH A, @DC+]

The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A, @DC] instruction reads the lower 4 bits of fixed data, and [LDH A, @DC+] instruction reads the upper 4 bits.

The DC is a 12-bit register, allowing it to address the entire program memory space.

In this case, the uppers bit of the DC (MSB) is ignored.

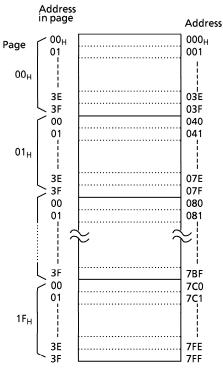


Figure 2-2. Configuration of Program Memory

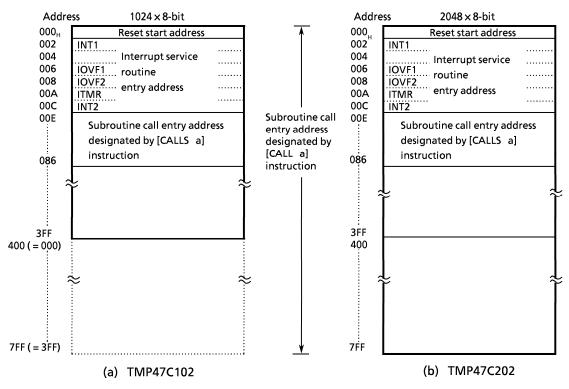
2.2.1 Program Memory Capacity

The TMP47C102 has 1024 \times 8 bits (addresses 000_H through 3FF_H) of program memory (mask ROM), the TMP47C202 has 2048 \times 8 bits (addresses 000_H through 7FF_H).

Figure 2-3 shows the program memory map. Address $000_{\rm H}$ to $086_{\rm H}$ of the program memory are also used for special purposes.

2.2.2 Program Memory Map

On the TMP47C102, no physical program memory exists in the address range $400_{\rm H}$ through 7FF_H. However, if this space is accessed by program, the most significant bit of each address is always regarded as "0" and the contents of the program memory corresponding to the address $000_{\rm H}$ through 3FF_H are read.



Note: Address 004_H and 005_H can be used to store ordinary user's processing data.

Figure 2-3. Program Memory Map

Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

| Parameter | Symbol | Pins | | Ratings | Unit | |
|---------------------------------|---------------------|------------------------------|-----|--------------------------------|------|--|
| Supply Voltage | V_{DD} | | | – 0.3 to 6.5 | V | |
| Input Voltage | V_{IN} | - 0.3 to V _{DD} + 0 | | – 0.3 to V _{DD} + 0.3 | ٧ | |
| Output Voltage | V _{OUT} | | | - 0.3 to V _{DD} + 0.3 | ٧ | |
| | I _{OUT1} | Port R4 | | 30 | | |
| Output Current (Per 1 pin) | I _{OUT2} | Port R5 | 15 | mA | | |
| | I _{OUT3} | Ports R7, R8 | | 3.2 | | |
| Output Current (Total) | Σ I _{OUT1} | Port R4, R5 | | 60 | mΑ | |
| Down Dissipation [Tone 70%] | PD | DIP | | 300 | \4/ | |
| Power Dissipation [Topr = 70°C] | PD | | SOP | 180 | mW | |
| Soldering Temperature (time) | Tsld | | | 260 (10 s) | ů | |
| Storage Temperature | Tstg | | | – 55 to 125 | °C | |
| Operating Temperature | Topr | | | – 30 to 70 | °C | |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

| Parameter | Symbol | Pins | | Con | Conditions | | Max | Unit |
|--------------------|----------------------|-------------------------|-----------|--------------------------------|--------------------------------|----------------------|----------------------|----------------|
| | | | Normal | Crystar | fc = 6.0 MHz | 4.5 | | |
| Supply Voltage | W | | Normal | or ceramic | fc = 4.2 MHz | 2.7 |] | l _v |
| | V_{DD} | | mode | RC | fc = 2.5 MHz | 2.2 | 5.5 | l v |
| | | | HOLD mode | _ | _ | 2.0 | | |
| Input High Voltage | V_{IH1} | Except Hysteresis Input | | In the normal | | $V_{DD} \times 0.7$ | | |
| | V_{IH2} | Hysteresis Input | | operating area | | $V_{DD} \times 0.75$ | V_{DD} | V |
| | V _{IH3} | | | In the HOLD mode | | $V_{DD} \times 0.9$ | | |
| | V_{IL1} | Except Hysteresis Input | | In the normal | | | $V_{DD} \times 0.3$ | |
| Input Low Voltage | V_{IL2} | Hysteresis Input | | operating area | | 0 | $V_{DD} \times 0.25$ | V |
| | V _{IL3} | | | In the HOLD mode | | | $V_{DD} \times 0.1$ | |
| | requency fc XIN, XOU | | | V _{DD} = 4 | V _{DD} = 4.5 to 5.5 V | | 6.0 | |
| Clock Frequency | | | IT | V _{DD} = 2.7 to 5.5 V | | 0.4 | 4.2 | MHz |
| | | | | V _{DD} = 2.2 | to 5.5 V (RC) | | 2.5 | |

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics

 $(V_{SS} = 0 \text{ V, Topr} = -30 \text{ to } 70^{\circ}\text{C})$

| Parameter | Symbol | Pins | Conditions | Min | Тур. | Max | Unit | |
|---|--------------------------|-----------------------------|--|-----|------|-----|------|--|
| Hysteresis Voltage | V _{HS} | Hysteresis Input | | _ | 0.7 | - | V | |
| Input Current | I _{IN1} | RESET, HOLD | V - F F V V - F F V / O V | | | ± 2 | μΑ | |
| input Current | I _{IN2} | Open drain output ports | $V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V} / 0 \text{ V}$ | _ | _ | | | |
| Input Resistance | R _{IN} | RESET | | 100 | 220 | 450 | kΩ | |
| Input Low Current | I _{IL} | Push-pull output ports | $V_{DD} = 5.5 \text{ V}, \ V_{IN} = 0.4 \text{ V}$ | _ | _ | - 2 | mA | |
| Output Leakage Current | I _{LO} | Open drain output ports | V _{DD} = 5.5 V, V _{OUT} = 5.5 V | _ | - | 2 | μΑ | |
| Output High Voltage | | | $V_{DD} = 4.5 \text{ V}, \ I_{OH} = -200 \ \mu\text{A}$ | 2.4 | - | _ | ., | |
| | VOH | Push-pull output ports | $V_{DD} = 2.2 \text{ V}, \ I_{OH} = -5 \mu\text{A}$ | 2.0 | _ | _ | V | |
| Output Low | l | V _{OL} Port R7, R8 | $V_{DD} = 4.5 \text{ V}, \ I_{OL} = 1.6 \text{ mA}$ | _ | - | 0.4 |]] | |
| Voltage | V _{OL} | | $V_{DD} = 2.2 \text{ V}, \ I_{OL} = 20 \ \mu\text{A}$ | _ | _ | 0.1 | V | |
| | I _{OL1} Port R4 | | | _ | 20 | _ | | |
| Output Low Current | I _{OL2} | Port R5 | $V_{DD} = 4.5 \text{ V}, \ V_{OL} = 1.0 \text{ V}$ | _ | 7 | _ | mA | |
| Supply Current (in the Normal operating mode) | | | V _{DD} = 5.5 V, fc = 4 MHz | _ | 2 | 4 | | |
| | I _{DD} | | V _{DD} = 5.5 V, fc = 4 MHz | _ | 1 | 2 | mA | |
| | | | $V_{DD} = 3.0 \text{ V}, \text{ fc} = 400 \text{ kHz}$ | _ | 0.5 | 1 | | |
| Supply Current (in the HOLD operating mode) | I _{DDH} | | V _{DD} = 5.5 V | - | 0.5 | 10 | μΑ | |

Note 1: Typ. values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1} : The current through resistor is not included.

Note 3: Supply Current: $V_{IN} = 5.3 \text{ V} / 0.2 \text{ V} (V_{DD} = 5.5 \text{ V}) \text{ or } 2.8 \text{ V} / 0.2 \text{ V} (V_{DD} = 3.0 \text{ V})$

AC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

| Parameter | Symbol | Co | nditions | Min | Тур. | Max | Unit |
|------------------------------|------------------|------------------------------------|--|-----|-------------|-----|------|
| Instruction Cycle Time | | | $V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$ | 1.3 | | 20 | |
| | tcy | | $V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$ | 1.9 | _ | | μS |
| | | | V _{DD} = 2.2 to 5.5 V | 3.2 | | | |
| History Classic walks Winds | t _{WCH} | For external clock operation | V _{DD} ≧2.7 V | 80 | - - - | - | |
| High level Clock pulse Width | | | V _{DD} <2.7 V | 160 | | | ns |
| Low level Clock pulse Width | t _{WCL} | | V _{DD} ≧2.7 V | 80 | | | 113 |
| | | | V _{DD} <2.7 V | 160 | | | |

Recommended Oscillating Conditions

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

(1) 6 MHz

Ceramic Resonator

CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ EFOEC6004A4 (NATIONAL) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ XIN XOUT

6 MHz

or
4 MHz

C_{XIN}

C_{XOUT}

(2) 4 MHz

Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ EFOEC4004A4 (NATIONAL) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ C_{XIN} XOUT R_{XOUT} C_{XOU}

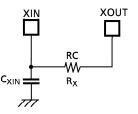
Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT} = 20 pF$

(3) 400 kHz

Ceramic Resonator

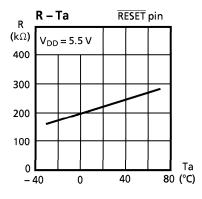
 $\begin{array}{lll} \text{CSB400B (MURATA)} & \text{C}_{\text{XIN}} = \text{C}_{\text{XOUT}} = 220 \text{ pF}, \text{ R}_{\text{XOUT}} = 6.8 \text{ k}\Omega \\ \text{KBR-400B (KYOCERA)} & \text{C}_{\text{XIN}} = \text{C}_{\text{XOUT}} = 100 \text{ pF}, \text{ R}_{\text{XOUT}} = 10 \text{ k}\Omega \\ \text{EFOA400K04B (NATIONAL)} & \text{C}_{\text{XIN}} = \text{C}_{\text{XOUT}} = 470 \text{ pF}, \text{ R}_{\text{XOUT}} = 0 \Omega \\ \end{array}$

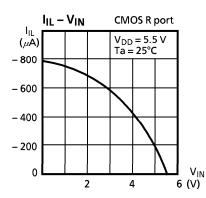


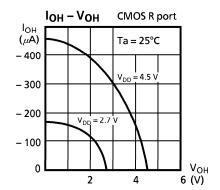
(4) RC Oscillation ($V_{SS} = 0V$, $V_{DD} = 5.0 V$, Topr = 25°C)

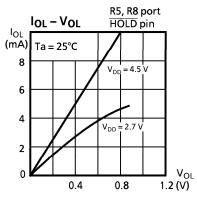
2 MHz (Typ.) $C_{XIN} = 33 \, pF, \, R_X = 10 \, k\Omega$ 400 kHz (Typ.) $C_{XIN} = 100 \, pF, \, R_X = 30 \, k\Omega$

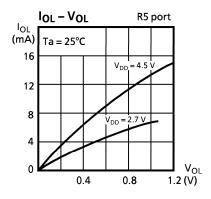
Typical Characteristics

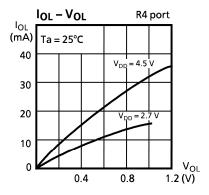


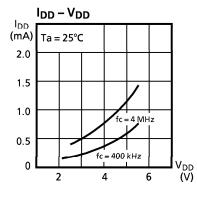


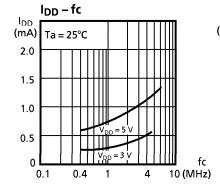


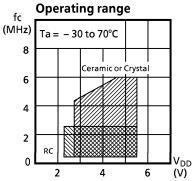


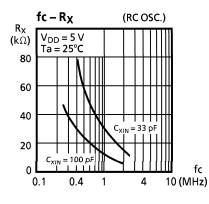


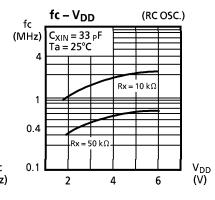












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