- **Output Swing includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
  950 μV Max at T_A = 25°C (TLC2262A)
- **Macromodel Included**
- **Performance Upgrade for the TS27M2/M4 and TLC27M2/M4**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control/Print Support
  Qualification to Automotive Standards

description

The TLC2262 and TLC2264 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC226x family offers a compromise between the micropower TLC225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

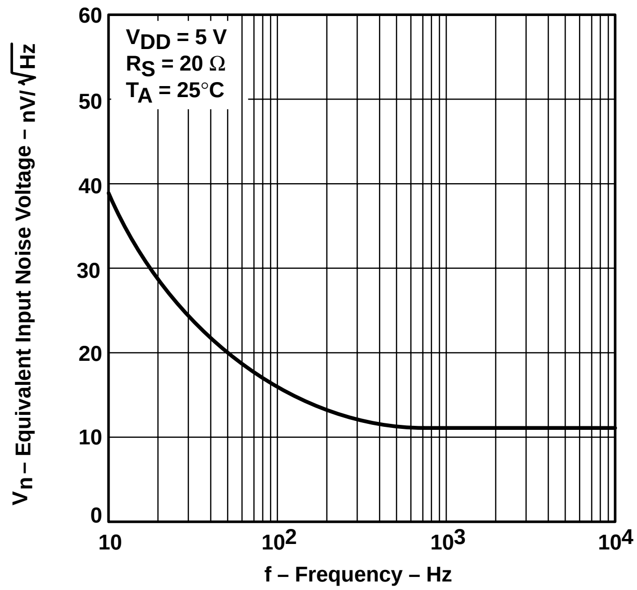


Figure 1

The TLC226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC226xA family is available and has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2262/4 also makes great upgrades to the TLC27M2/L4 or TS27M2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

TLC2262 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	2.5 mV	TLC2262CD	—	—	TLC2262CP	TLC2262CPW	—
–40°C to 125°C	950 μV 2.5 mV	TLC2262AID TLC2262ID	— —	— —	TLC2262AIP TLC2262IP	TLC2262AIPW —	— —
–40°C to 125°C	950 μV 2.5 mV	TLC2262AQD TLC2262QD	— —	— —	— —	— —	— —
–55°C to 125°C	950 μV 2.5 mV	— —	TLC2262AMFK TLC2262MFK	TLC2262AMJG TLC2262MJG	— —	— —	TLC2262AMU TLC2262MU

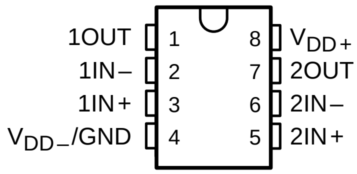
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

TLC2264 AVAILABLE OPTIONS

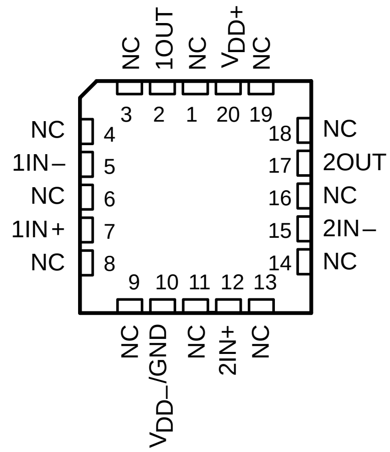
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)
0°C to 70°C	2.5 mV	TLC2264CD	—	—	TLC2264CN	TLC2264CPW	—
–40°C to 125°C	950 μV 2.5 mV	TLC2264AID TLC2264ID	— —	— —	TLC2264AIN TLC2264IN	TLC2264AIPW —	— —
–40°C to 125°C	950 μV 2.5 mV	TLC2264AQD TLC2264QD	— —	— —	— —	— —	— —
–55°C to 125°C	950 μV 2.5 mV	— —	TLC2264AMFK TLC2264MFK	TLC2264AMJ TLC2264MJ	— —	— —	TLC2264AMW TLC2264MW

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2264CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

TLC2262C, TLC2262AC
TLC2262I, TLC2262AI
TLC2262Q, TLC2262AQ
D, P, OR PW PACKAGE
(TOP VIEW)

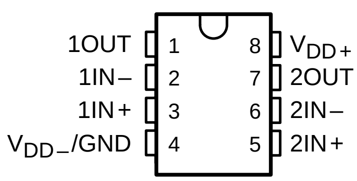


TLC2262M, TLC2262AM . . . FK PACKAGE
(TOP VIEW)

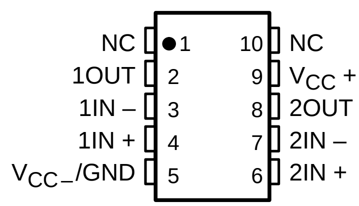


NC – No internal connection

TLC2262M, TLC2262AM . . . JG PACKAGE
(TOP VIEW)

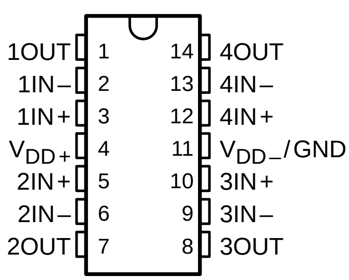


TLC2262M, TLC2262AM . . . U PACKAGE
(TOP VIEW)

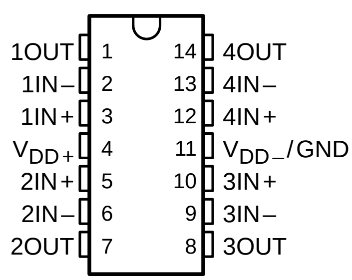


NC – No internal connection

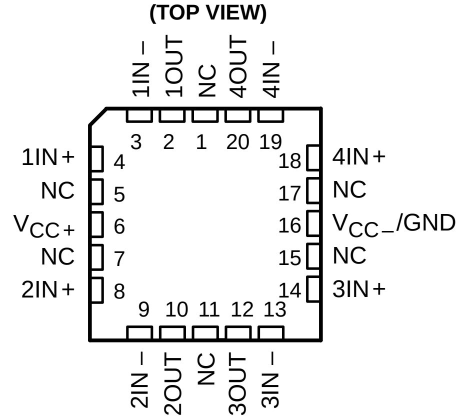
TLC2264C, TLC2264AC
TLC2264I, TLC2264AI
TLC2264Q, TLC2264AQ
D, N, OR PW PACKAGE
(TOP VIEW)



TLC2264M, TLC2264AM . . . J OR W PACKAGE
(TOP VIEW)

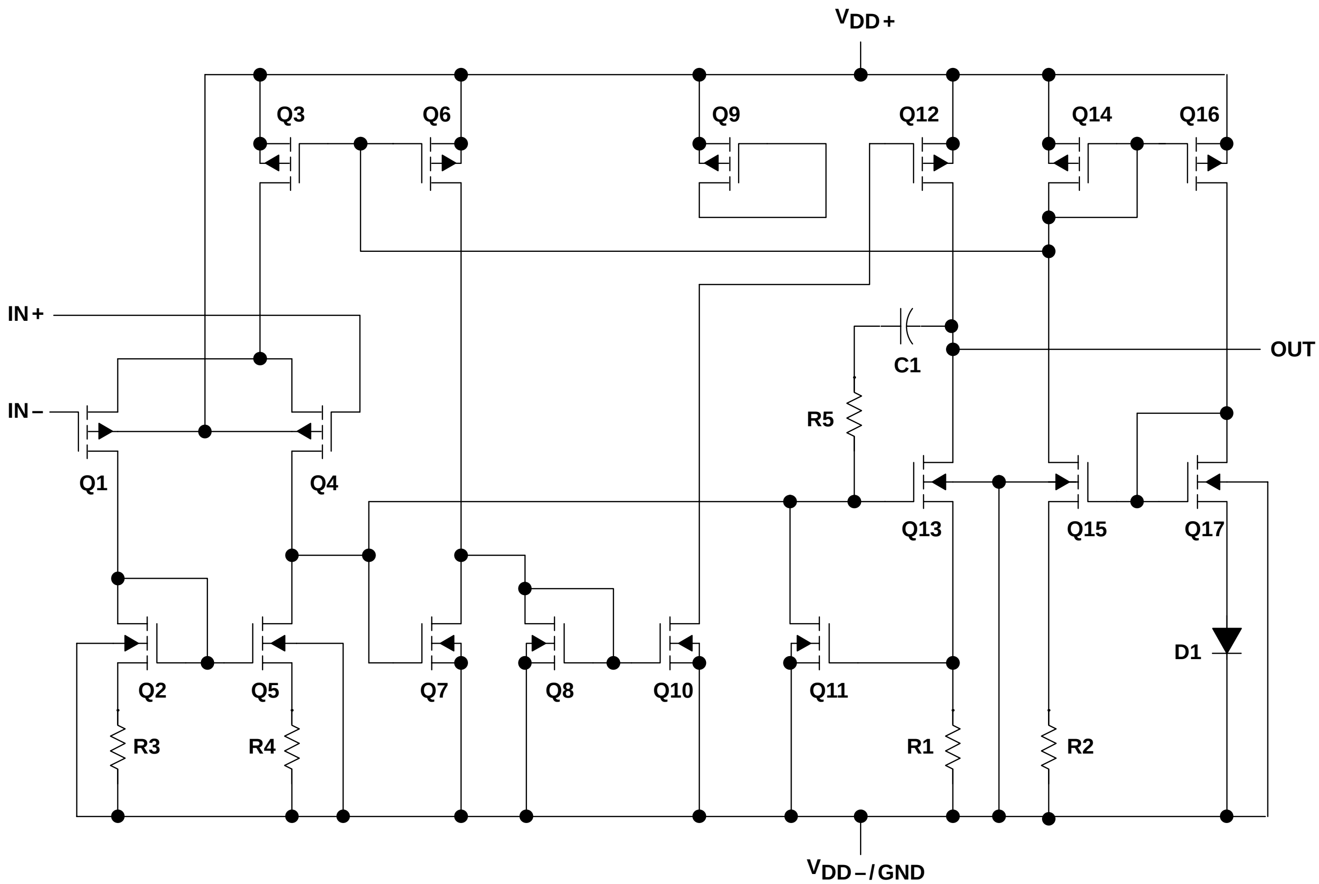


TLC2264M, TLC2264AM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2262	TLC2264
Transistors	38	76
Resistors	28	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . . –8 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±16 V
Input voltage, V_I (any input, see Note 1) . . . . . V_{DD-} – 0.3 V to V_{DD+}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 125°C
Q suffix . . . . . –40°C to 125°C
M suffix . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, and PW packages . . . . . 260°C
J, JG, U, and W packages . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows if input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW–14	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C

TLC2262C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262C MIN	TLC2262C TYP	TLC2262C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500	μV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		
				Full range	4.82			
		I_{OH} = −400 μA		25°C	4.70	4.85		
				Full range	4.60			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15	
				Full range			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.7	1	
				Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		V/mV
				Full range	55			
			R_L = 1 MΩ‡	25°C		550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500	μA
				Full range			500	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262C MIN	TLC2262C TYP	TLC2262C MAX	UNIT
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		µs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		56°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

TLC2262C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	TLC2262C MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500	µV
			Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV, $R_S = 50\ \Omega$	25°C	−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		
			Full range	4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		
			Full range	4.6			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		
			Full range	−4.85			
		$V_{IC} = 0$, $I_O = 1$ mA	25°C	−4.7	−4.8		
			Full range	−4.7			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		
			Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 50\ k\Omega$	25°C	80	200		V/mV
			Full range	55			
		$V_O = \pm 4$ V, $R_L = 1\ M\Omega$	25°C		1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$ V, $R_S = 50\ \Omega$	25°C	75	88		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = 2.2$ V to ± 8 V, $V_{IC} = 0$, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 0$ V, No load	25°C		425	500	µA
			Full range			500	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262C MIN	TLC2262C TYP	TLC2262C MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm1.9$ V, $C_L = 100$ pF	$R_L = 50$ kΩ	25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion pulse duration	$V_O = \pm2.3$ V, f = 20 kHz, $R_L = 50$ kΩ	$A_V = 1$	25°C		0.014%		
			$A_V = 10$			0.024%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ	25°C		0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		85		kHz
t_s	Settling time	$A_V = -1$, Step = –2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1		µs
			To 0.01%			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.

TLC2264C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500	μV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le$ 5 mV	25°C	0 to 4	–0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = –20 μA		25°C		4.99		V
		I_{OH} = –100 μA		25°C	4.85	4.94		
				Full range	4.82			
		I_{OH} = –400 μA		25°C	4.70	4.85		
				Full range	4.60			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15	
				Full range			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.7	1	
				Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		V/mV
				Full range	55			
			R_L = 1 MΩ‡	25°C		550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1	mA
				Full range			1	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4. Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		µs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

TLC2264C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	$V_O = 0$,	25°C		300	2500	μV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	$R_S = 50\ \Omega$	25°C	−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$		25°C		4.99		V
		$I_O = -100\ \mu A$		25°C	4.85	4.94		
				Full range	4.82			
		$I_O = -400\ \mu A$		25°C	4.7	4.85		
				Full range	4.6			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_O = 50\ \mu A$	25°C		−4.99		V
		$V_{IC} = 0$,	$I_O = 500\ \mu A$	25°C	−4.85	−4.91		
				Full range	−4.85			
		$V_{IC} = 0$,	$I_O = 1$ mA	25°C	−4.7	−4.8		
				Full range	−4.7			
		$V_{IC} = 0$,	$I_O = 4$ mA	25°C	−4	−4.3		
				Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 50\ k\Omega$	25°C	80	200		V/mV
				Full range	55			
			$R_L = 1\ M\Omega$	25°C		1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$	25°C		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$,	$R_S = 50\ \Omega$	25°C	75	88		dB
				Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = 0$,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$,	No load	25°C		0.85	1	mA
				Full range			1	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm1.9$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, f = 20 kHz, $R_L = 50$ kΩ	$A_V = 1$	25°C		0.014%		
			$A_V = 10$			0.024%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		70		kHz
t_s	Settling time	$A_V = -1$, Step = –2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1		µs
			To 0.01%			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.

TLC2262I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				85°C			150			150	
				Full range			800			800	pA
I_{IB}	Input bias current			25°C		1			1		pA
				85°C			150			150	pA
				Full range			800			800	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$,	$\|V_{IO}\| \leq 5$ mV	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = –20$ µA		25°C		4.99			4.99		V
		$I_{OH} = –100$ µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		$I_{OH} = –400$ µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50$ µA	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 500$ µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		$V_{IC} = 2.5$ V,	$I_{OL} = 4$ mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 50$ kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			$R_L = 1$ MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $R_S = 50\ \Omega$	$V_O = 2.5$ V,	25°C	70	83		70	83		dB
				Full range	70			70			

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	µA
				Full range			500			500	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

TLC2262I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I MIN	TLC2262I TYP	TLC2262I MAX	TLC2262AI MIN	TLC2262AI TYP	TLC2262AI MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				85°C			150			150	pA
				Full range			800			800	pA
I_{IB}	Input bias current			25°C		1			1		pA
				85°C			150			150	pA
				Full range			800			800	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\|V_{IO}\| \le 5$ mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$		25°C		4.99			4.99		V
		$I_O = -100\ \mu A$		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		$I_O = -400\ \mu A$		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$		25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA		25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V	$R_L = 50\ k\Omega$	25°C	80	200		80	200		V/mV
				Full range	50			50			
			$R_L = 1\ M\Omega$	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$		25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	88		75	88		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply Current	V_O = 2.5 V,	No load	25°C		425	500		425	500	
				Full range			500			500	
SR	Slew rate at unity gain	V_O = ±1.9 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		85			85		kHz
t_s	Settling time	A_V = –1, Step = –2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C.

TLC2264I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$,	$\lvert V_{IO}\rvert \le 5$ mV	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20$ µA		25°C		4.99			4.99		V
		$I_{OH} = -100$ µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		$I_{OH} = -400$ µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50$ µA	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 500$ µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		$V_{IC} = 2.5$ V,	$I_{OL} = 4$ mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 50$ kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			$R_L = 1$ MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $R_S = 50\ \Omega$	$V_O = 2.5$ V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	V/µs
				Full range			1			1	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

TLC2264I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264I			TLC2264AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			85°C			150			150	
			Full range			800			800	
I_{IB}	Input bias current		25°C		1			1		pA
			85°C			150			150	pA
			Full range			800			800	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO}\rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 50\ k\Omega$	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$V_O = \pm 4$ V, $R_L = 1\ M\Omega$	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	$V_O = 0$,	No load	25°C		0.85	1		0.85	1	mA
				Full range			1			1	
SR	Slew rate at unity gain	$V_O = \pm 1.9$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.014%			0.014%		
			$A_V = 10$			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		70			70		kHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1			7.1		μs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C.

TLC2262Q/M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262Q, TLC2262M MIN	TLC2262Q, TLC2262M TYP	TLC2262Q, TLC2262M MAX	TLC2262AQ, TLC2262AM MIN	TLC2262AQ, TLC2262AM TYP	TLC2262AQ, TLC2262AM MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		5			5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −100 µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	µA
				Full range			500			500	

† Full range is −40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262Q/M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.
‡ Referenced to 2.5 V

TLC2262Q/M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		5			5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV		25°C	−5 to 4	−5.3 to 4		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −100 µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_O = −400 µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA		25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 4 mA		25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 50 kΩ	25°C	80	200		80	200		V/mV
				Full range	50			50			
			R_L = 1 MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω		25°C	75	88		75	88		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load		25°C		425	500		425	500	µA
				Full range			500			500	

† Full range is −40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262Q/M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262Q, TLC2262M MIN	TYP	MAX	TLC2262AQ, TLC2262AM MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.014%			0.014%		
			$A_V = 10$			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		85			85		kHz
t_s	Settling time	$A_V = -1$, Step = –2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

TLC2264Q/M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264Q, TLC2264M MIN	TYP	MAX	TLC2264AQ, TLC2264AM MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			800			800	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\|$ ≤5 mV	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = –20 μA	25°C		4.99			4.99		V
		I_{OH} = –100 μA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		I_{OH} = –400 μA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
			Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
			Full range	50			50			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V,	25°C	80	95		80	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264Q/M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264Q, TLC2264M MIN	TLC2264Q, TLC2264M TYP	TLC2264Q, TLC2264M MAX	TLC2264AQ, TLC2264AM MIN	TLC2264AQ, TLC2264AM TYP	TLC2264AQ, TLC2264AM MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.
‡ Referenced to 2.5 V

TLC2264Q/M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264Q, TLC2264M MIN	TYP	MAX	TLC2264AQ, TLC2264AM MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			800			800	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			800			800	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 50\ k\Omega$	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$V_O = \pm4$ V, $R_L = 1\ M\Omega$	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.85	1		0.85	1	mA
			Full range			1			1	

† Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264Q/M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2$ V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		70			70		kHz
t_s	Settling time	$A_V = -1$, Step = –2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

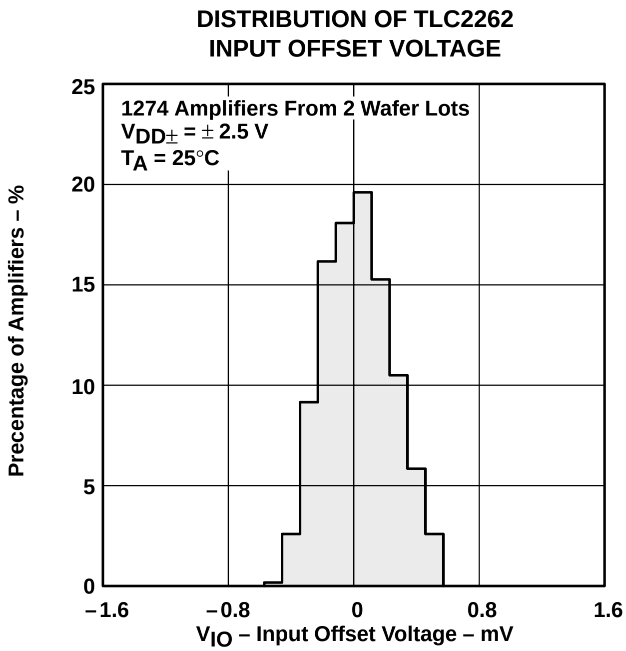


Figure 2

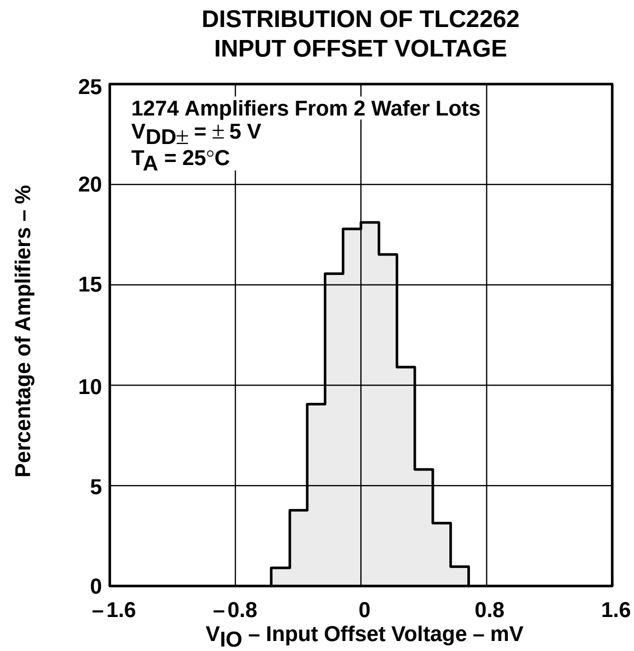


Figure 3

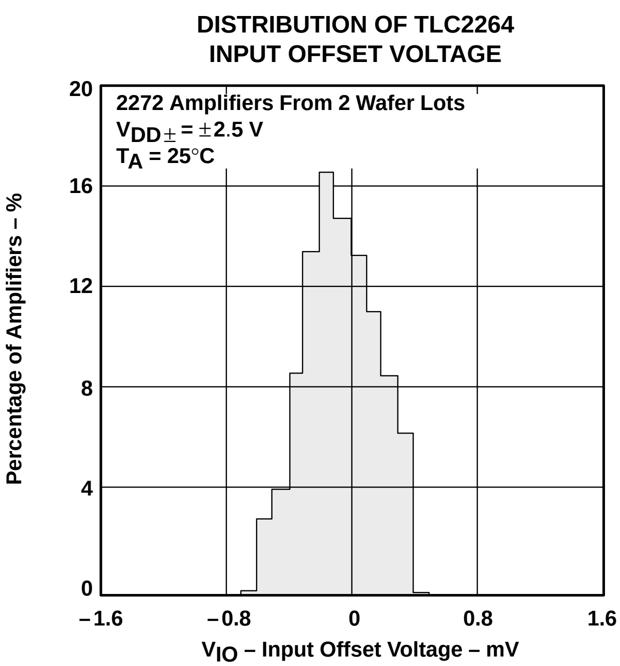


Figure 4

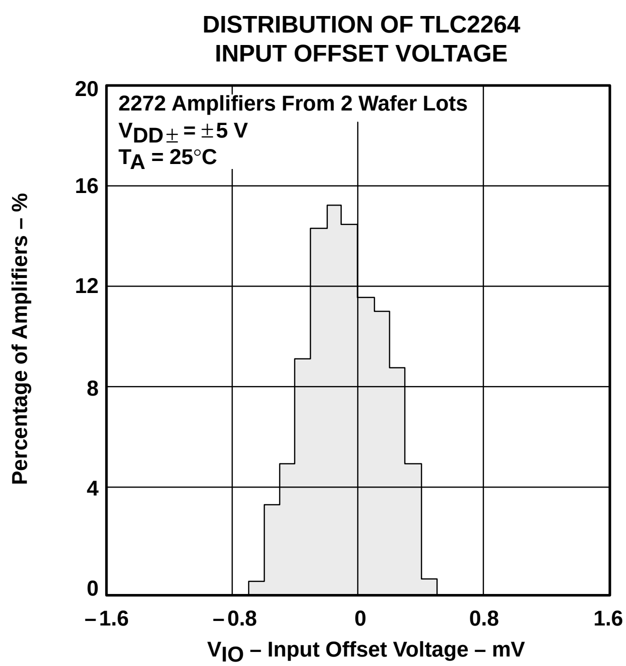
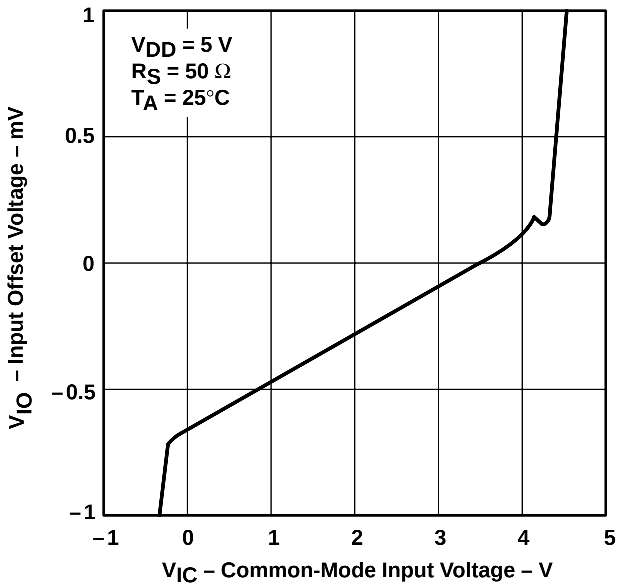


Figure 5

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 6

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

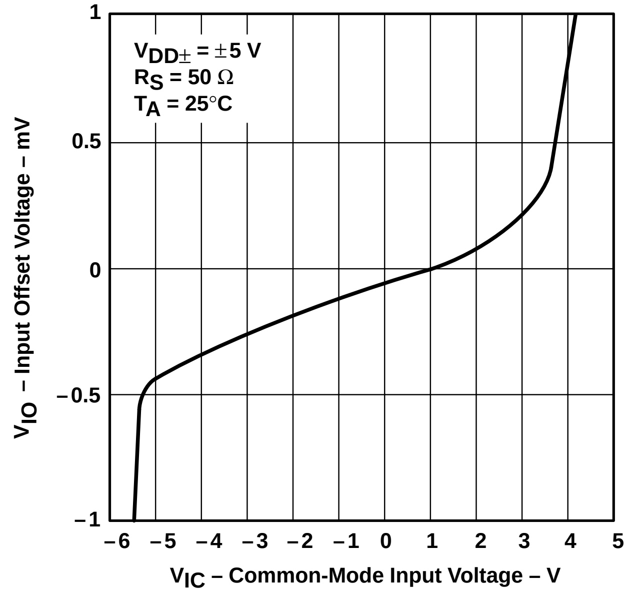


Figure 7

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

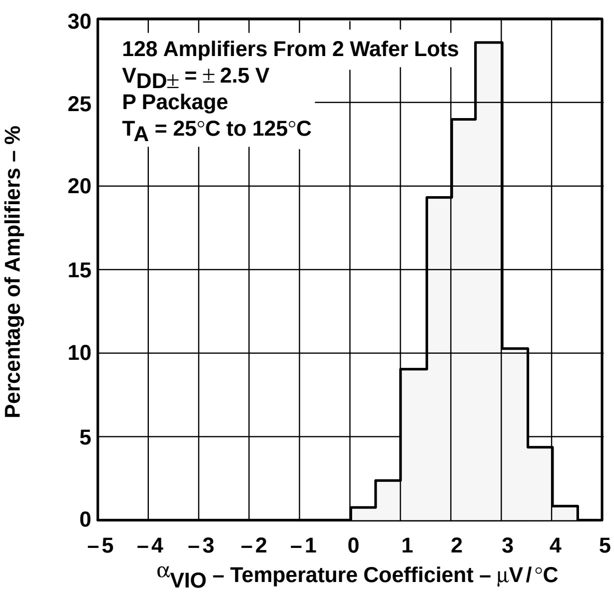


Figure 8

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

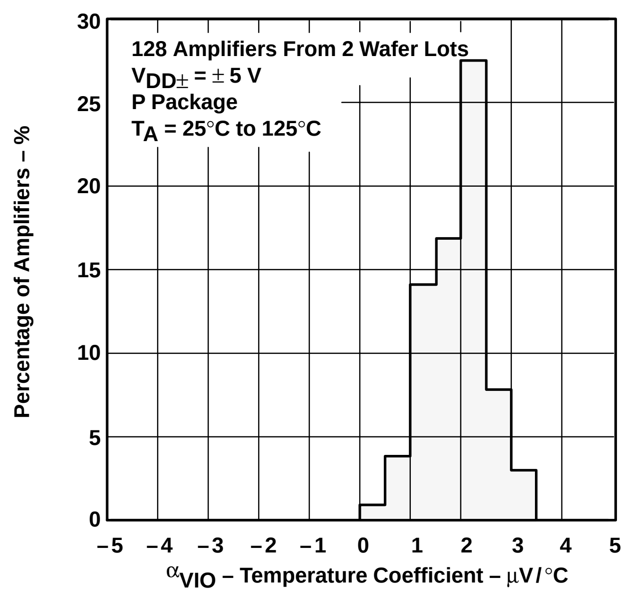


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

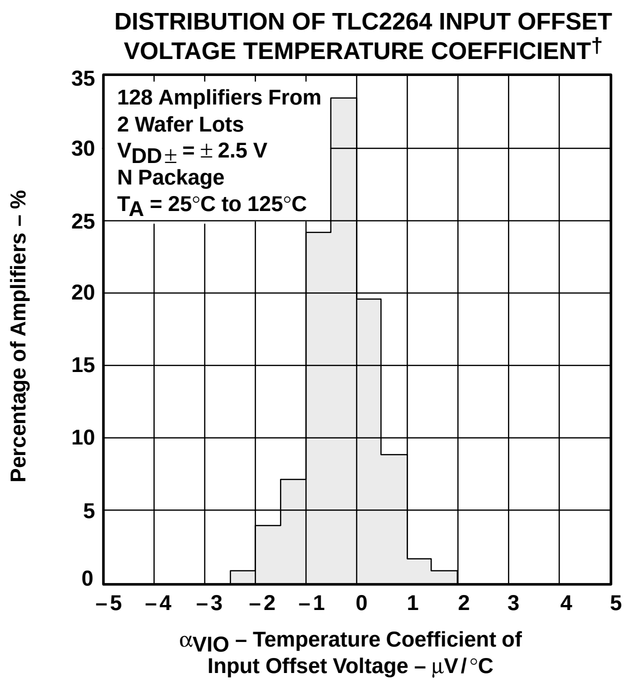


Figure 10

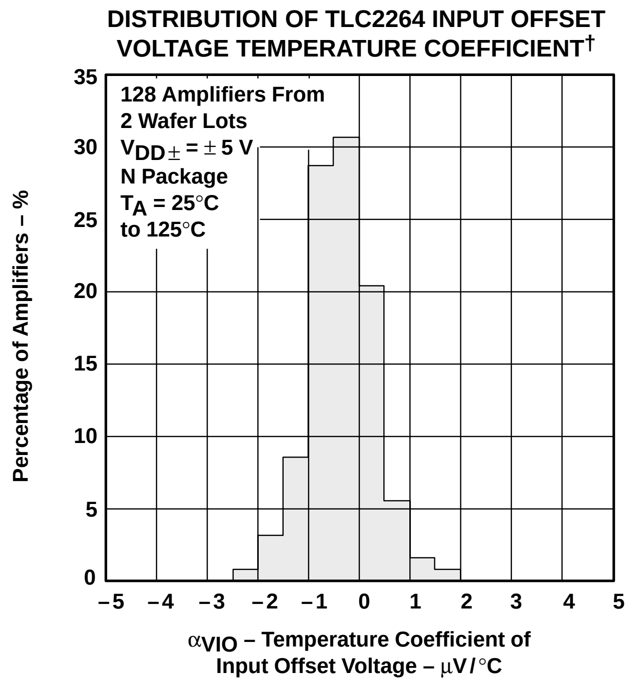


Figure 11

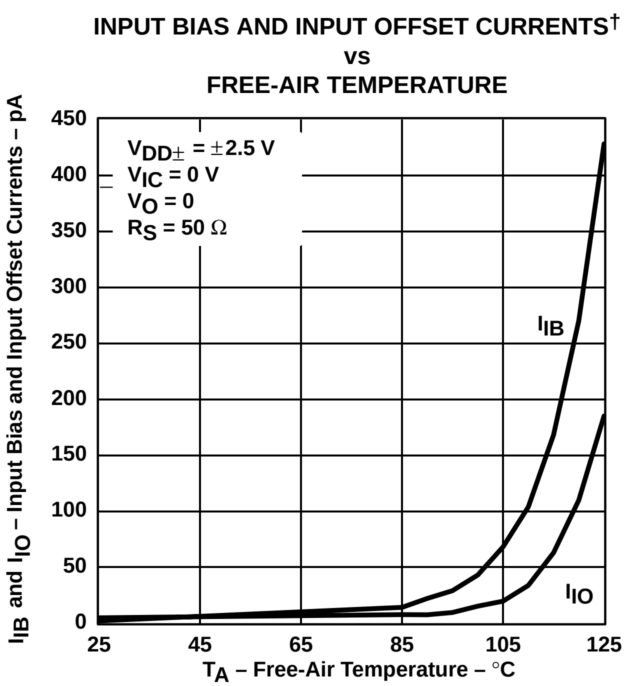


Figure 12

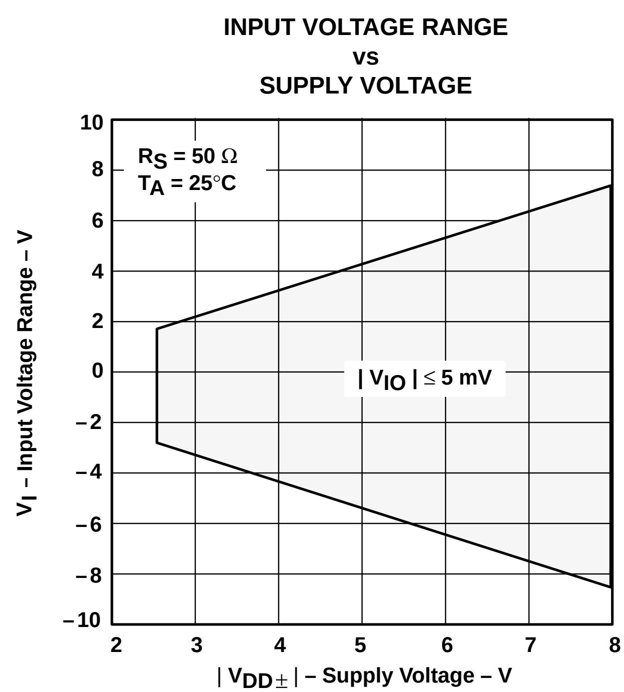


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE†‡
vs
FREE-AIR TEMPERATURE

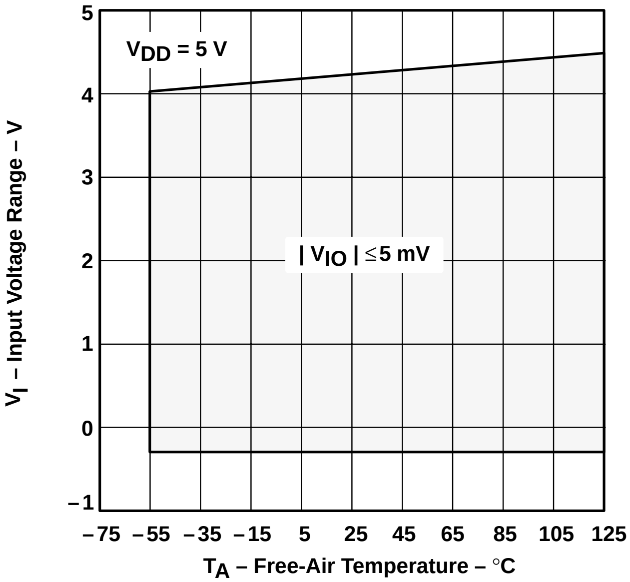


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

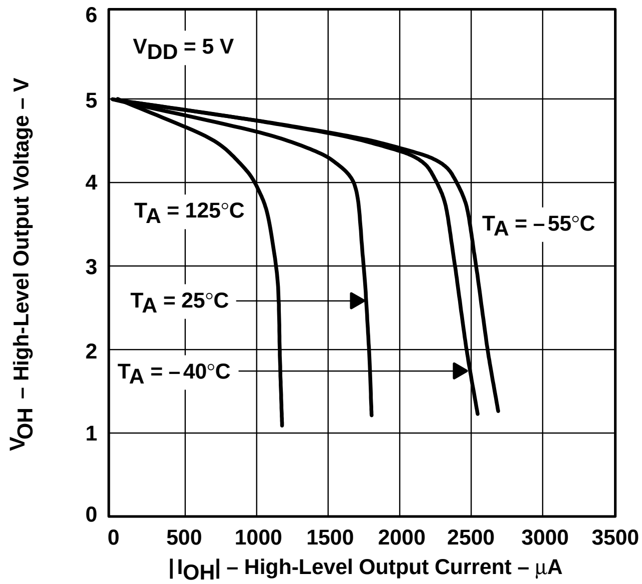


Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

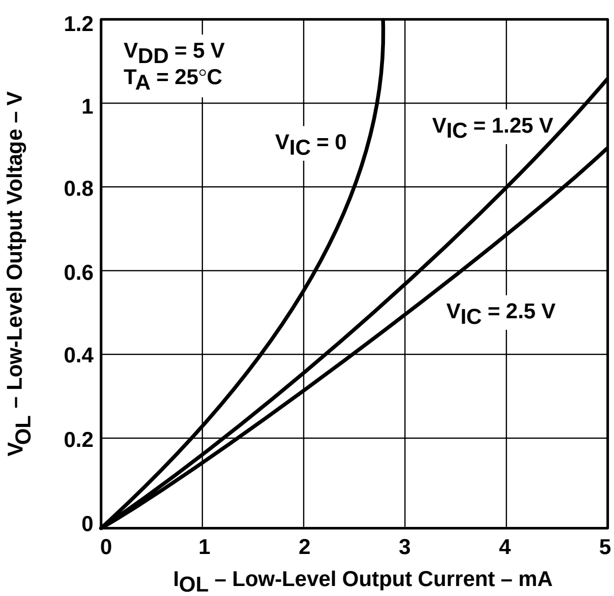


Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

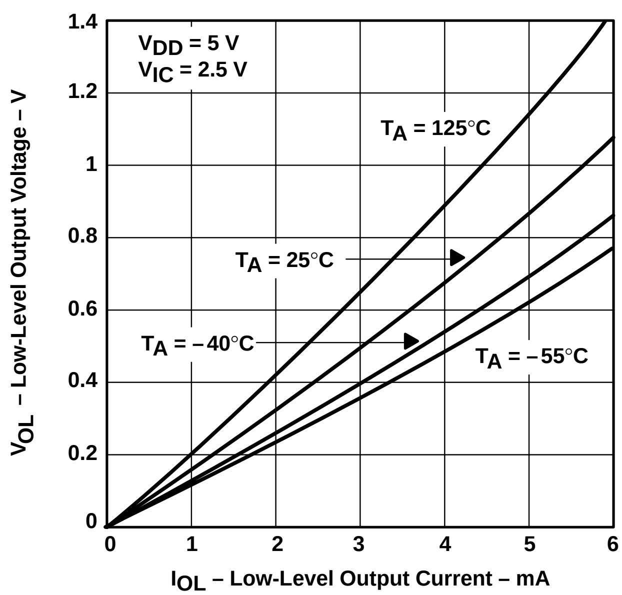


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE†
vs
OUTPUT CURRENT

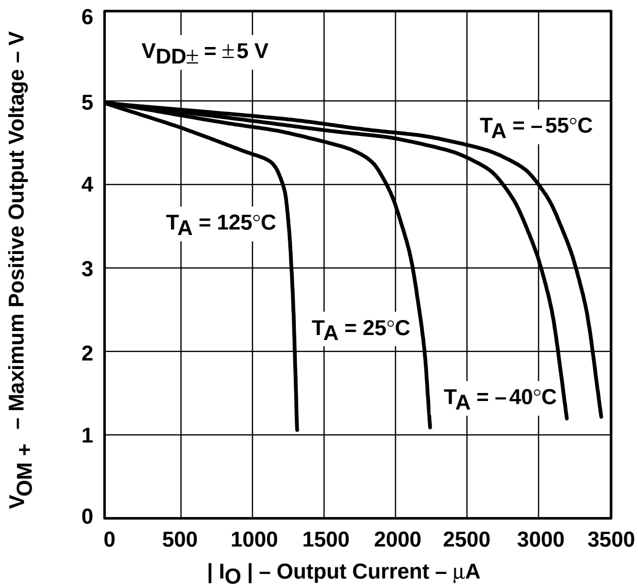


Figure 18

MAXIMUM NEGATIVE OUTPUT VOLTAGE†
vs
OUTPUT CURRENT

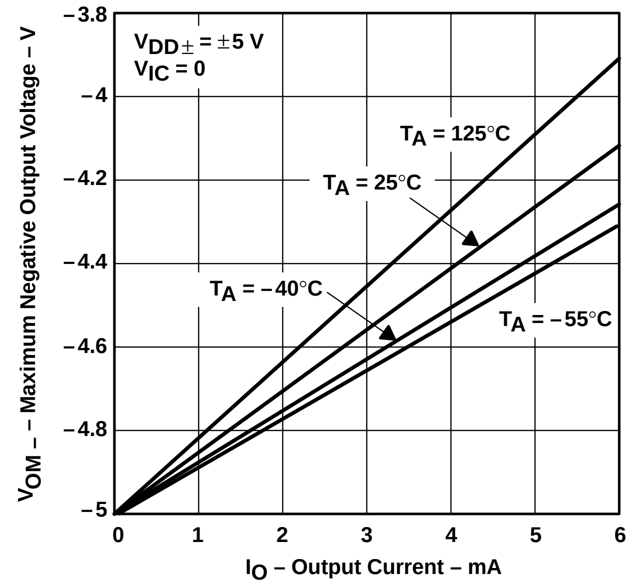
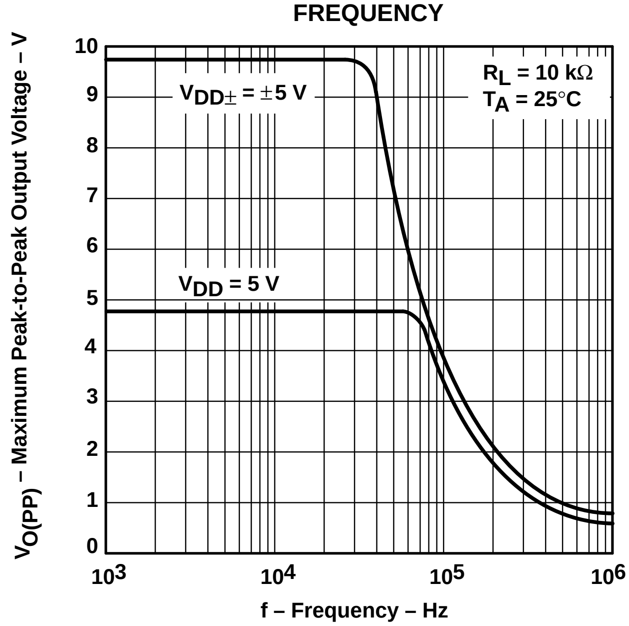


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†‡
vs
FREQUENCY



‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

Figure 20

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

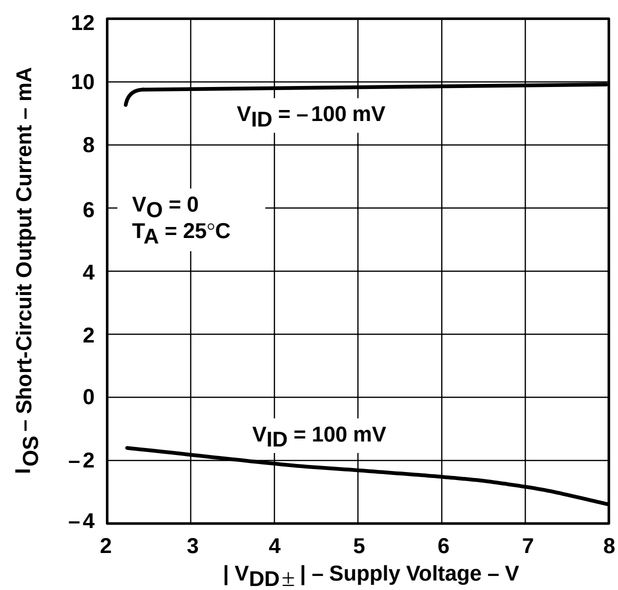


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

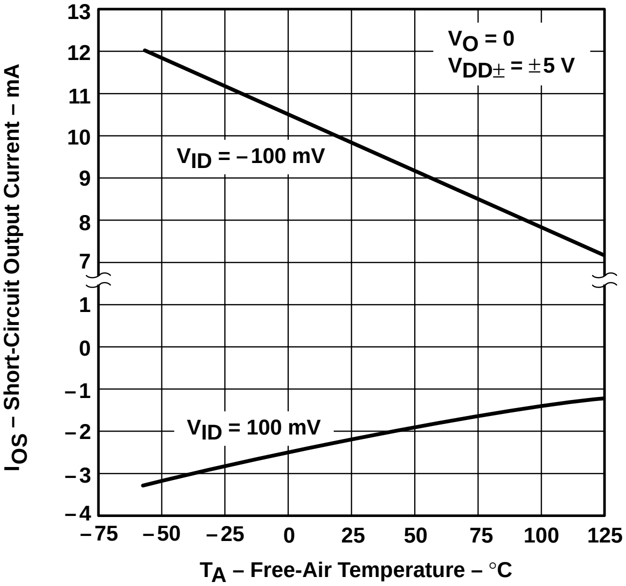


Figure 22

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

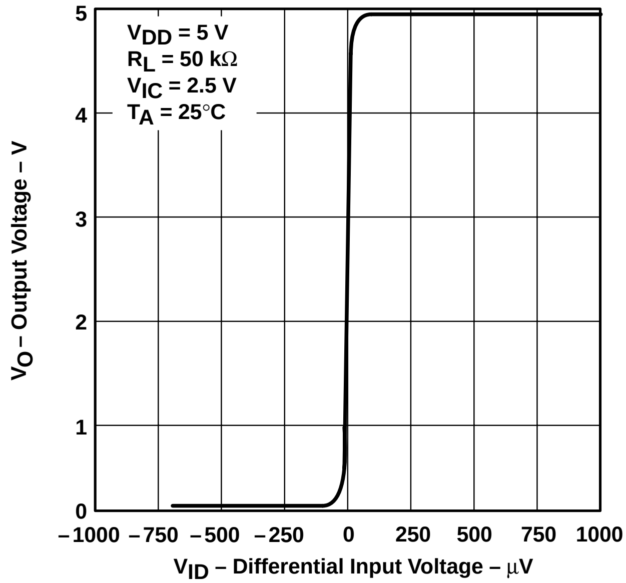


Figure 23

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

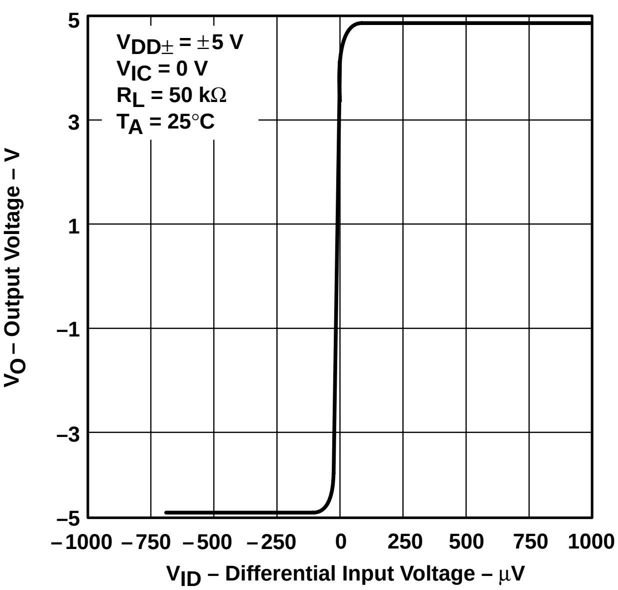


Figure 24

DIFFERENTIAL GAIN‡
vs
LOAD RESISTANCE

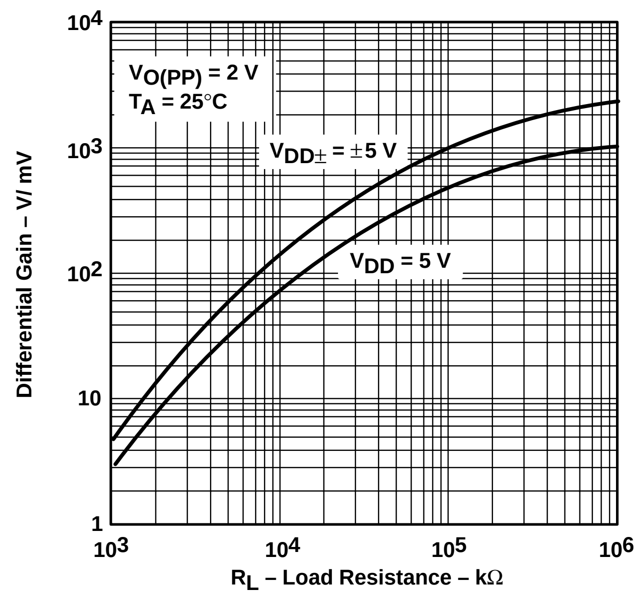
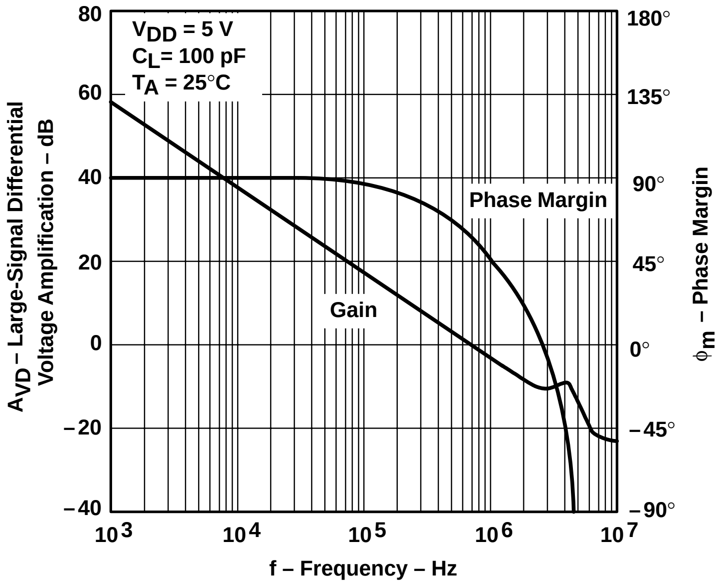


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

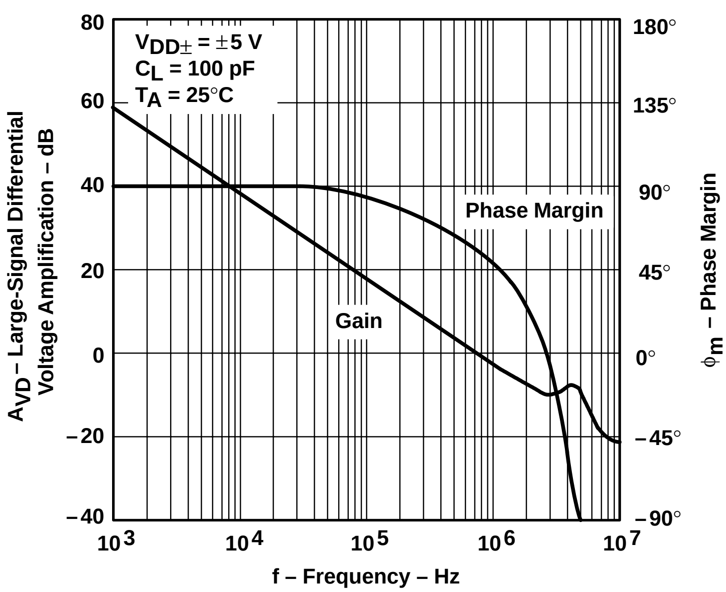


Figure 27

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

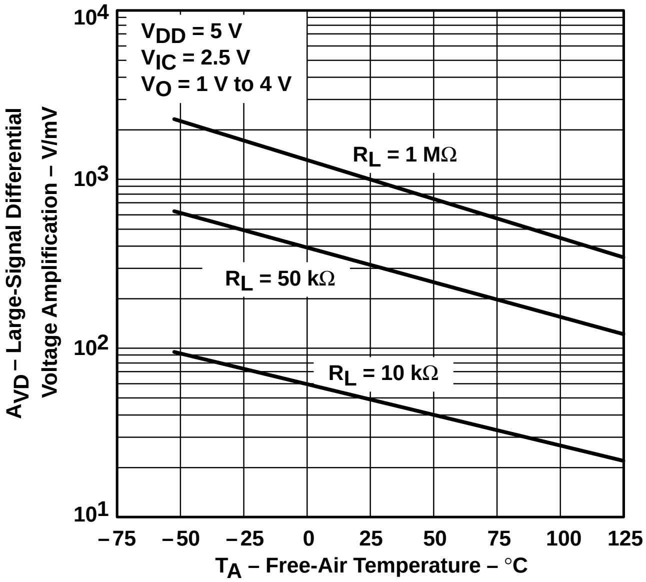


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

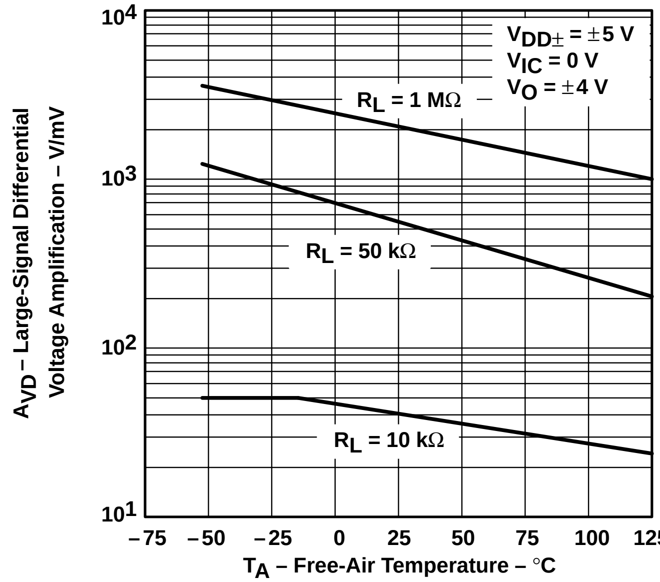


Figure 29

OUTPUT IMPEDANCE‡ vs FREQUENCY

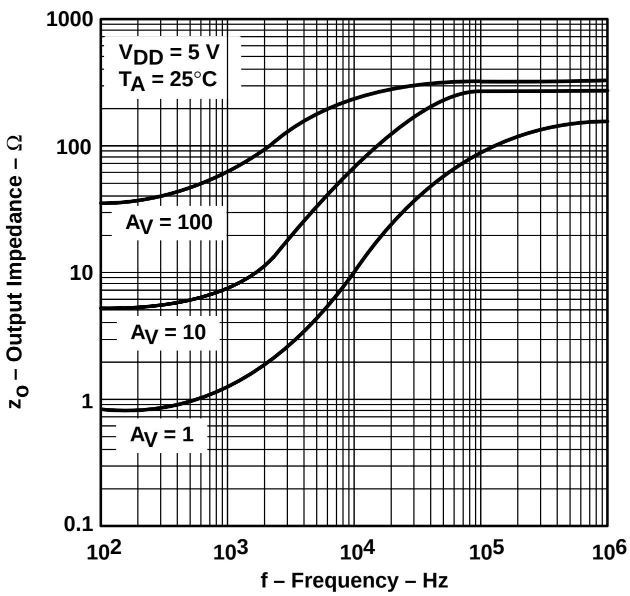


Figure 30

OUTPUT IMPEDANCE vs FREQUENCY

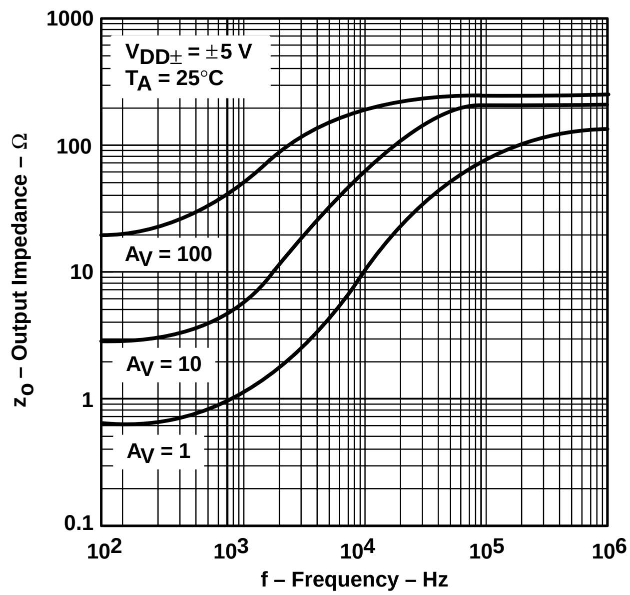


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO† vs FREQUENCY

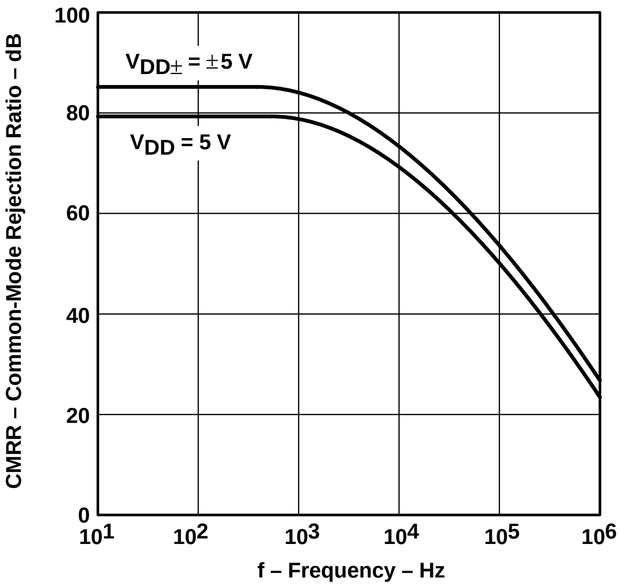


Figure 32

COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE

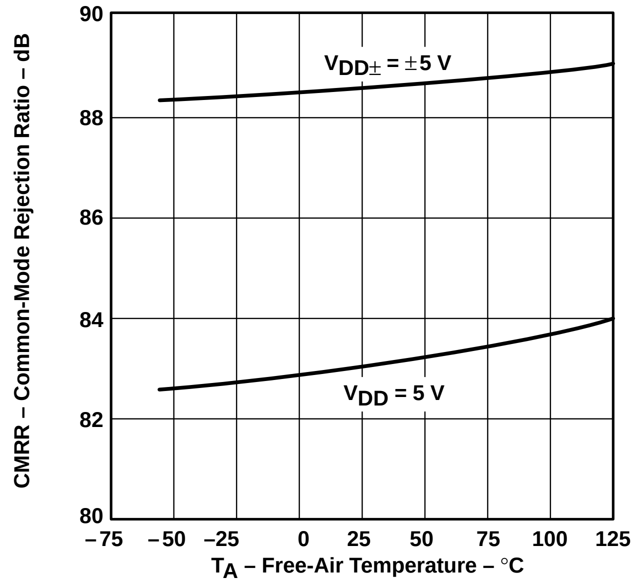


Figure 33

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

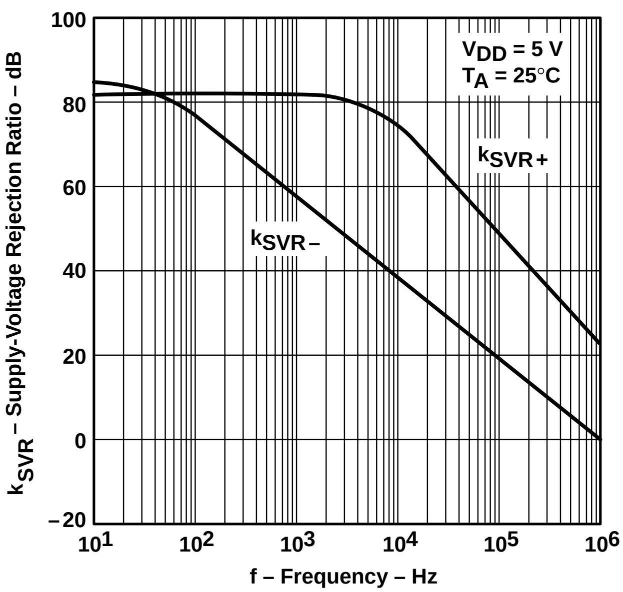


Figure 34

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

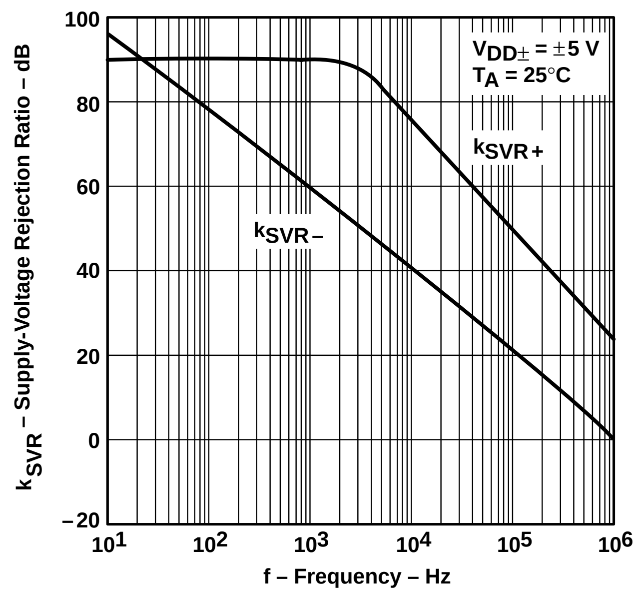


Figure 35

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

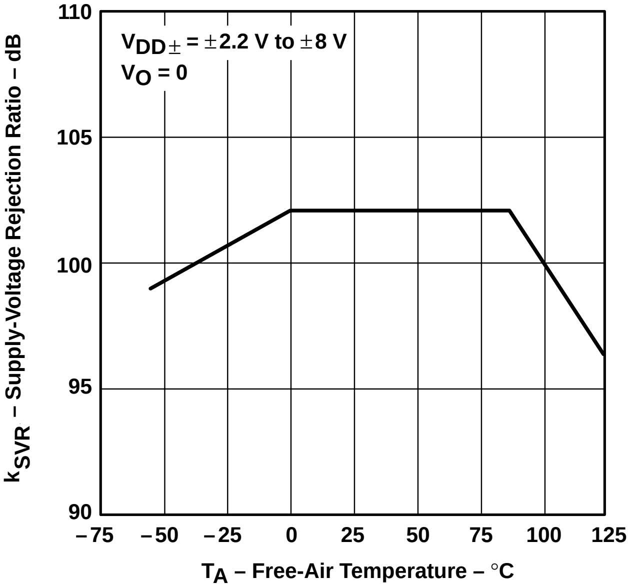


Figure 36

TLC2262
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

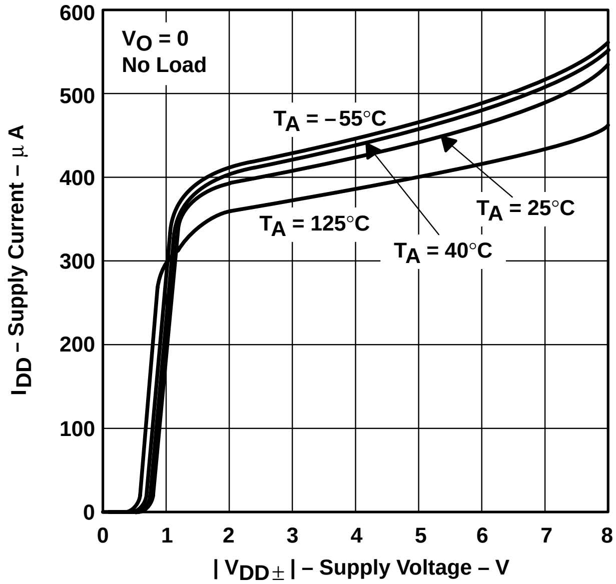


Figure 37

TLC2264
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

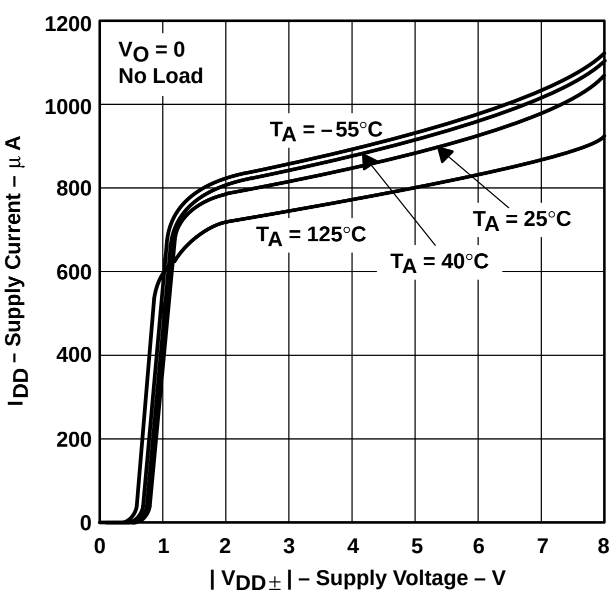


Figure 38

TLC2262
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

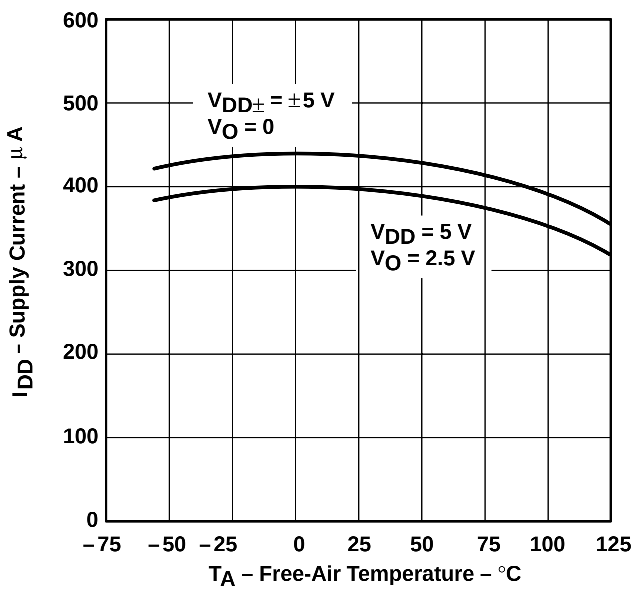


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

TLC2264
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

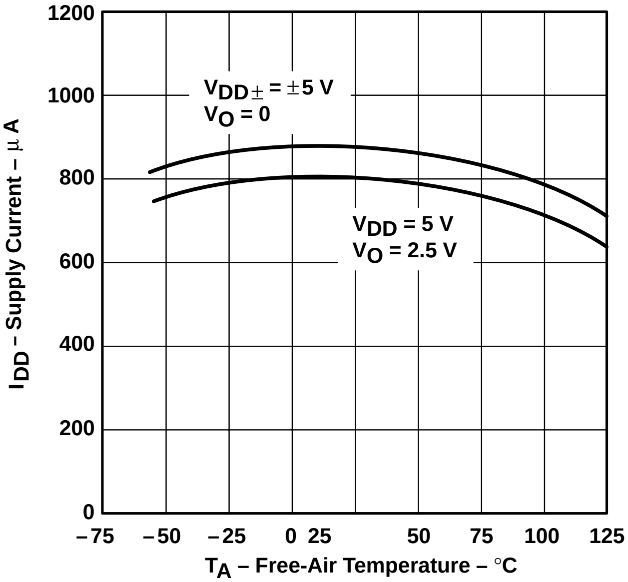


Figure 40

SLEW RATE‡
vs
LOAD CAPACITANCE

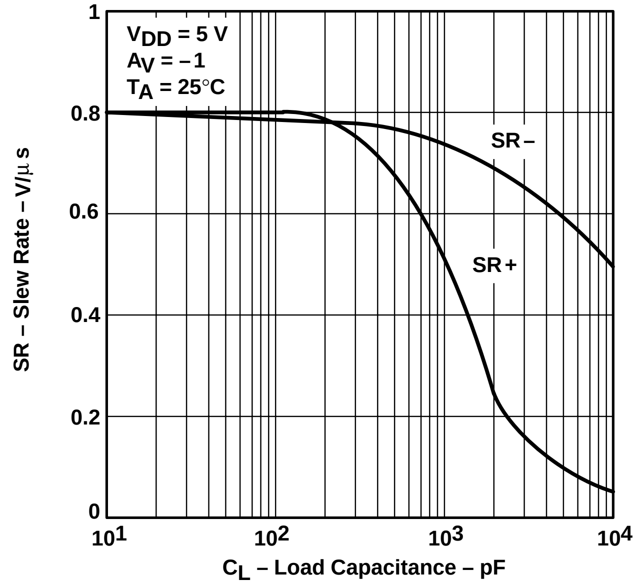


Figure 41

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

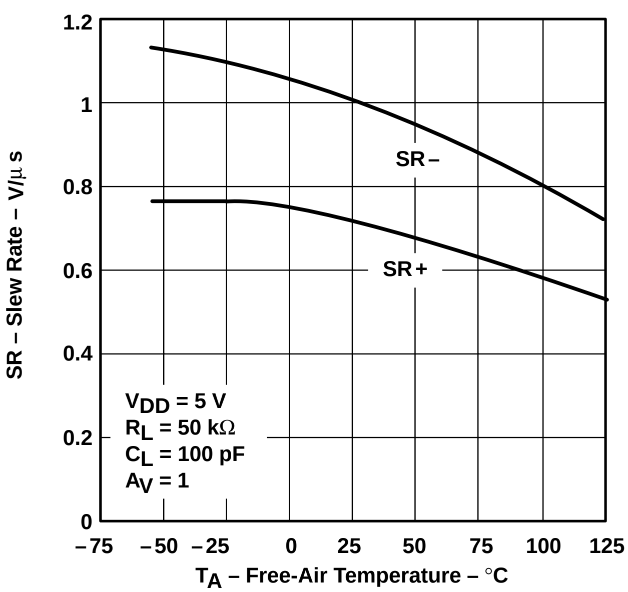


Figure 42

INVERTING LARGE-SIGNAL PULSE
RESPONSE‡

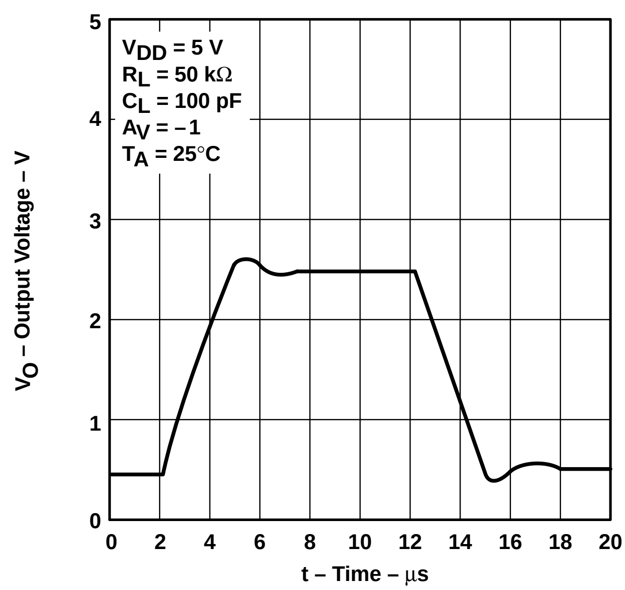


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

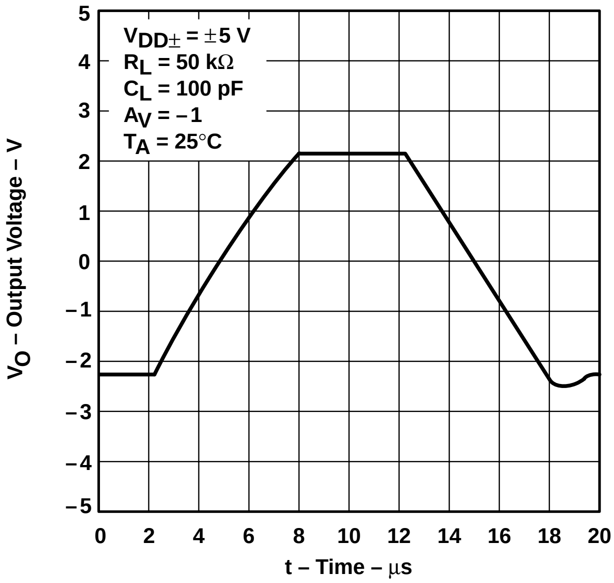


Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

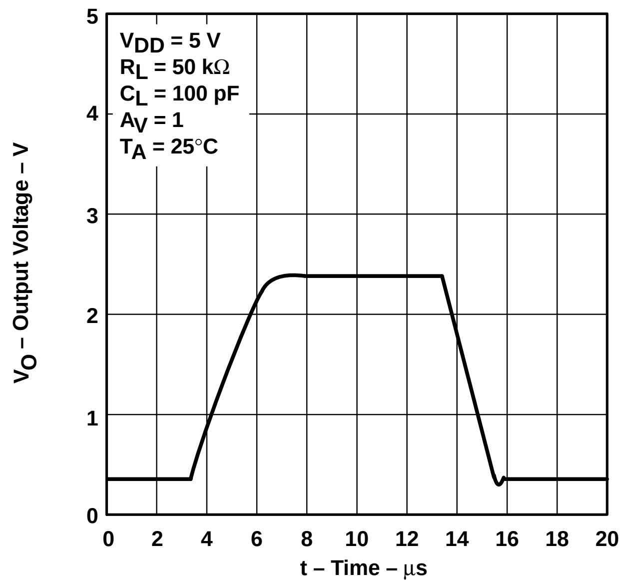


Figure 45

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

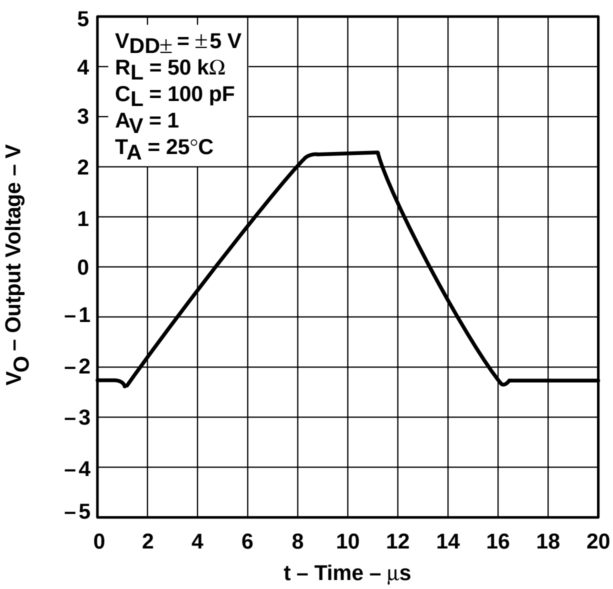


Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†

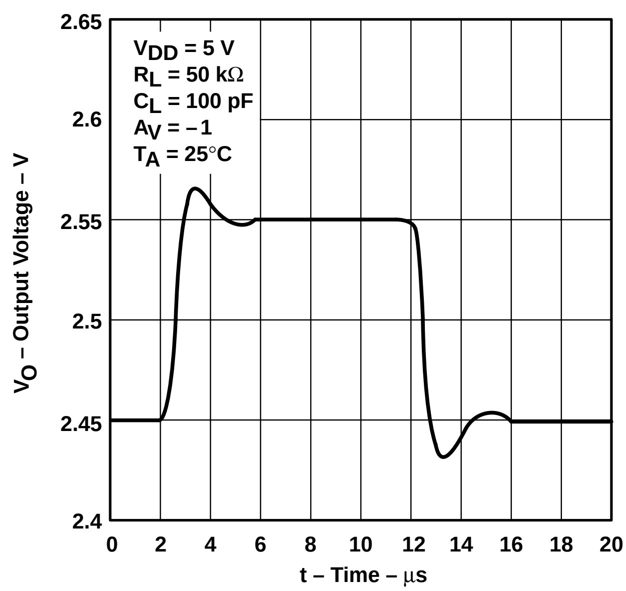


Figure 47

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL
PULSE RESPONSE

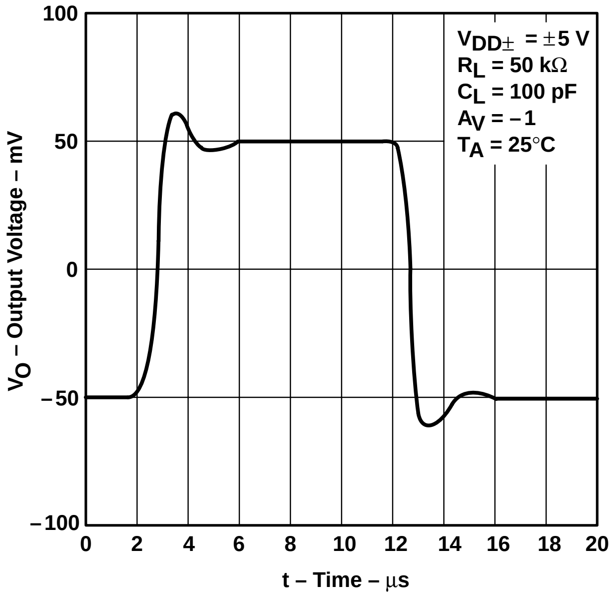


Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

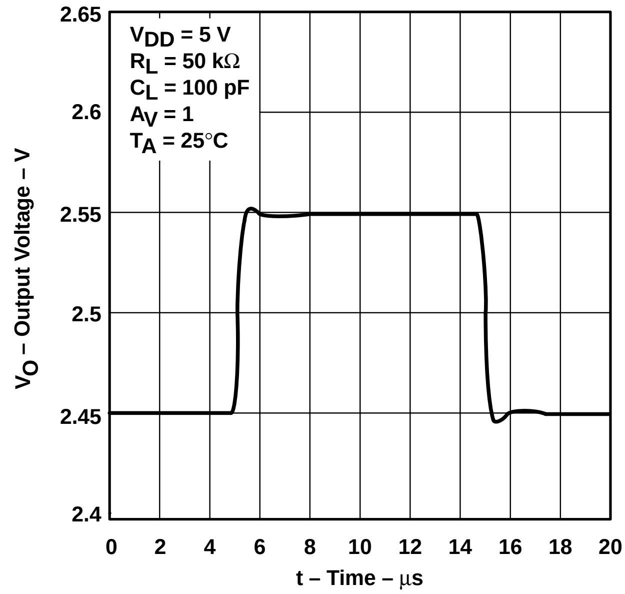


Figure 49

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

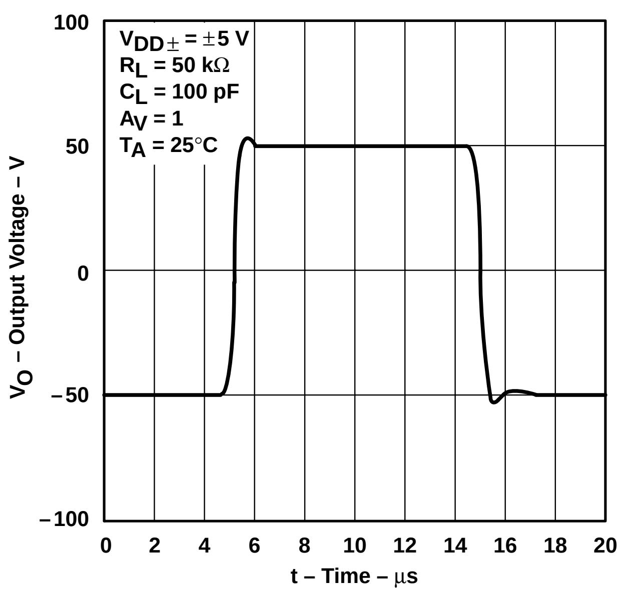


Figure 50

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

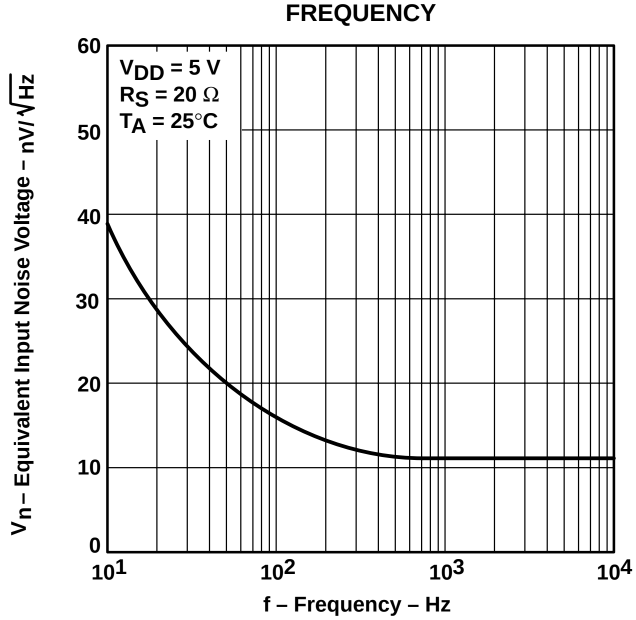


Figure 51

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

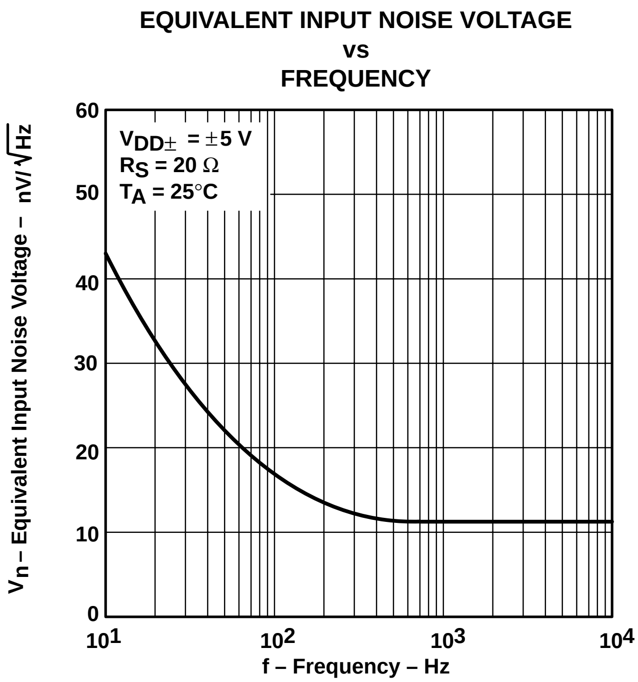


Figure 52

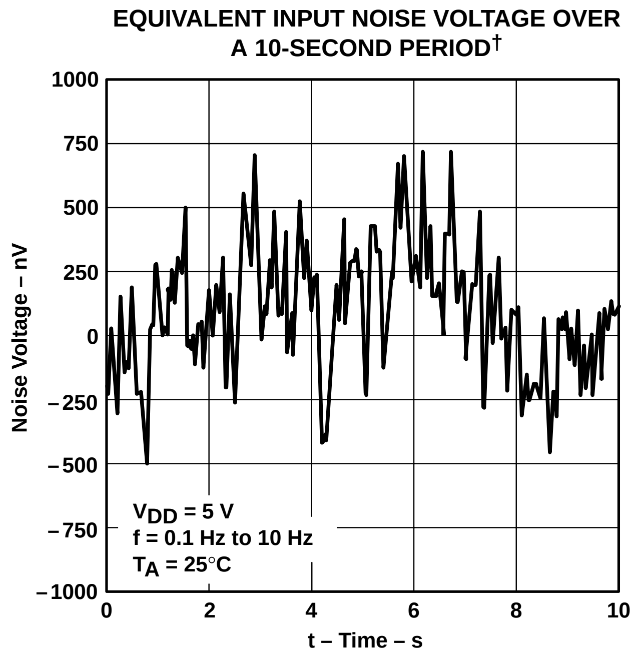


Figure 53

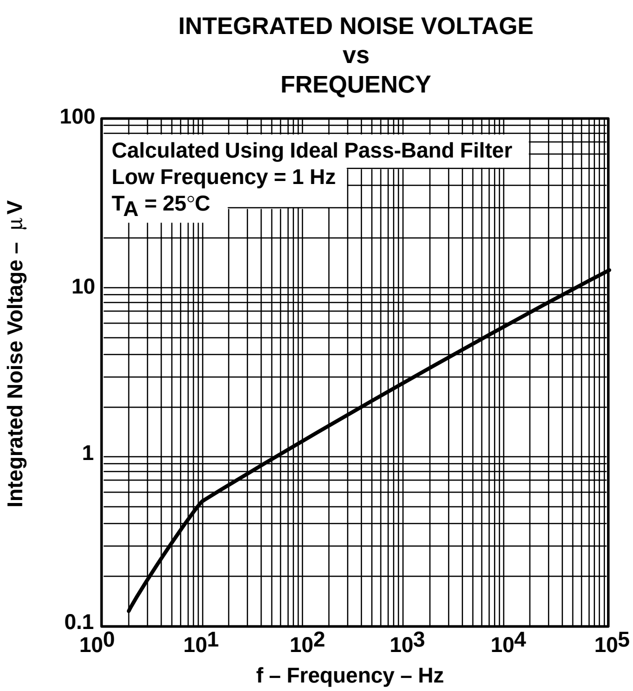


Figure 54

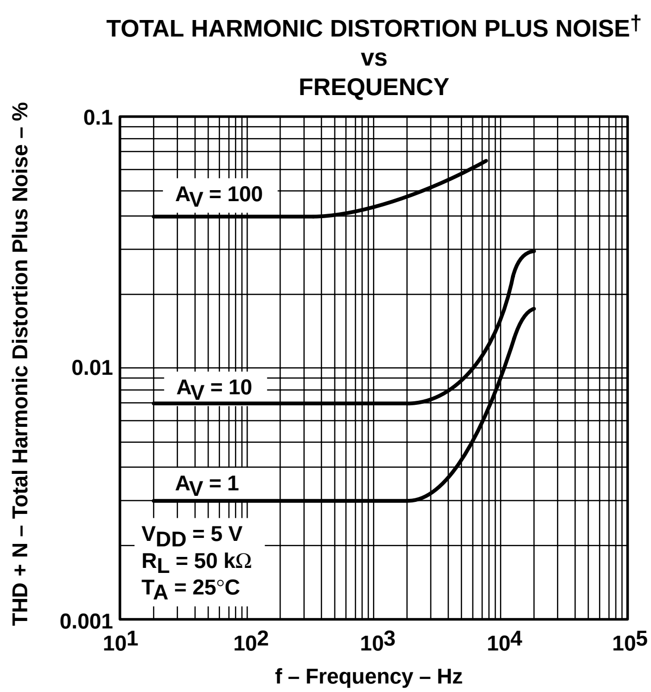


Figure 55

† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

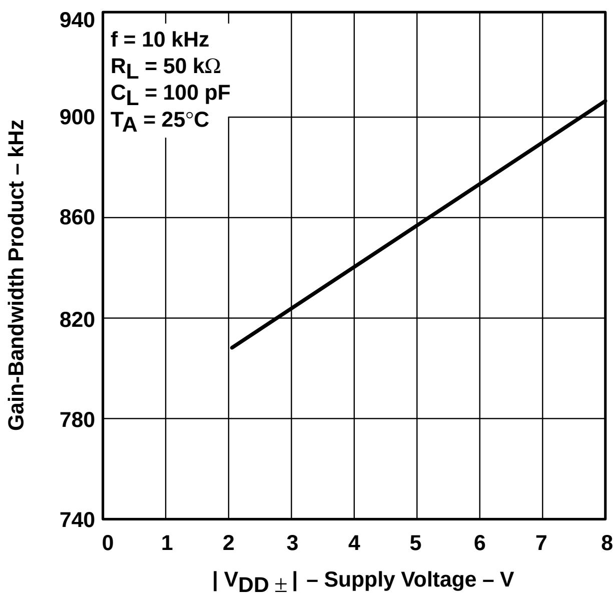


Figure 56

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

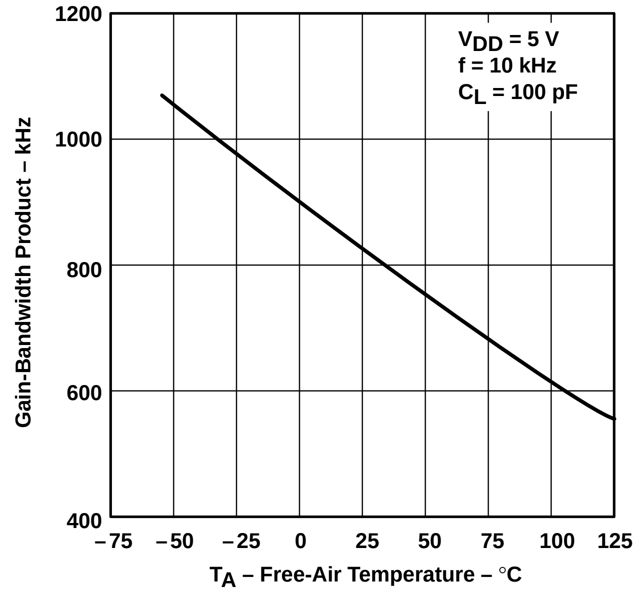


Figure 57

PHASE MARGIN
vs
LOAD CAPACITANCE

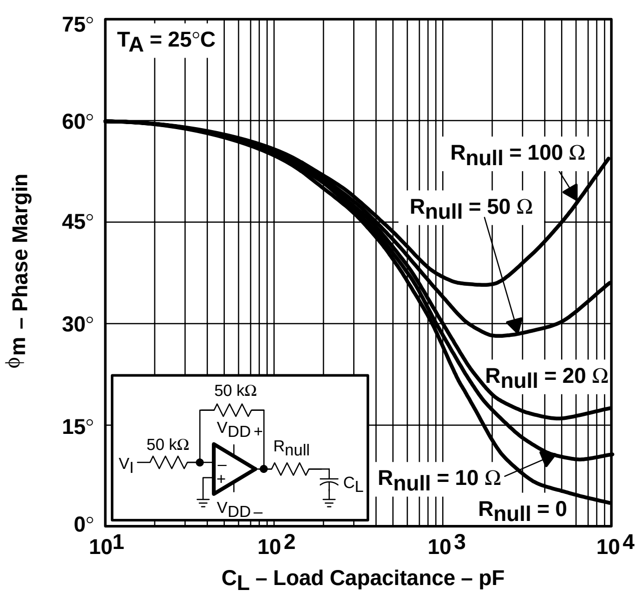


Figure 58

GAIN MARGIN
vs
LOAD CAPACITANCE

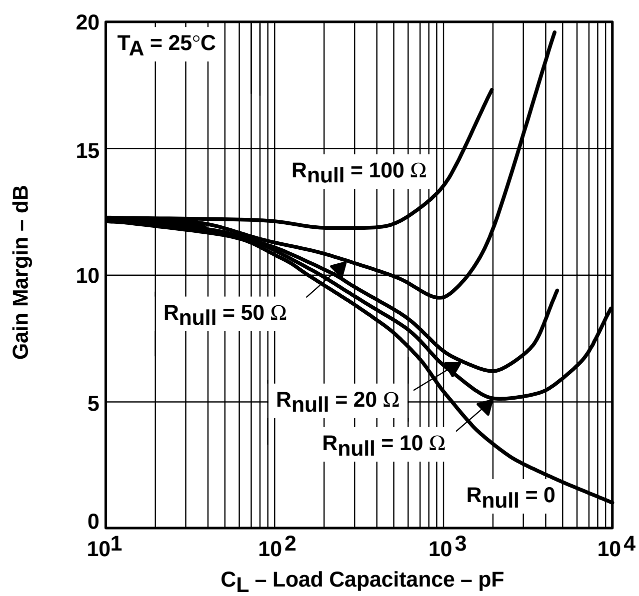


Figure 59

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH†
vs
LOAD CAPACITANCE

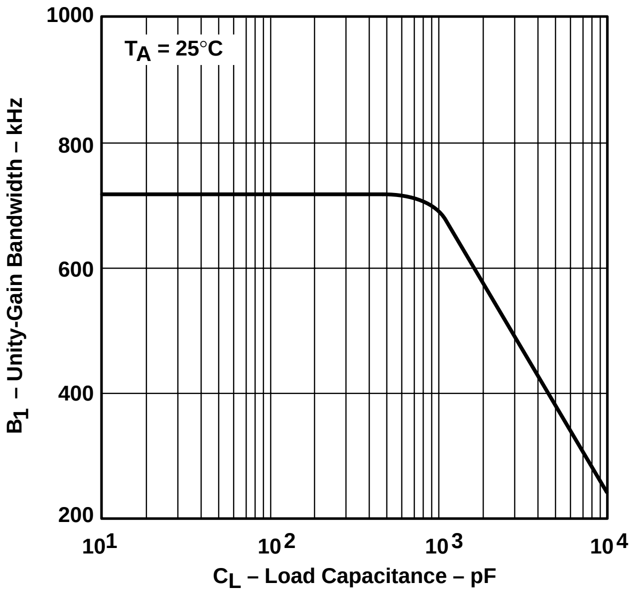


Figure 60

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE

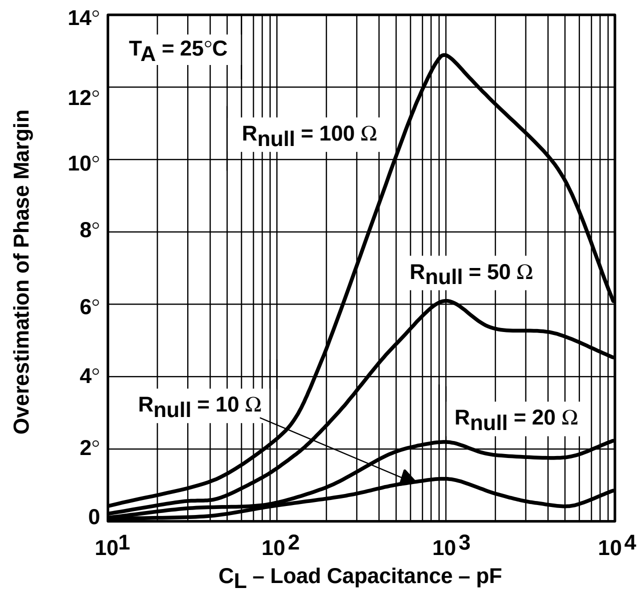


Figure 61

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 58 and Figure 59 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 62) improves the gain and phase margins when driving large capacitive loads. Figure 58 and Figure 59 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\Theta_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \tag{1}$$

Where :

$\Delta\Theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 60). To use equation 1, UGBW must be approximated from Figure 60.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 61. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \tag{2}$$

Where :

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

For the TLC226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 70 MHz, at C_L = 1000 pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation in equation 1 to better approximate the improvement in phase margin.

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\Theta_{m2} = \tan^{-1}\left[\frac{UGBW}{\left(F \times P_2\right)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \tag{3}$$

Where :

$\Delta\Theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation 2

P_2 = unadjusted pole (70 MHz@10 pF, 7 MHz@100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

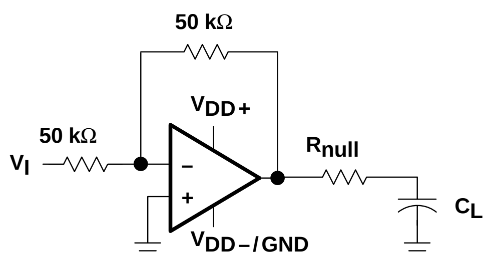


Figure 62. Series-Resistance Circuit

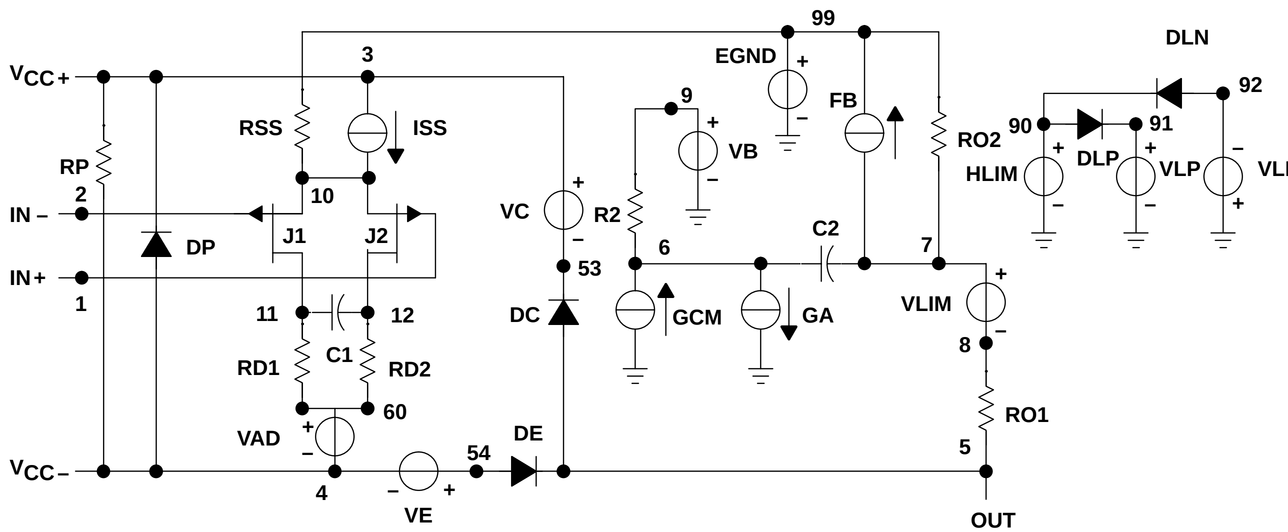
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 63 are generated using the TLC226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLC226x 1 2 3 4 5
        C1     11   12   3.560E–12
        C2     6    7    15.00E–12
        DC     5    53   DX
        DE     54   5    DX
        DLP    90   91   DX
        DLN    92   90   DX
        DP     4    3    DX
        EGND   99   0    POLY (2) (3,0) (4,0) 0 .5 .5
        FB     7    99   POLY (5) VB VC VE VLP
        + VLN 0 21.04E6 –30E6 30E6 30E6 –30E6
        GA     6    0    11   12 47.12E–6
        GCM    0    6    10   99 4.9E–9
        ISS    3    10   DC 8.250E–6
        HLIM   90   0    VLIM 1K
        J1     11   2    10 JX
        J2     12   1    10 JX
        R2     6    9    100.0E3
```

```
RD1    60   11   21.22E3
RD2    60   12   21.22E3
R01    8    5    120
R02    7    99   120
RP     3    4    26.04E3
RSS    10   99   24.24E6
VAD    60   4    –.6
VB     9    0    DC 0
VC     3    53   DC .65
VE     54   4    DC .65
VLIM   7    8    DC 0
VLP    91   0    DC 1.4
VLN    0    92   DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=281E–6
+ VTO=–.065)
.ENDS
```

Figure 63. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-9469201Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9469201QHA	ACTIVE	CFP	U	10	1	TBD	Call TI	Call TI	
5962-9469201QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-9469202Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9469202QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-9469202QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
5962-9469203Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9469203QHA	ACTIVE	CFP	U	10	1	TBD	Call TI	Call TI	
5962-9469203QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-9469204Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9469204QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-9469204QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
TLC2262AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2262AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2262AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AIPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC2262AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC2262AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2262AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC2262AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC2262AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	
TLC2262AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TLC2262AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2262CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2262CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC2262CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC2262ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2262IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2262MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2262MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC2262MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	
TLC2262QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262QDG4	ACTIVE	SOIC	D	8	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2262QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2264AINE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC2264AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AIPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
TLC2264AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2264AMJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
TLC2264AMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
TLC2264AMWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
TLC2264AQD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AQDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264AQDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
TLC2264AQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2264CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2264CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC2264CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
TLC2264CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2264INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC2264MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC2264MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
TLC2264MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
TLC2264QD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
TLC2264QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC2264QDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
TLC2264QDRG4	ACTIVE	SOIC	D	14	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC2262, TLC2262A, TLC2262AM, TLC2262M, TLC2264, TLC2264A, TLC2264AM, TLC2264M :

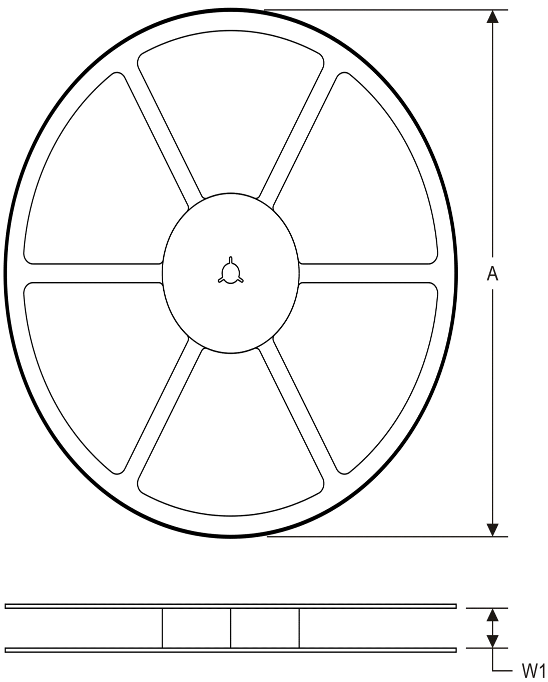
- Catalog: TLC2262A, TLC2262, TLC2264A, TLC2264
- Automotive: TLC2264A-Q1, TLC2264A-Q1
- Military: TLC2262M, TLC2262AM, TLC2264M, TLC2264AM

NOTE: Qualified Version Definitions:

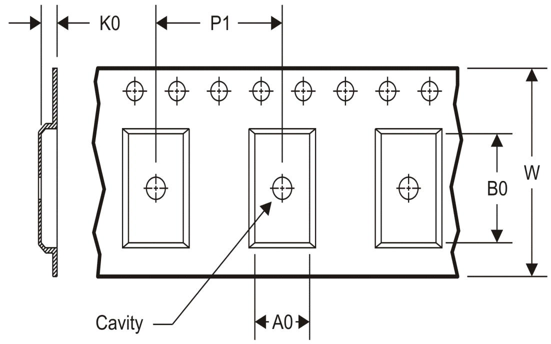
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



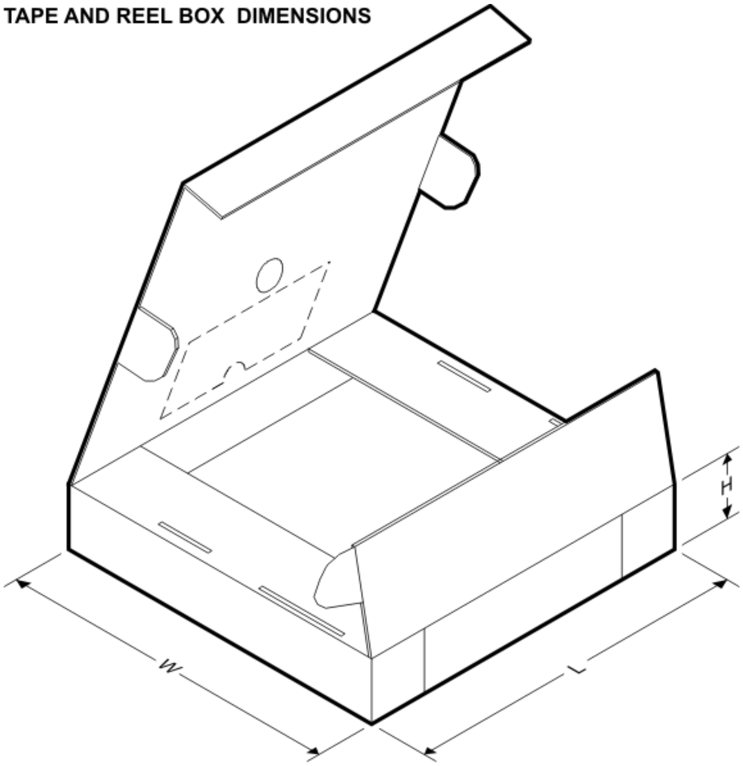
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2262AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2264AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

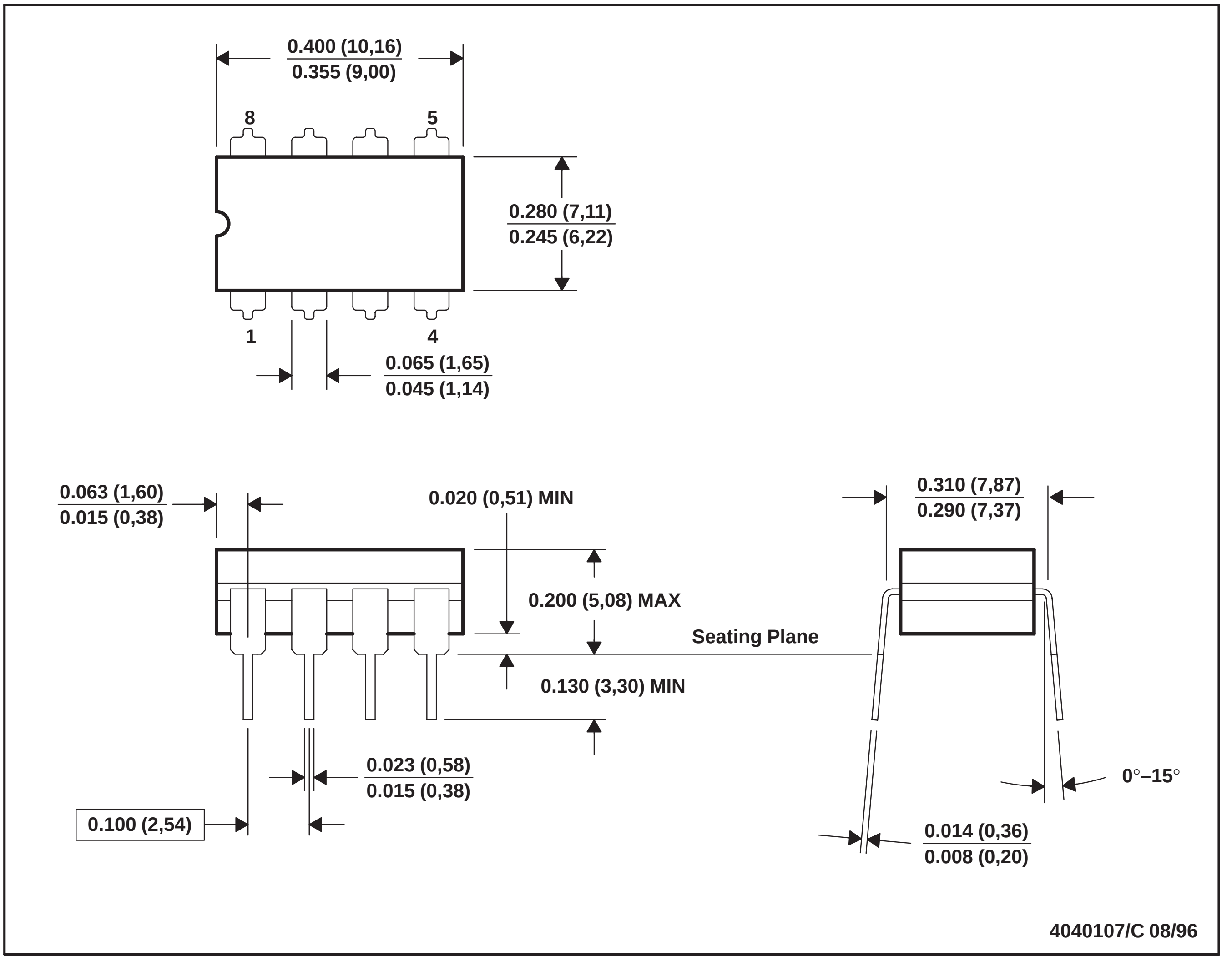
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2262AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2262AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2262CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2262CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2262IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2264AIDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2264AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2264CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2264CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2264IDR	SOIC	D	14	2500	333.2	345.9	28.6

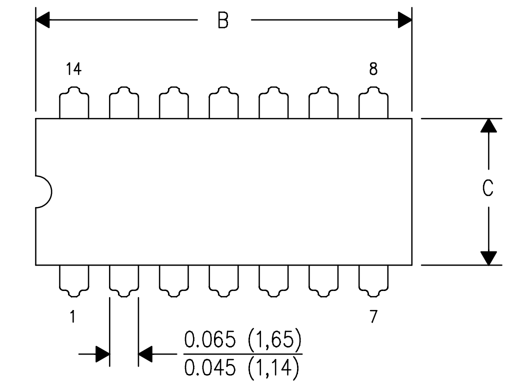
JG (R-GDIP-T8) CERAMIC DUAL-IN-LINE



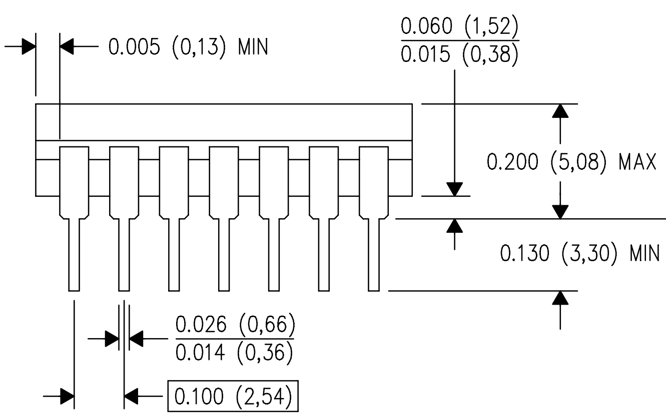
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

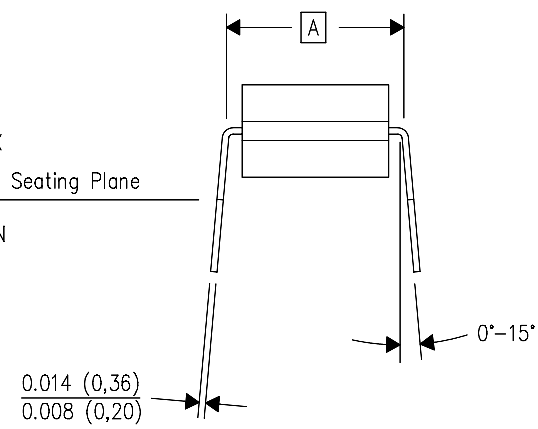
J (R−GDIP−T**) CERAMIC DUAL IN−LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

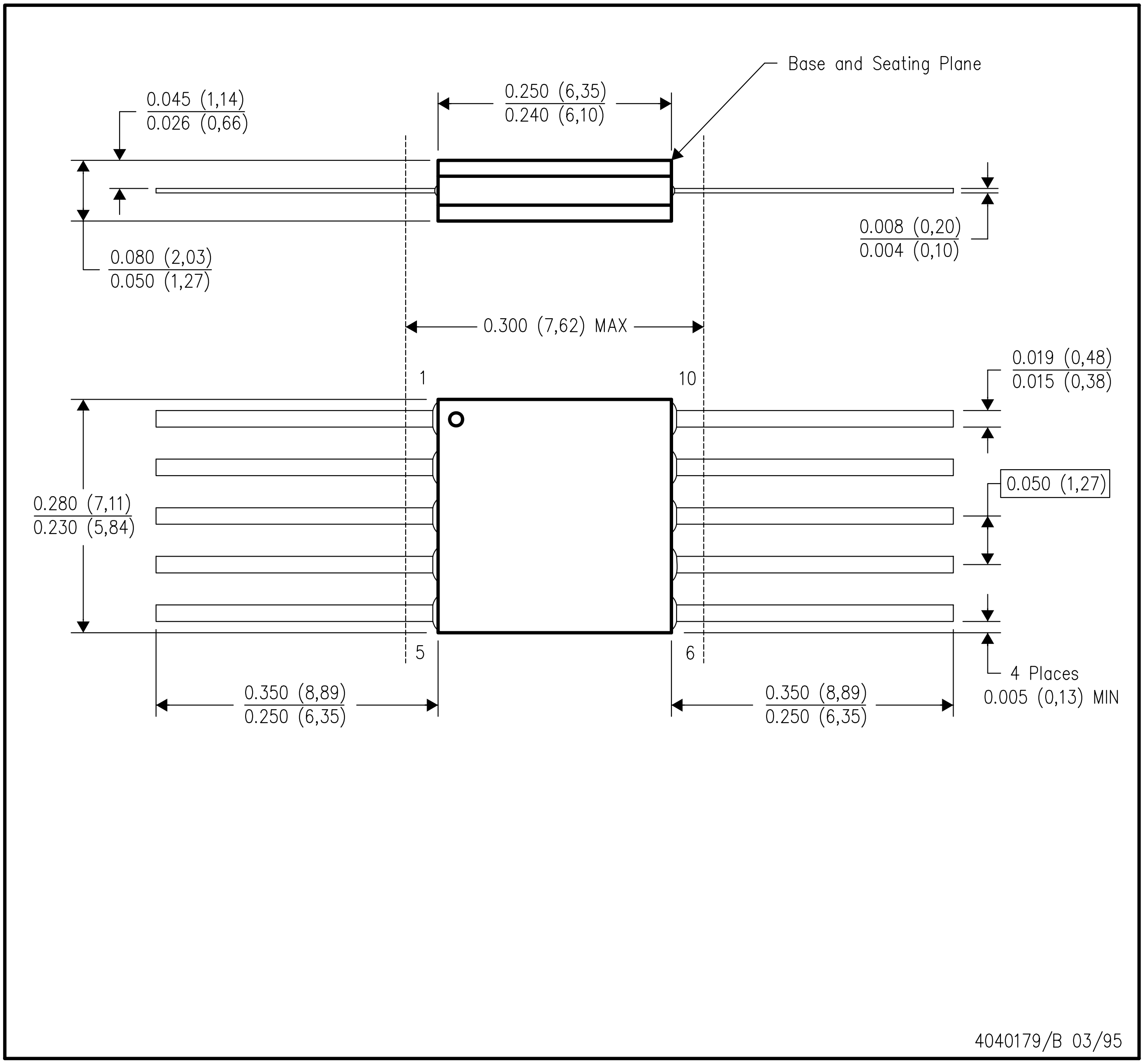




4040083/F 03/03

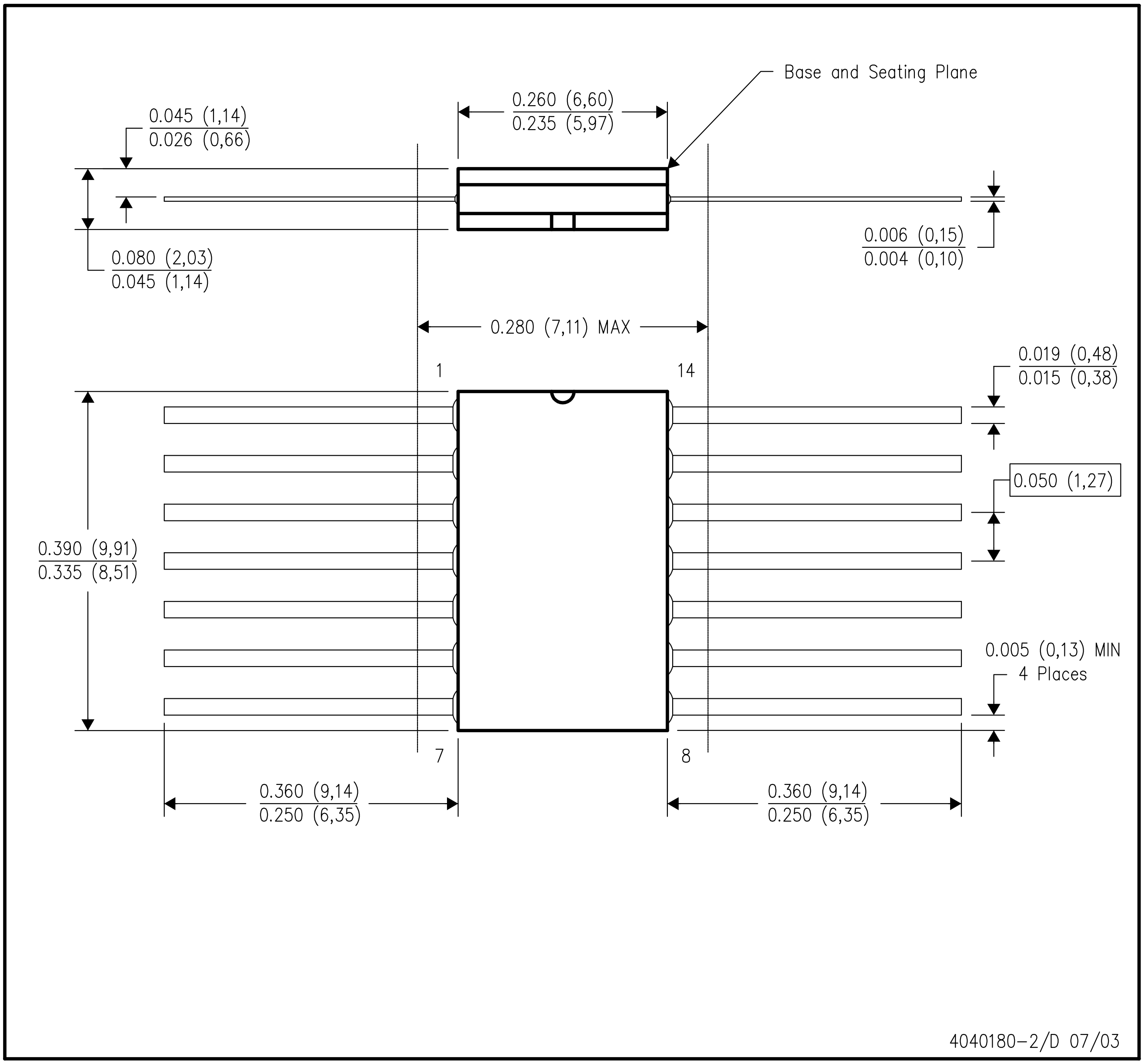
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

U (S-GDFP-F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

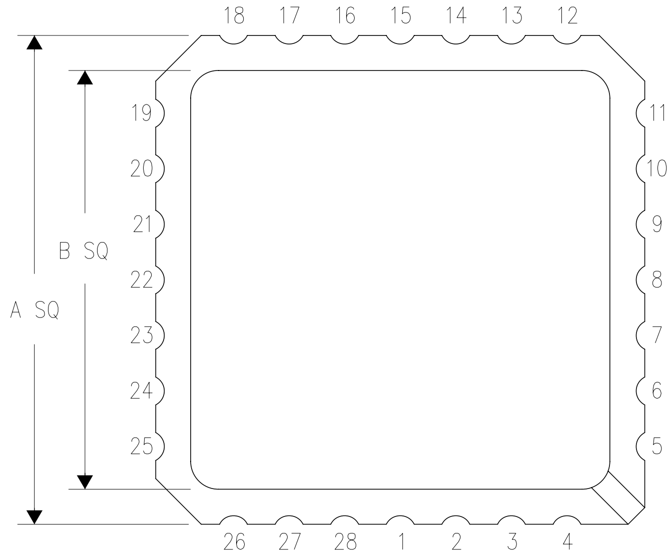
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



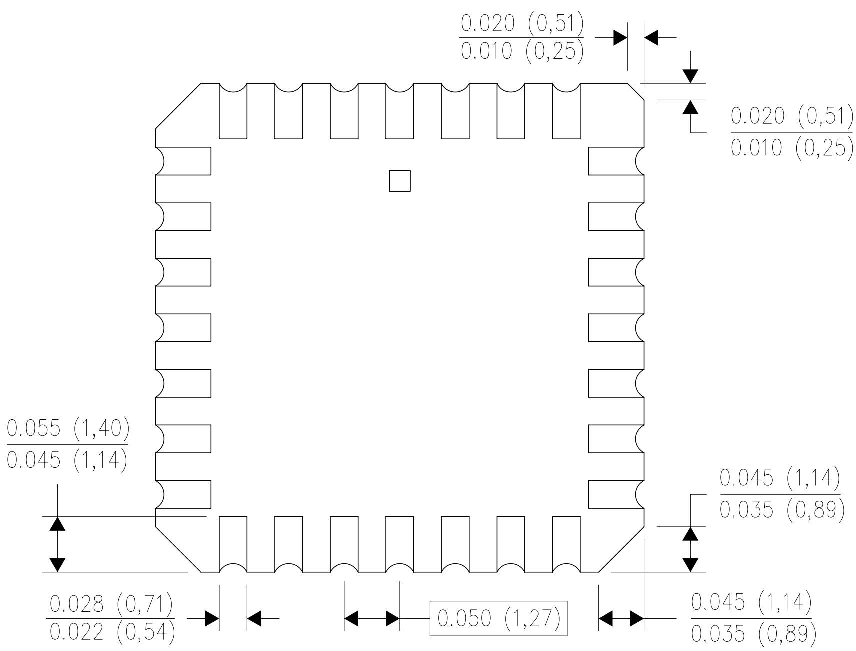
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

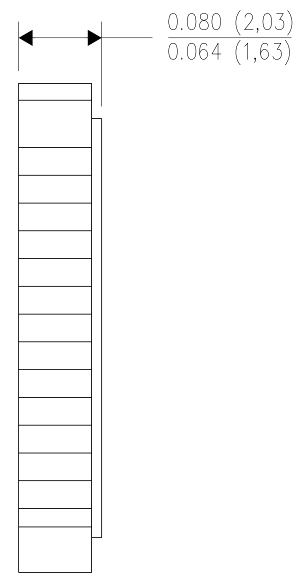
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

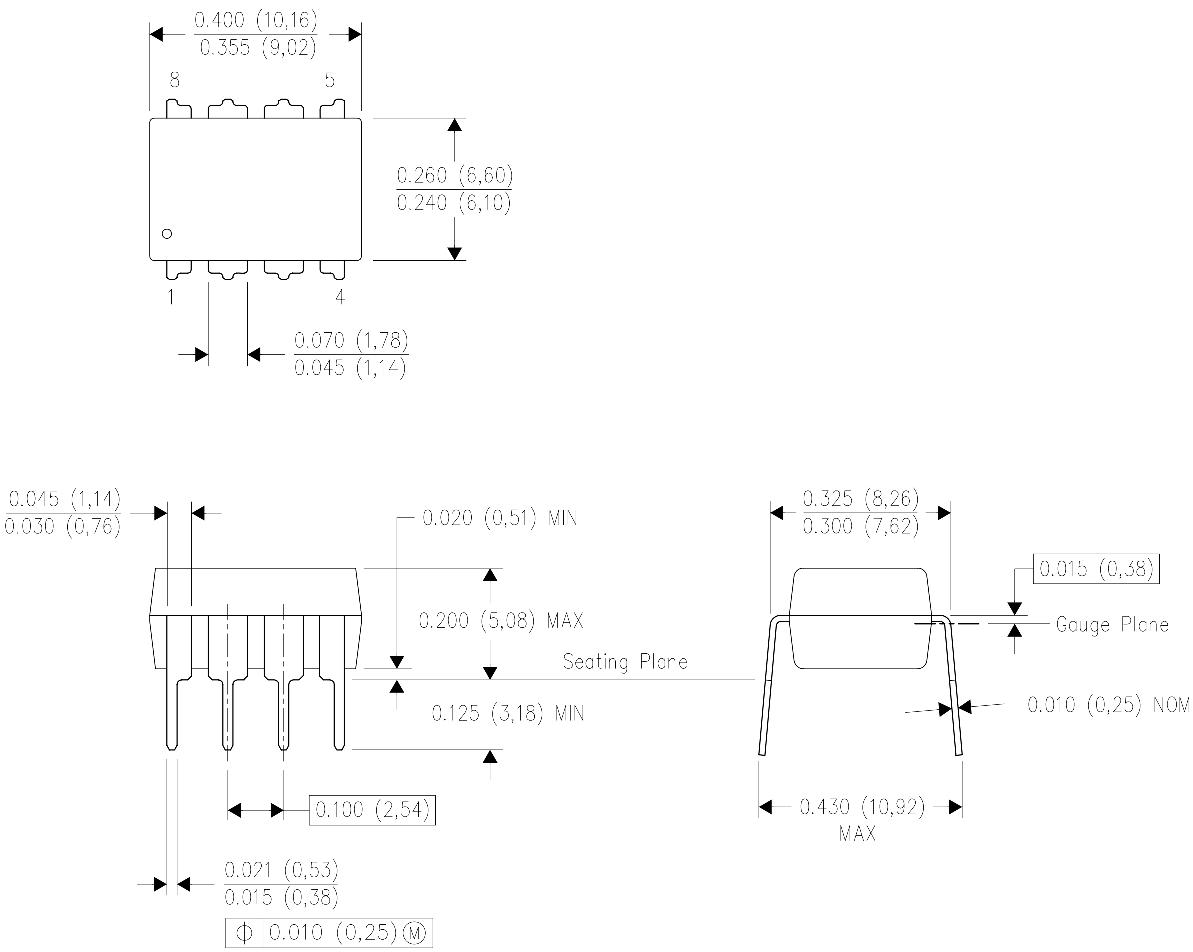




4040140/D 01/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

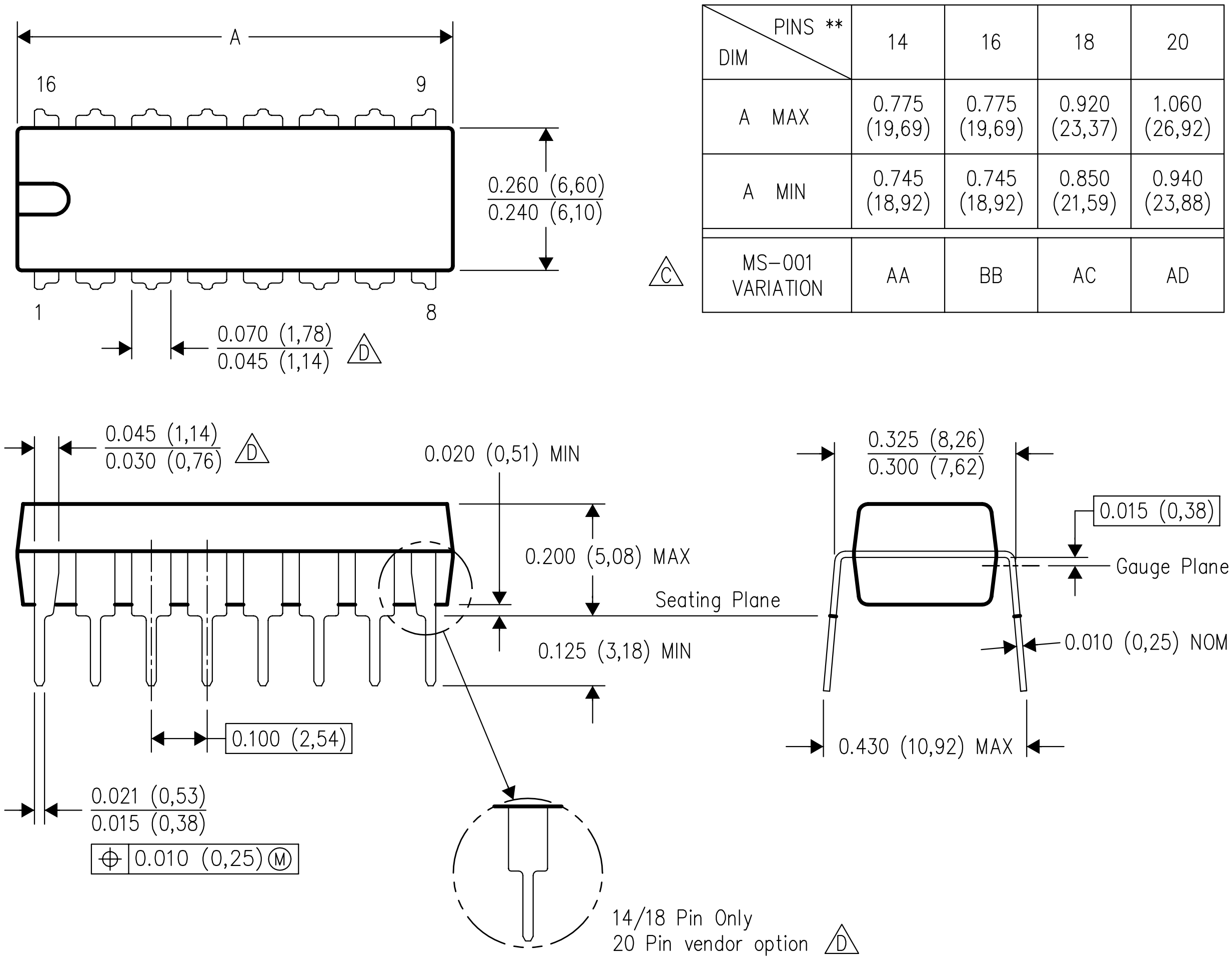


4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

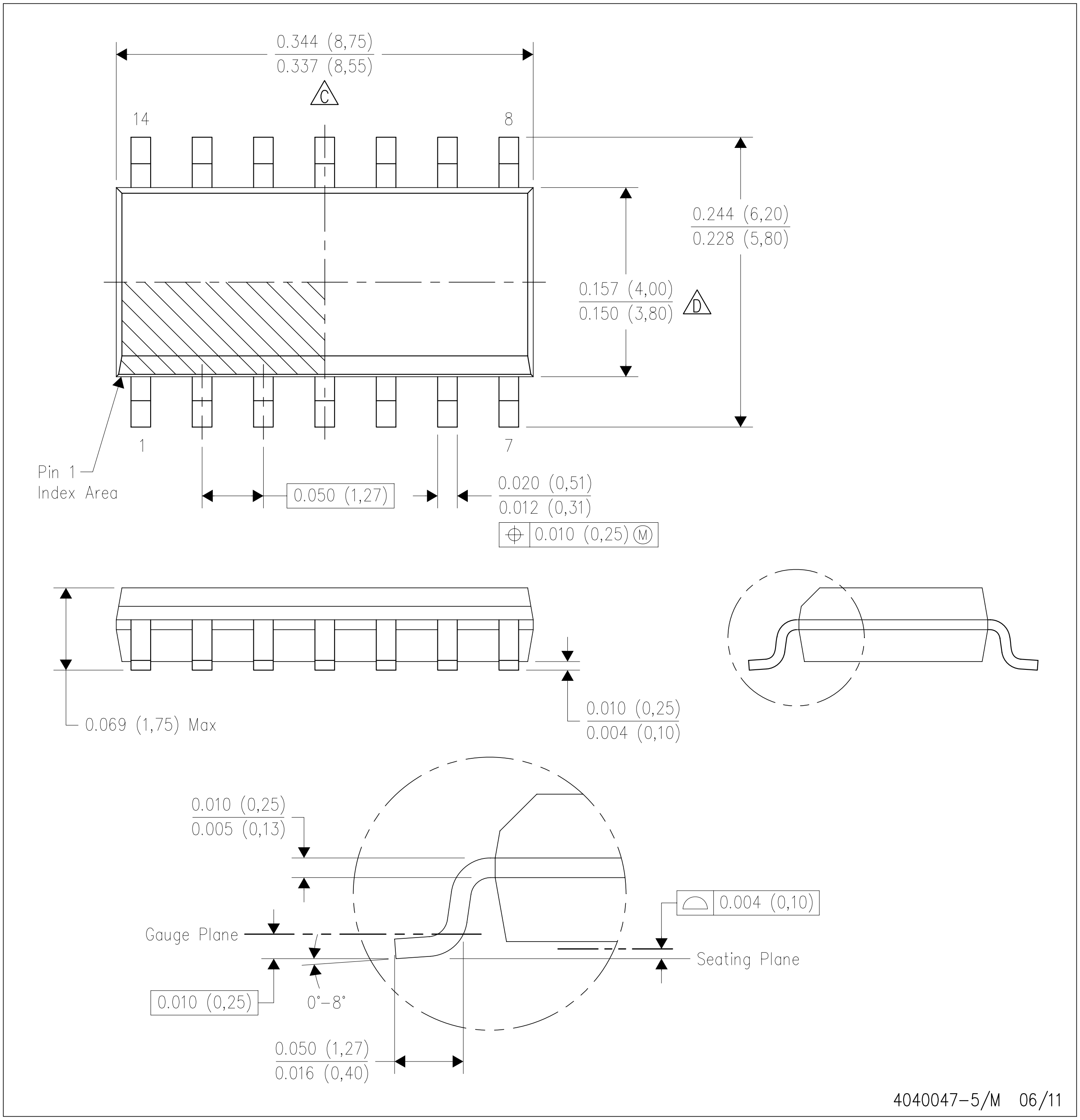


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

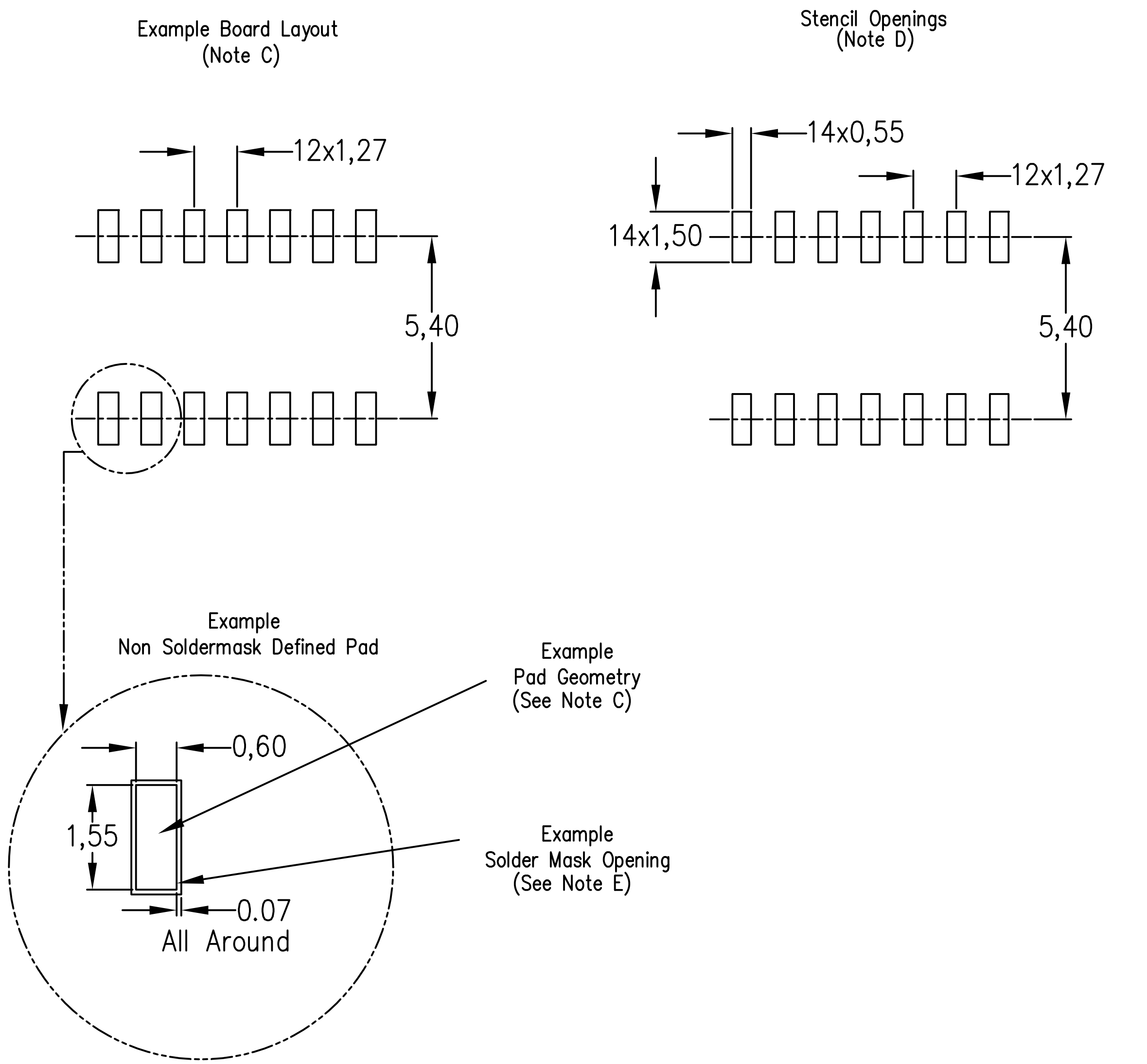
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

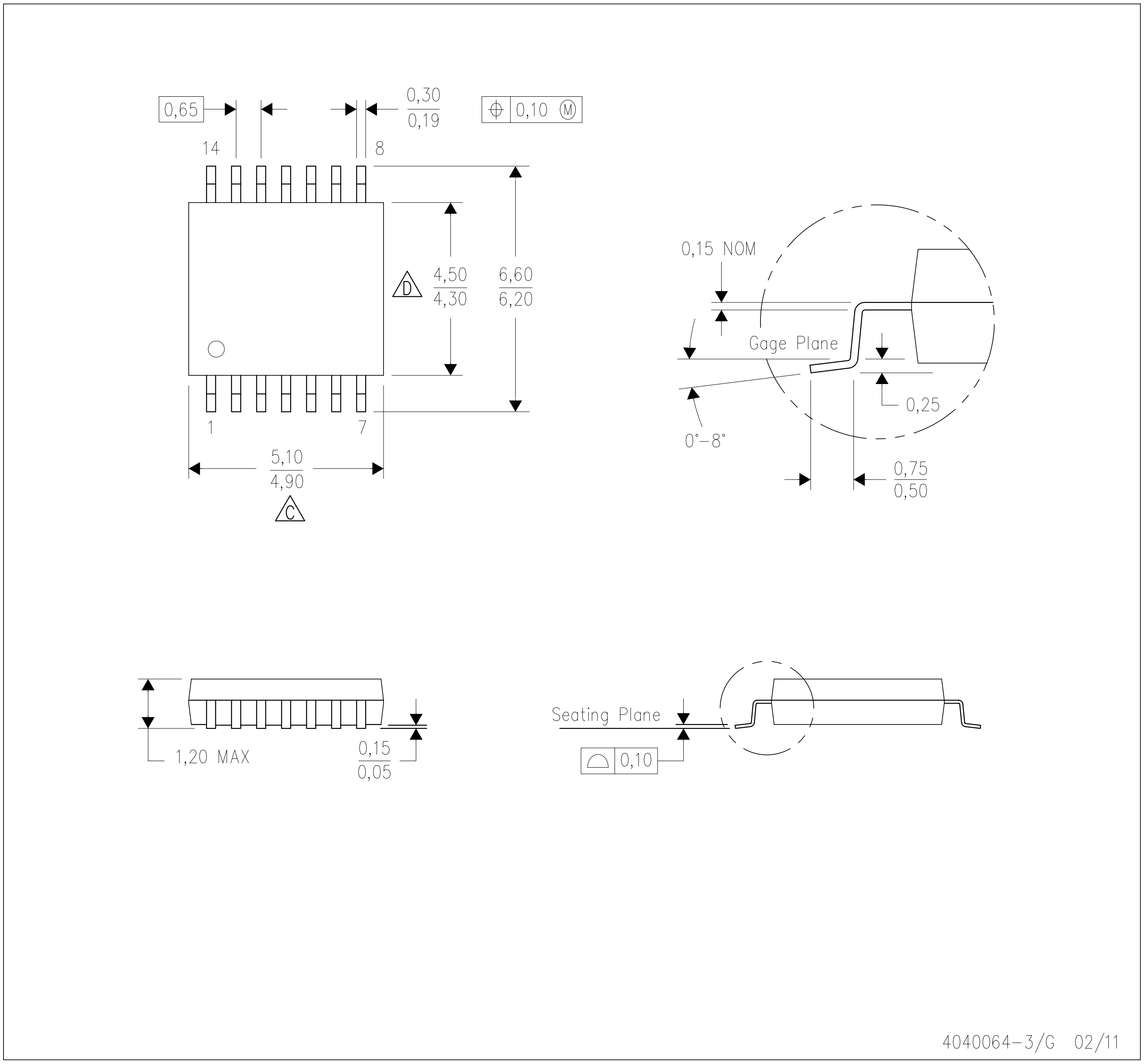
D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

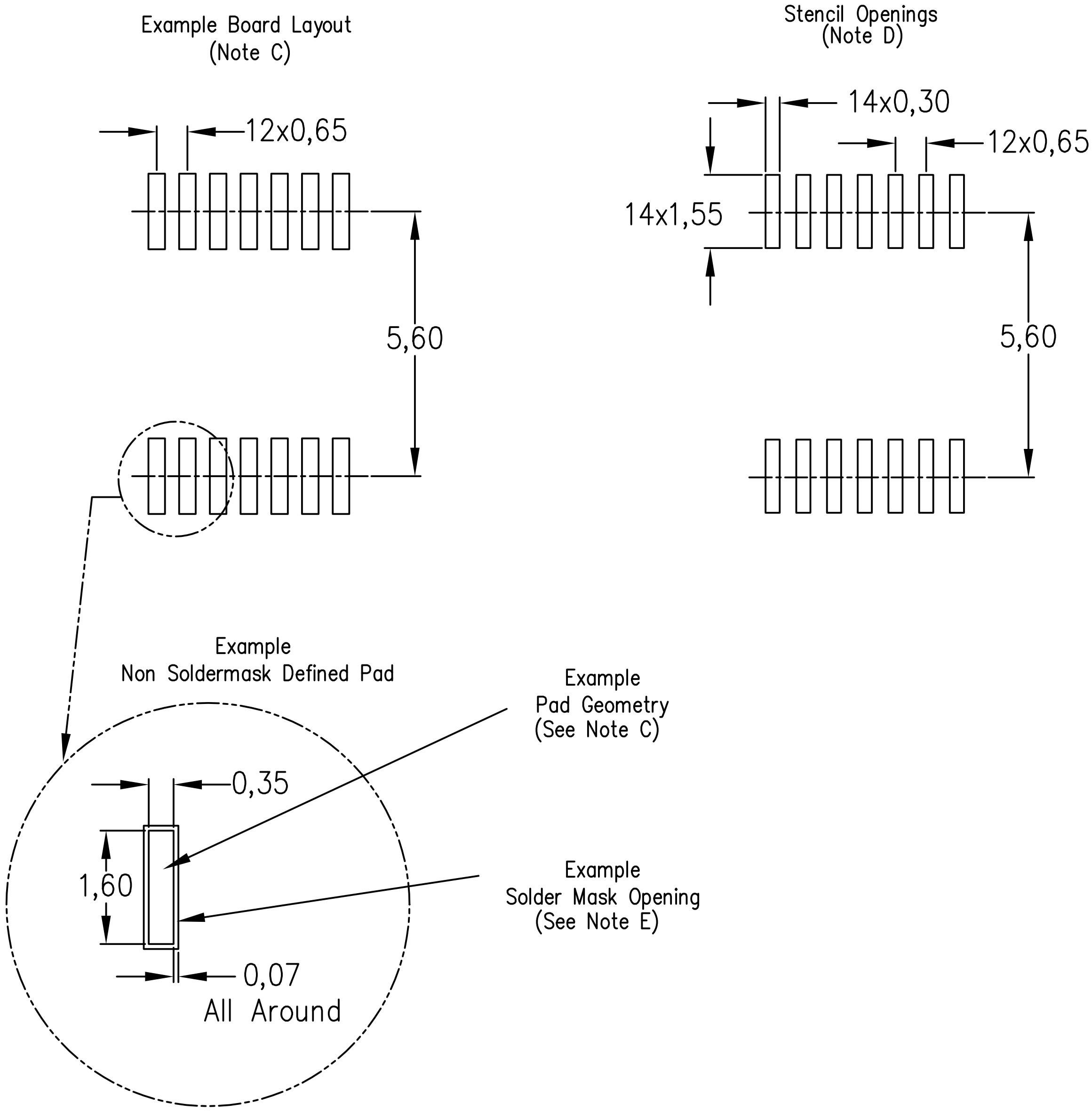
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

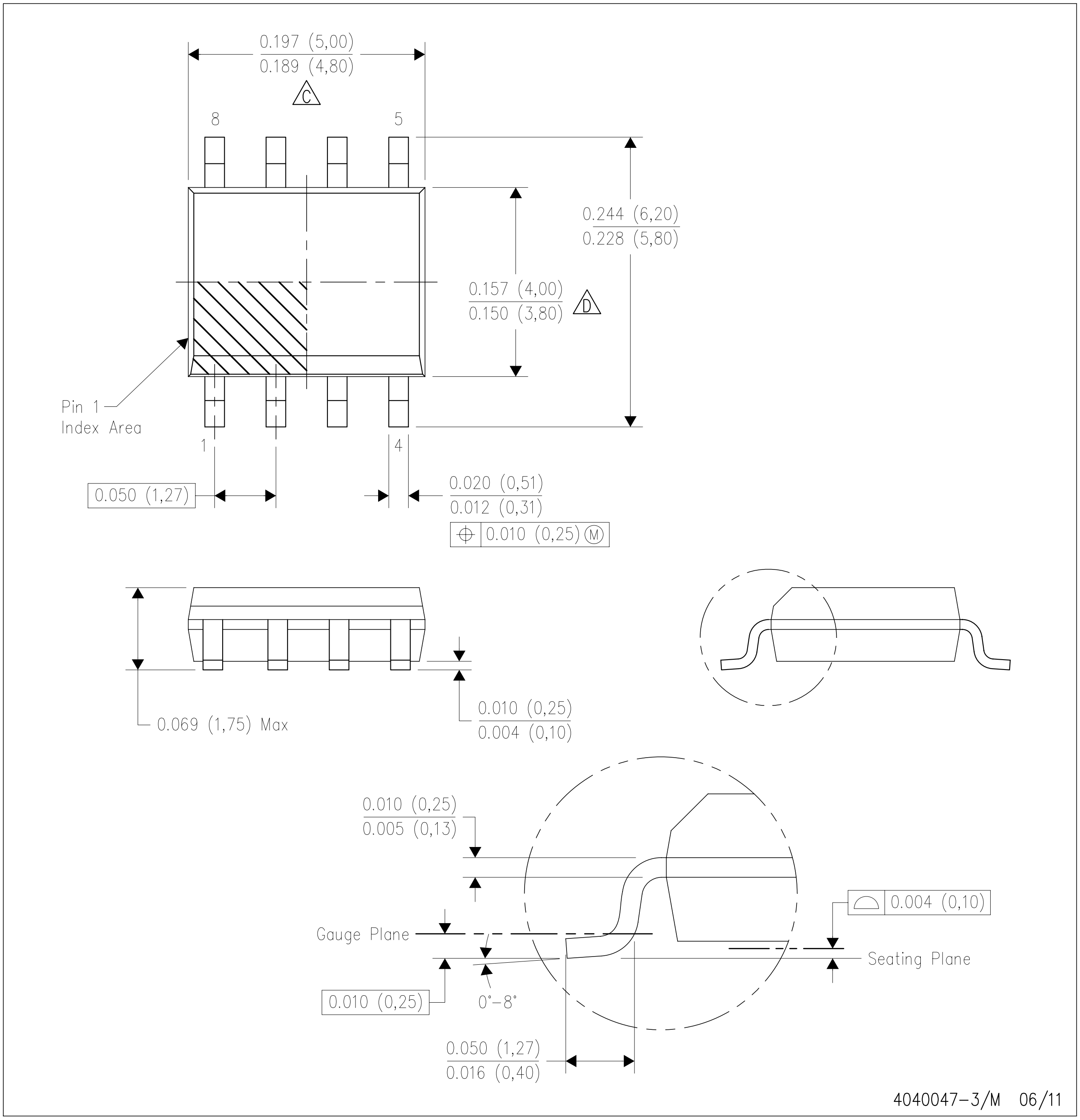
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4211284–2/F 12/12

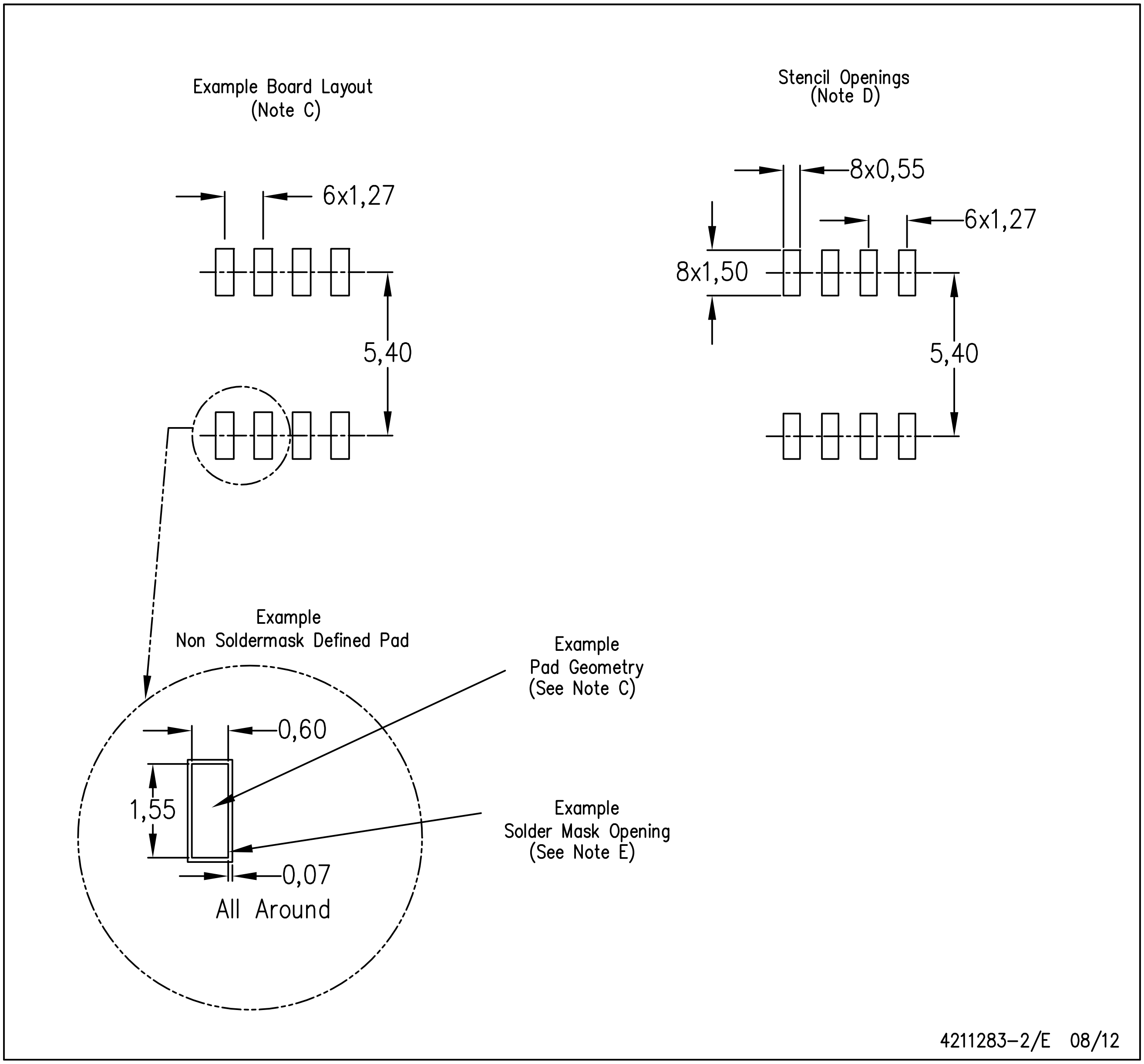
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



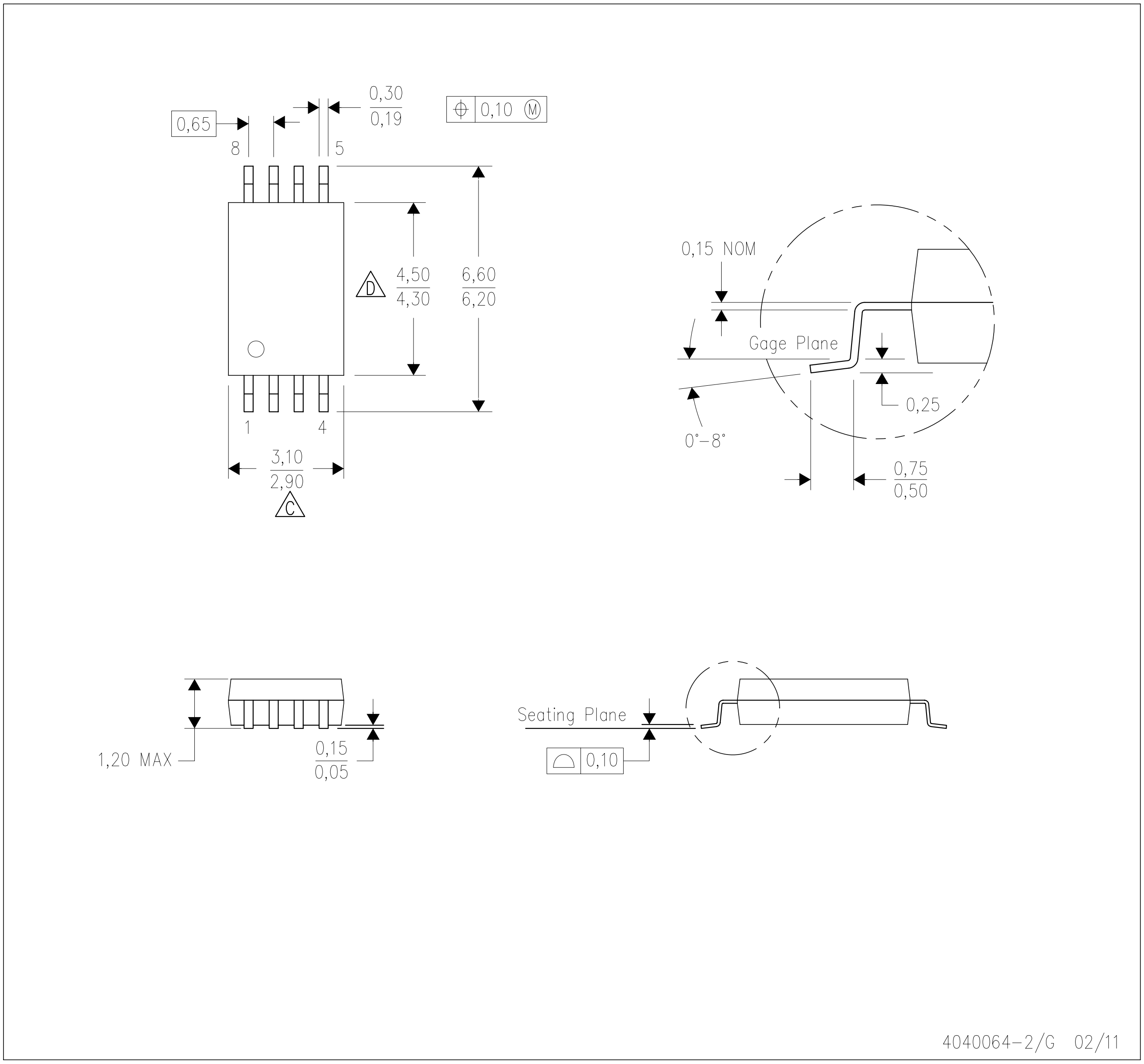
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

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