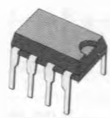
LOW NOISE JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

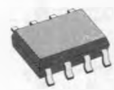
- HIGH SLEW-RATE . . . 13V/μs TYP.
- LOW-NOISE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH INPUT IMPEDANCE . . . JFET-INPUT STAGE
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- OUTPUT SHORT-CIRCUIT PROTECTION
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

The TL072 JFET-input operational amplifiers are designed to offer low-noise high slew-rate, low input bias and offset current, and low offset voltage temperture coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

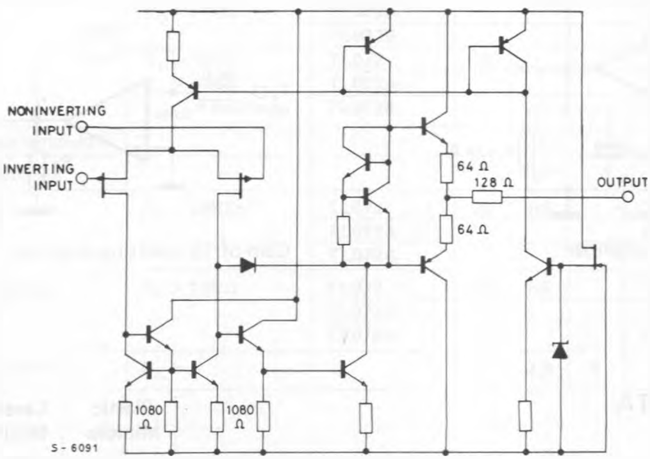


Minidip
(Plastic and Ceramic)



SO-8J

SCHEMATIC DIAGRAM
(one section)

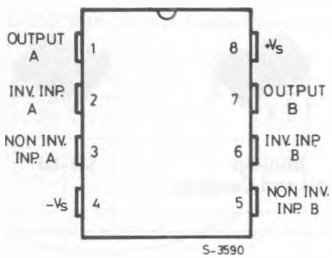


ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_I	Input voltage	± 15	V
T_{op}	Operating temperature (TL072I)	-25 to 85	°C
	(TL072C)	0 to 70	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

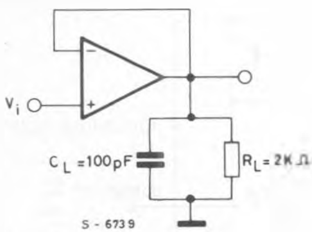
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

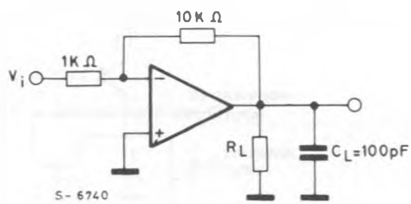


0 to 70°C	-25 + 85°C	Package
TL072CJG TL072ACJG TL072BCJG	TL072IJG – –	Ceramic Minidip
TL072CP TL072ACP TL0BCP	TL072IP – –	Plastic Minidip
TL072CD	TL072ID	SO-8

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = 15V, T_{amb} = 25°C, otherwise specified)

Parameter		Test conditions		"I" Min.	"I" Typ.	"I" Max.	"C" Min.	"C" Typ.	"C" Max.	Unit
V_{OS}	Input offset voltage	R_s = 50Ω	TL072		3	6		3	10	mV
			TL072A					3	6	mV
			TL072B					2	3	mV
		R_s = 50Ω, T_{amb} = full range	TL072			9			13	mV
			TL072A						7.5	mV
			TL072B						5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	R_s = 500Ω, T_{amb} = full range			10			10		μV/°C
I_{OS}	Input offset current		TL072		5	50		5	50	pA
			TL072A					5	50	pA
			TL072B					5	50	pA
		T_{amb} = full range	TL072			10			2	nA
			TL072A						2	nA
			TL072B						2	nA
I_b	Input bias current		TL072		30	200		30	200	pA
			TL072A					30	200	pA
			TL072B					30	200	pA
		T_{amb} = full range	TL072			20			7	nA
			TL072A						7	nA
			TL072B						7	nA
V_{CM}	Common mode input voltage range		TL072	± 11	± 12		± 10	± 11		V
			TL072A				± 11	± 12		V
			TL072B				± 11	± 12		V
V_{OPP}	Large signal voltage swing		R_L = 10KΩ	24	27		24	27		V
		T_{amb} = full range	R_L ≥ 10KΩ	24			24			V
			R_L ≥ 2KΩ	20	24		20	24		V
G_V	Large signal voltage gain	R_L ≥ 2KΩ, V_o = ± 10V	TL072	50	200		25	200		V/mV
			TL072A				50	200		V/mV
			TL072B				50	200		V/mV
		R_L ≥ 2KΩ, V_o = ± 10V, T_{amb} = full range	TL072	25			15			V/mV
			TL072A				25			V/mV
			TL072B				25			V/mV
B	Unity gain bandwidth				3			3		MHz
R_i	Input resistance				10^{12}			10^{12}		Ω
CMR	Common mode rejection	R_s ≥ 10KΩ	TL072	80	86		70	76		dB
			TL072A				80	86		dB
			TL072B							dB
SVR	Supply voltage rejection	R_s ≥ 10KΩ	TL072	80	86		70	76		dB
			TL072A				80	86		dB
			TL072B				80	86		dB
I_S	Supply current	R_L = ∞			2.8	5		2.8	5	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		"I" Min.	"I" Typ.	"I" Max.	"C" Min.	"C" Typ.	"C" Max.	Unit
Cs	Channel separation	$G_V = 100$			120			120		dB
SR	Slew-rate at	$V_I = 10V$, $C_L = 100pF$	$R_L = 2K\Omega$		13			13		V/μs
t_r	Rise time	$V_I = 20mV$	$R_L = 2K\Omega$		0.1			0.1		μs
	Overshot factor	$C_L = 100pF$			10			10		%
e_N	Total input noise voltage	$R_S = 100\Omega$	F = 1KHz		18			18		$\frac{nV}{\sqrt{Hz}}$
			f = 10Hz to 10KHz		4			4		μV
I_N	Input noise current	f = 1KHz			0.01			0.01		$\frac{pA}{\sqrt{Hz}}$
d	Total harmonic distortion	$V_o = 10V_{rms}$, $R_S < 1K\Omega$, $R_L > 2K\Omega$	f = 1KHz		0.01			0.01		%

Fig. 1 – Maximum peak to peak output voltage vs. frequency.

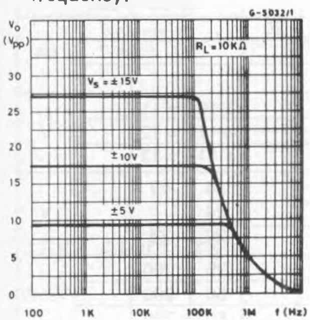


Fig. 2 – Maximum peak to peak output voltage vs. frequency

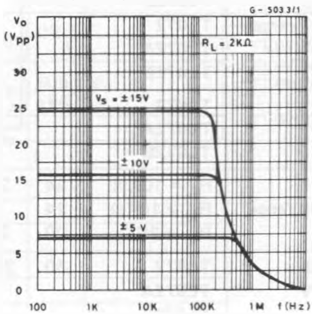


Fig. 3 – Maximum peak to peak output voltage vs. load resistance

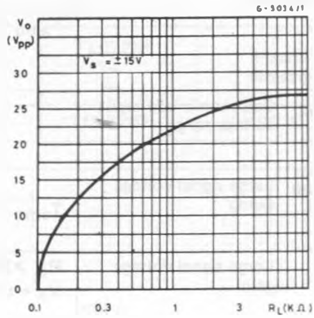


Fig. 4 – Large signal voltage gain and phase shift vs. frequency

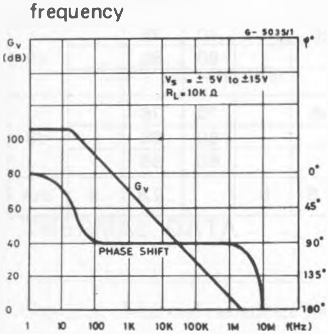


Fig. 5 Supply current vs. ambient temperature

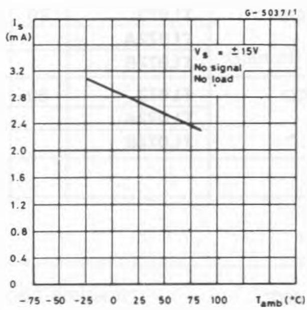
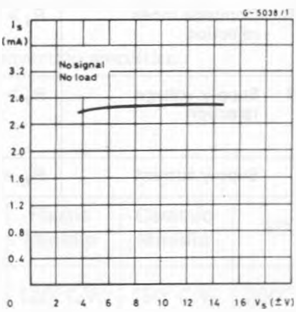


Fig. 6 – Supply current vs. supply voltage



SGS-THOMSON MICROELECTRONICS

Fig. 7 — Input bias current vs. temperature

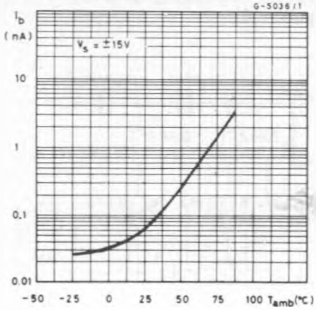


Fig. 8 — Voltage follower large signal pulse response

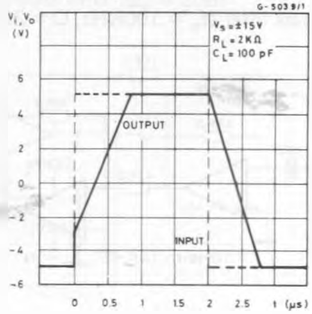


Fig. 9 — Output voltage vs. elapsed time

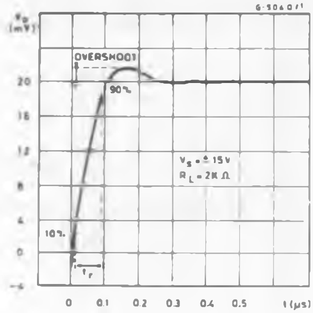


Fig. 10 — Equivalent input noise voltage vs. frequency

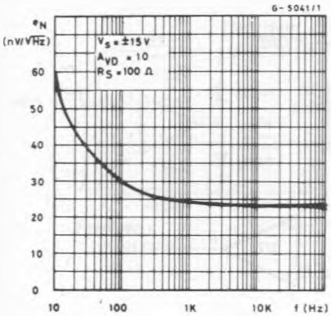


Fig. 11 — Total harmonic distortion vs. frequency

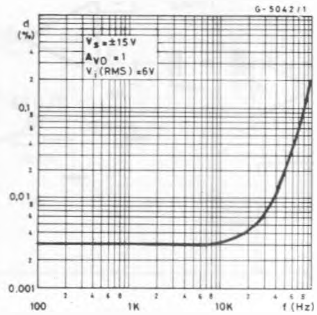
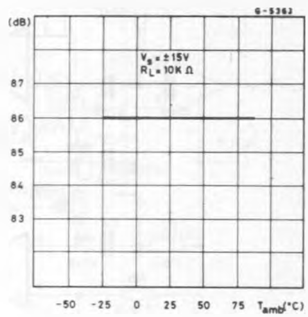
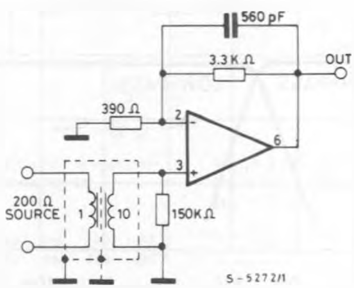


Fig. 12 Common mode rejection vs. temperature



APPLICATION INFORMATION

Fig. 13 — Low-Noise High Slew-Rate mike preamplifier (G_v = 40 dB)



APPLICATION INFORMATION (continued)

Fig. 14 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)

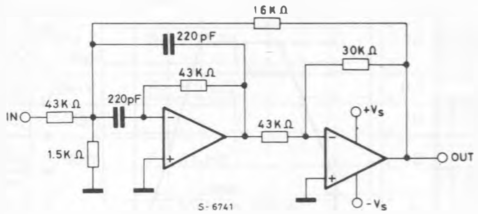


Fig. 15 - Fourth-order subtractive Linkwitz-Riley crossover filter (f = 200Hz)

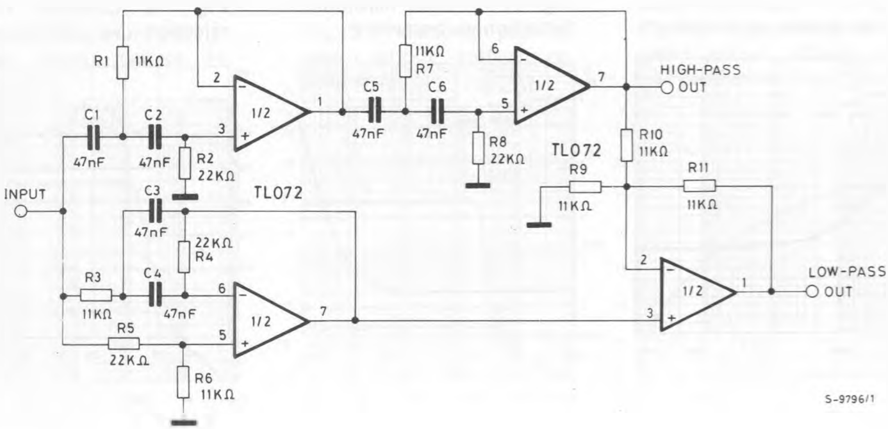
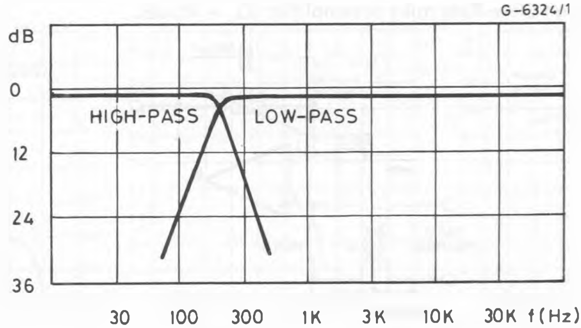


Fig. 16 - Frequency response of the 24dB/octave crossover filter of fig. 15



APPLICATION INFORMATION (continued)

Fig. 17 – 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

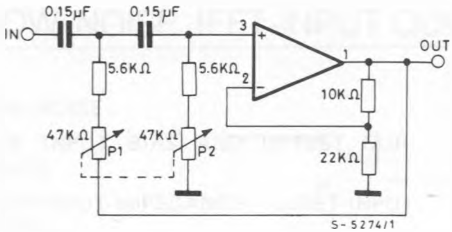


Fig. 18 - Frequency response of the high-pass filter of fig. 17

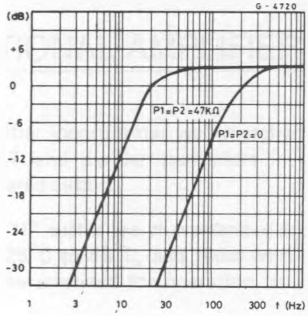


Fig. 19 - Unity-gain absolute-value circuit

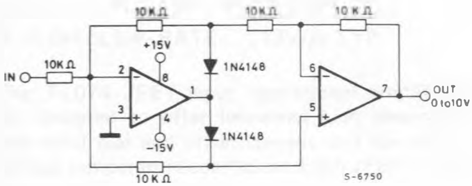


Fig. 20 - Single supply sample and hold

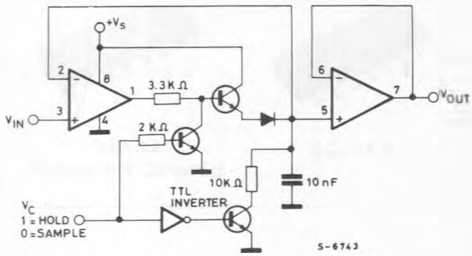
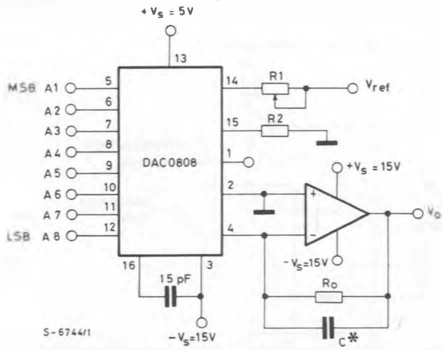


Fig. 21 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 µs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

V_{ref} = 2.0 V_{dc}
R1 = R2 ≈ 1.0 kΩ
R_o = 5.0 kΩ

$$V_o = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$