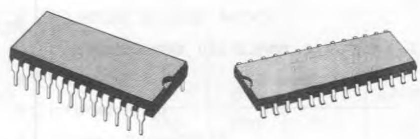
SPEECH CIRCUIT WITH POWER MANAGEMENT

ADVANCE DATA

- 2/4 WIRES INTERFACE WITH
  - Double antisidetone network
  - Rx gain and AC impedance externally programmable
- DTMF INTERFACE
- PULSE DIAL INTERFACE
- 4.0 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- RESET TO MICROPROCESSOR
- CURRENT SUPPLY FOR LOUDSPEAKER
- HANDS-FREE INTERFACE
- DC CHARACTERISTIC AND ON/OFF HOOK FOR FRANCE
- CONTROL AGAINST HIGH VOLTAGE TRANSIENTS



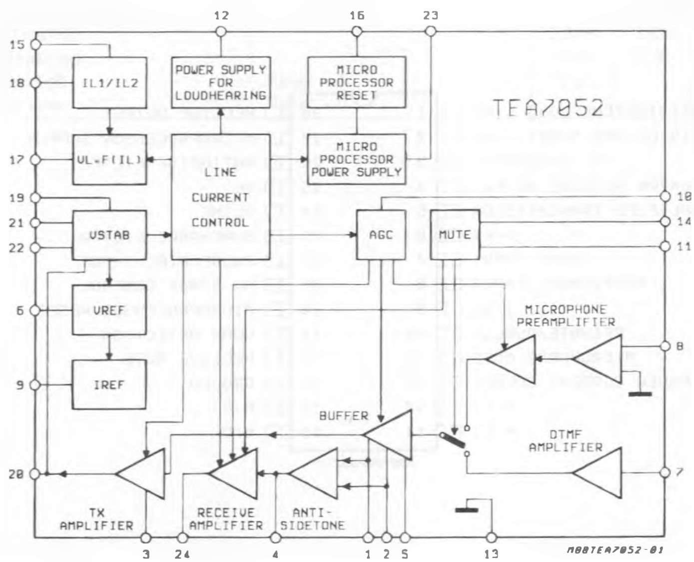
DIP24 SO-28

ORDER CODES : TEA7052DP (DIP24)
TEA7052D (SO-28)

DESCRIPTION

The TEA7052 is expressely designed to meet the french specification for telephone set in medium and high range equipments.

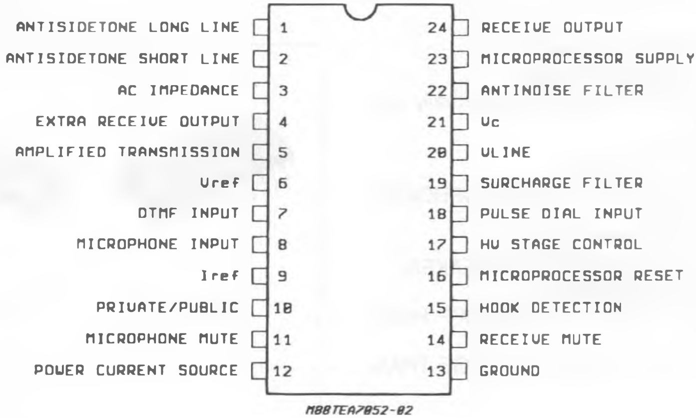
BLOCK DIAGRAM



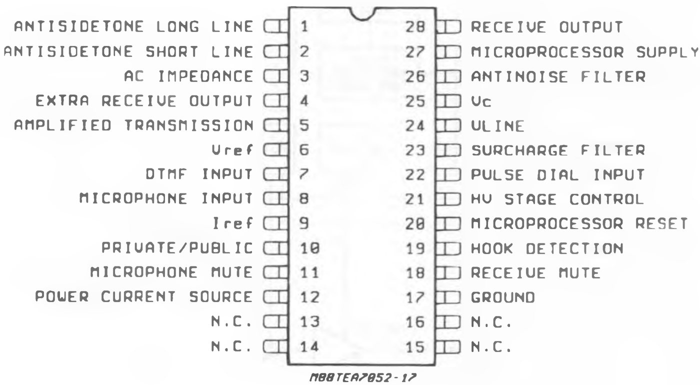
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice

PIN CONNECTIONS (top view)

DIP24



SO-28



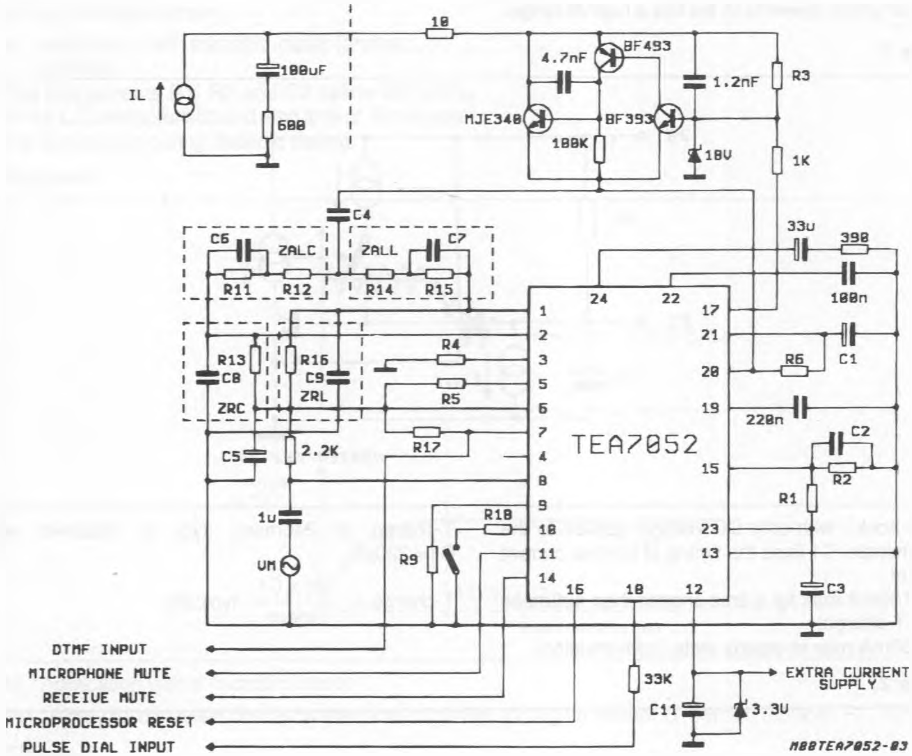
ELECTRICAL CHARACTERISTICS (Ta = 25°C ; PIN identification related to DIP–24 configuration)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vc	Stabilized Voltage (pin 21)	Il = 27mA	2.35	2.6	2.85	V
Idem	Charging Current (pin 21)	Il = 27mA		2.6		mA
Ir	Line Current Regulation for HV Control (pin17)	Pin 15 = Pin 21 = GND Il = 150mA Il = 100mA	 150 		 5	 µA
		Pin 15 ON ; Pin 21 = GND Il = 75mA	 150			 µA
   Ir/Il		Pins 15 and 21 ON Il = 60mA Il = 16mA 27mA < Il < 50mA	 150 0.8	 0.9	 100 1.0	 µA nA µA/mA
Iint	Internal Bias Current (pin 21)	Il = 27mA ; R9 = 26.7 Kohms ; (V20 = R6 x Iint + Vc)	250	280	310	µA
Vref	Reference Voltage	Il = 27mA	1.32	1.38	1.47	V
Iref	Current at Vref		– 10		100	µA
Vmp	Stabilized Supply at Pin 23		3.7	4.0		V
Icmp	Charging Current at Pin 23	Pin 15 = Pin 21 = GND IL1 = Il – Idem	0.7 x x IL1			mA
Ispm	Static Current at Pin 23	Il = 6mA Il > 25mA	0.5 2.5	 2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Iea	Supply Current for Parallel Circuits (pin 12)	R9 = 26.7Kohm Il = 10mA Il = 27mA Il = 42mA	 8 21	 3 9.5 23.5	 11 26	 mA mA mA
 Vrh Vrb Vrsh Vrsb	Microprocessor Reset High Treshold Low Treshold Output High Output Low	 Reset = 1 Reset = 0	 0.845 0.76 0.9 	 0.89 0.8 	 0.84 0.1	 Vmp (pin 23)

ELECTRICAL CHARACTERISTICS (Ta = 25°C ; PIN identification related to DIP–24 configuration)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vmh Vmb	Mute Microphone (pin 11)	ON OFF	1.6		 0.8	V V
Vmh Vmb	Mute Earphone (pin 14)	ON OFF	2.7		 2.1	V V
Gel Gec	Tx Gain Long Line Tx Gain Short Line	Il = 27mA Il = 42mA	41 34	42 36	43 38	dB
Gmf	DTMF Gain	Il = 27mA Pin 11 > 1.6V	41	42	43	dB
De	Tx Distorsion	Il = 27 to 42mA Vl = 0dBm Vl = 3dBm			 3 10	 % %
Ze	Microphone Impedance		20			Kohm
Bep	Tx Noise (psophometric)	Il > 27mA 2K at Pins 6-8		– 73		dBmp
Re	Tx Attenuation in Mute Mode	Il = 27mA Pin 11 > 1.6V	60			dB
Grl Grc	Rx Gain Long Line Rx Gain Short Line	Il = 27mA Il = 42mA	29 22	30 24	31 26	dB
Dr	Rx Distorsion	Il = 27 to 42mA Vec = 500mV Vec = 700mV			 3 10	 % %
Brp	Rx Noise	Il > 27mA		– 74		dBmp
Rc	Rx Attenuation in Mute Mode	Il = 27mA Pin 14 > 2.7V	60			dB
Gal	Antisidetone	Il = 27 to 42mA	– 22			dB
Zac	AC Impedance	Il > 27mA	500	650	800	ohm
Grs	Confidence Level Vrec/Vmf	Pin 11 > 1.6V ; Pin 14 > 2.7V	35.5	38.5	41.5	dB

TEST CIRCUIT



R1 = 920KΩ
R2 = 820KΩ
R3 = 1.5MΩ
R4 = 75Ω
R5 = 5.1KΩ
R8 = 13KΩ
R9 = 26.7KΩ
R11 = 140KΩ

R12 = 0Ω
R13 = 2.7KΩ
R14 = 0Ω
R15 = 140KΩ
R16 = 2.7KΩ
R17 = 1.2 KΩ
R18 = 680KΩ for private complex

C1 = 100μF
C2 = 4.7μF
C3 = 10μF
C4 = 1μF
C5 = 100μF

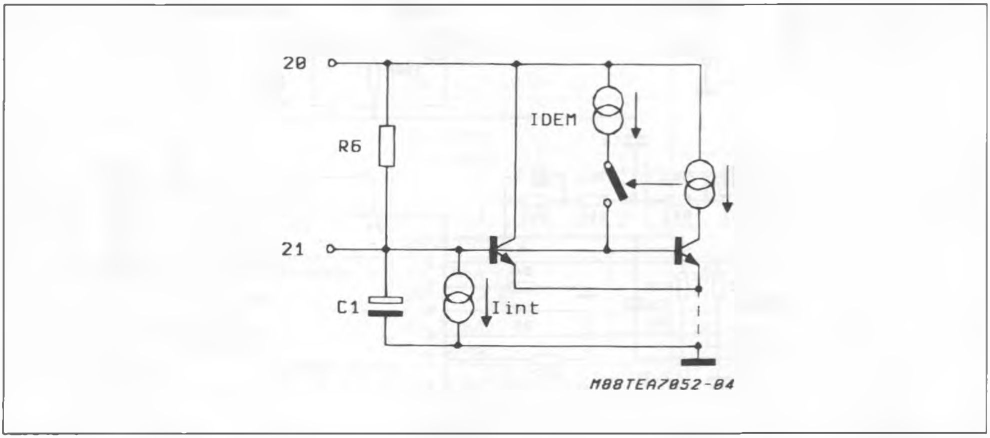
C6 = 27pF
C7 = 27pF
C8 = 2.2nF
C9 = 2.2nF
C11 = 220μF

CIRCUIT DESCRIPTION

1. DC-CHARACTERISTICS

1.1. VC (pin 21). The stabilized voltage Vc is connected to Vline (pin 20) through an internal shunt regulator which presents to the line a high AC impedance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 21) must be not lower than 47 microFarad.

Figure 1.



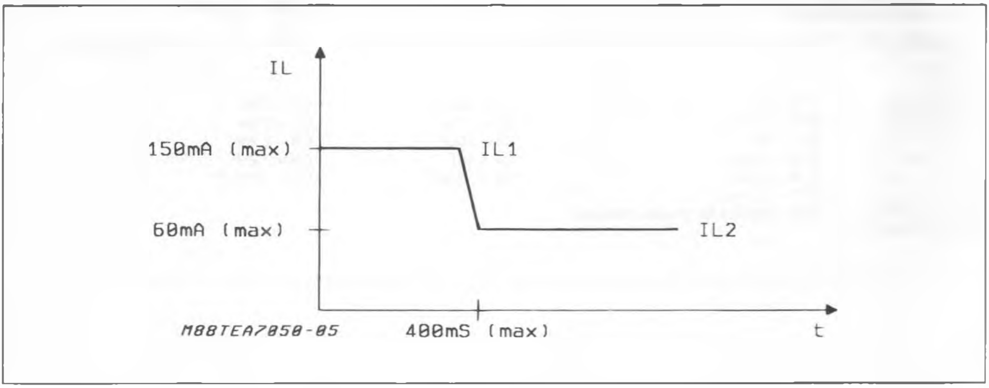
At "Off-hook", with only DC voltage applied to the line terminals, C1 fixes the timing of the line current profile at :

- 150mA max for a time shorter than 400msec (T-charge)
- 60mA max in steady state (conversation)

T-charge of 240msec (typ) is obtained with C1= 220µF.

$$\text{T-charge} = \frac{\text{Vc x C1}}{\text{Idem}} \text{ typically.}$$

Figure 2.



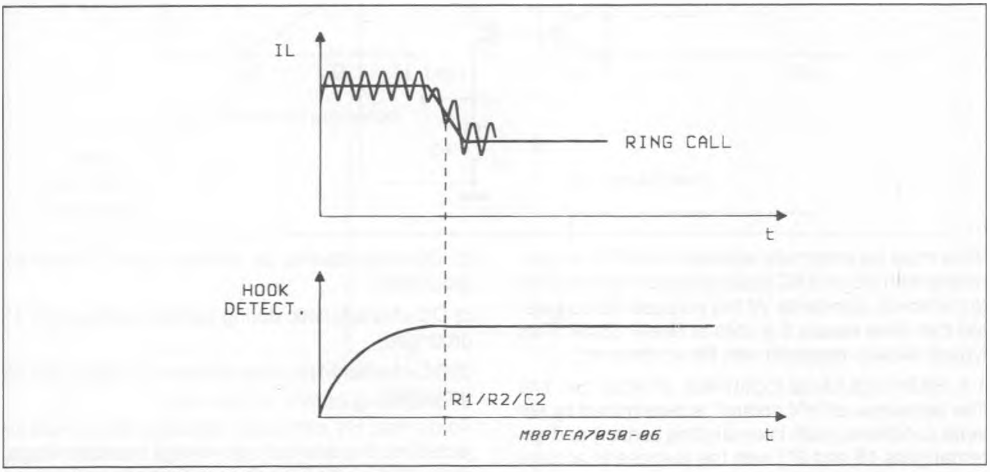
1.2. HOOK DETECTION (in ring mode) (pin 15).
The DC-characteristic requested to allow off-hook detection by the exchange during ring call may be accomplished :
a) through an analog control (R-C) or
b) by a microprocessor.

a) Application with standard dialer (analog control)
The components R1, R2 and C2 define the timing of the DC characteristic and also limit at 75mA-peak the line current during decadic dialing.

Optimum values are : - R1 x C2 = 1.8 sec ;
R2 x C2 = 0.8 sec.

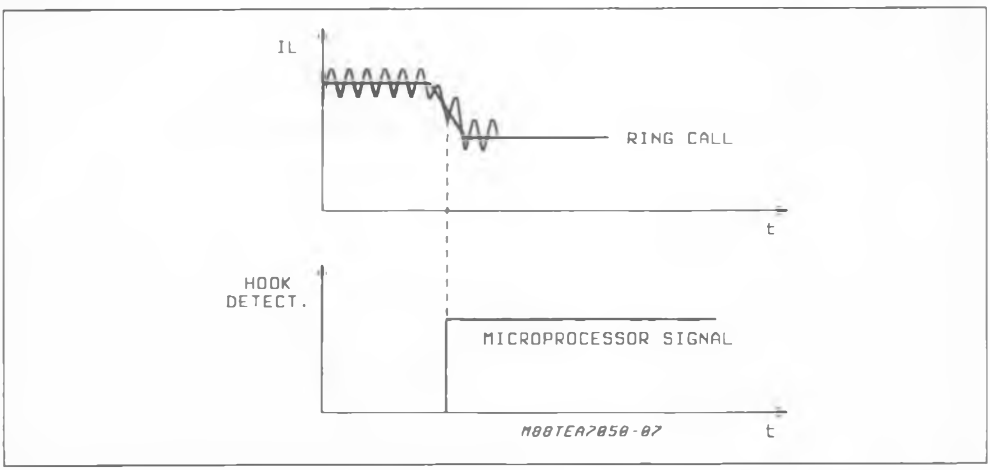
To reduce the minimum time between a "on-hook / off-hook" sequence, R2 may be replaced by a switch to ground.

Figure 3.



b) Application with a microprocessor
Pin 15 may be controlled directly by the micro-controller, through a resistor R1b which replaces R1, R2 and C2.

Figure 4.



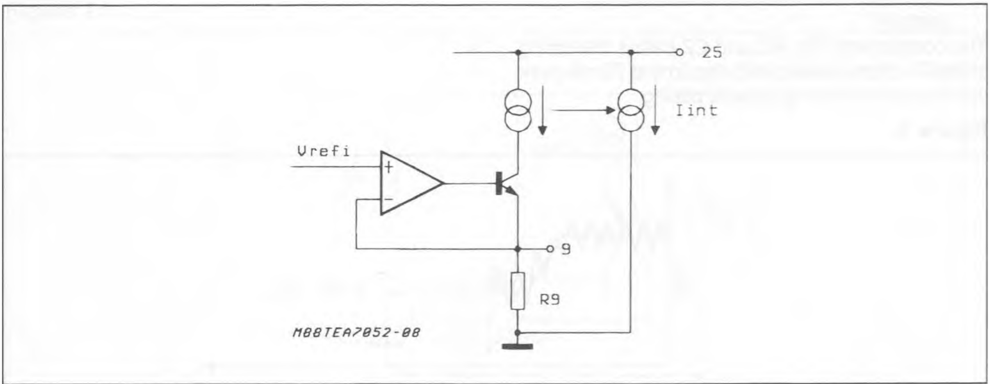
1.3. VLINE (pin 20). The line voltage (pin 20) is determined by the value of the external resistor R6 and by the internal current, lint, flowing between Vc (pin 21) and Ground (see also paragr. 1.1.) :

$$Vline = Vc + R6 \times lint.$$

Vc is fixed by design at about 2.6 volts.

Lint is reversely related to R9 (Lint = 7.5V/R9 at Iline = 27mA).

Figure 5.



Vline must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the french standards. At this purpose it is suggested that Vline equals 5.6 volts at Iline = 16mA. This typical value is obtained with R6 = 13Kohm.

1.4. HIGH VOLTAGE CONTROL STAGE (pin 17). The behaviour of "HV control" is determined by several conditions, both internal (Iline sensor) and external (pins 15 and 21) with the purpose to accomplish the different DC characteristics and transitory conditions imposed by the French specification :

a) steady DC-characteristic and lightnings (pins 15 and 21 ON)

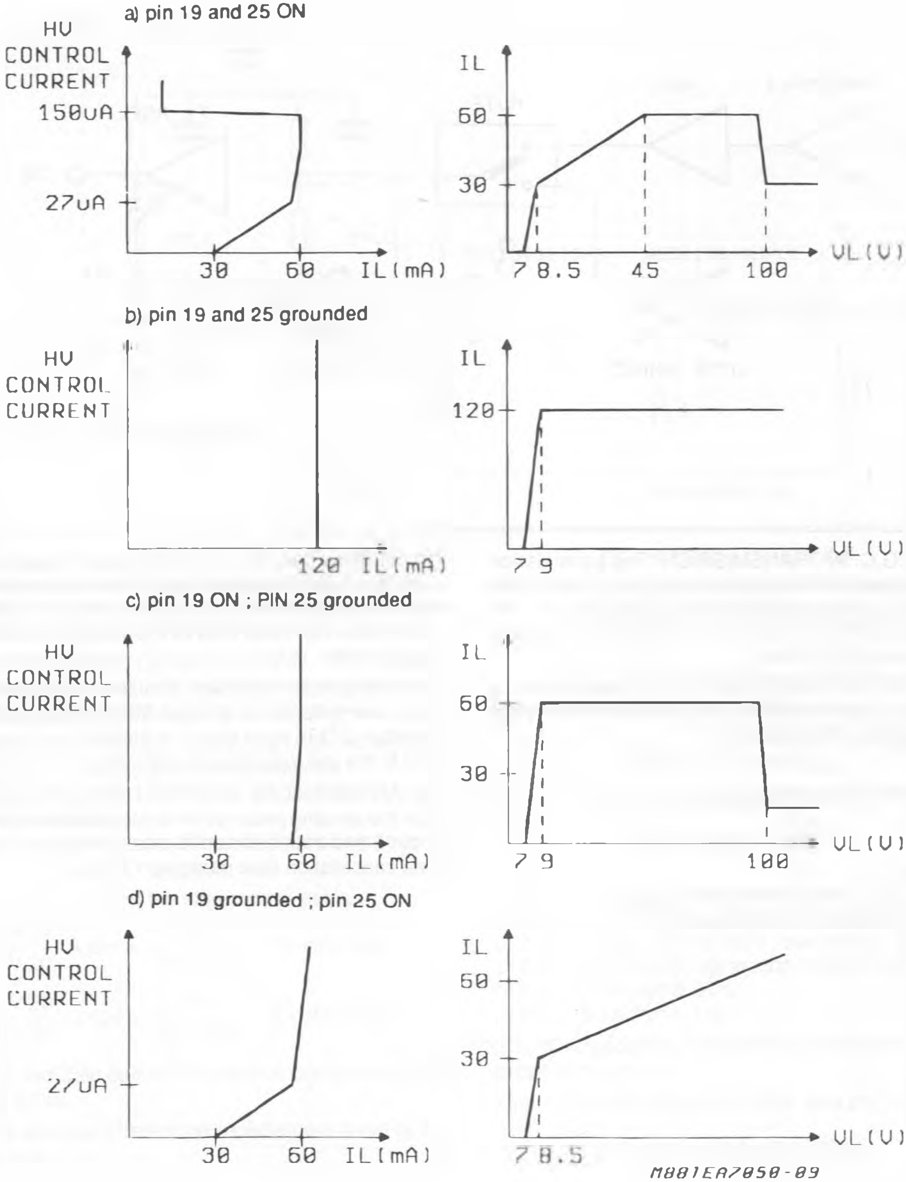
b) DC-characteristic at off-hook (pin 15 and 21 grounded)

c) DC-characteristic during decadic dialing (pin 21 grounded)

d) DC-characteristic after off-hook in ringing (pin 15 grounded)

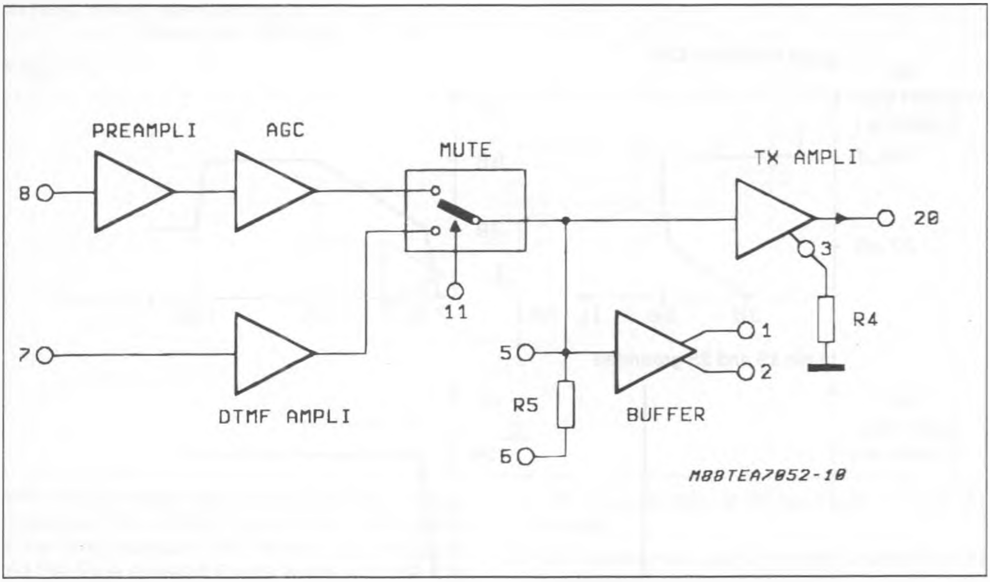
To do that, HV control pin regulates the current injected into the external high voltage transistor stage, requested by the French specification.

Figure 6.


a) pin 19 and 25 ON
HV
CONTROL
CURRENT
150uA
27uA
30
60
IL(mA)
IL
60
30
7 8.5
45
100
VL(V)
b) pin 19 and 25 grounded
HV
CONTROL
CURRENT
120
IL(mA)
IL
120
7 9
VL(V)
c) pin 19 ON ; PIN 25 grounded
HV
CONTROL
CURRENT
30
60
IL(mA)
IL
60
30
7 9
100
VL(V)
d) pin 19 grounded ; pin 25 ON
HV
CONTROL
CURRENT
27uA
30
60
IL(mA)
IL
60
30
7 8.5
VL(V)
M88TEA7050-09

2. TRANSMISSION CHAIN

Figure 7.



2.1. A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 8) and Vline (pin 20) is internally decreased of 6dB when the line current varies from 27mA to 42mA with a constant AC load of 600 ohms.

2.2. SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 (at pin 3).

Zout = 10.65 x Z4.

The total AC impedance shown to the line is the parallel

Zpar = Zout//Zint//Zext

where :

- Zint = 10kohm // 8.5nF (internal)
- Zext = R6 // C4 (at pin 20)

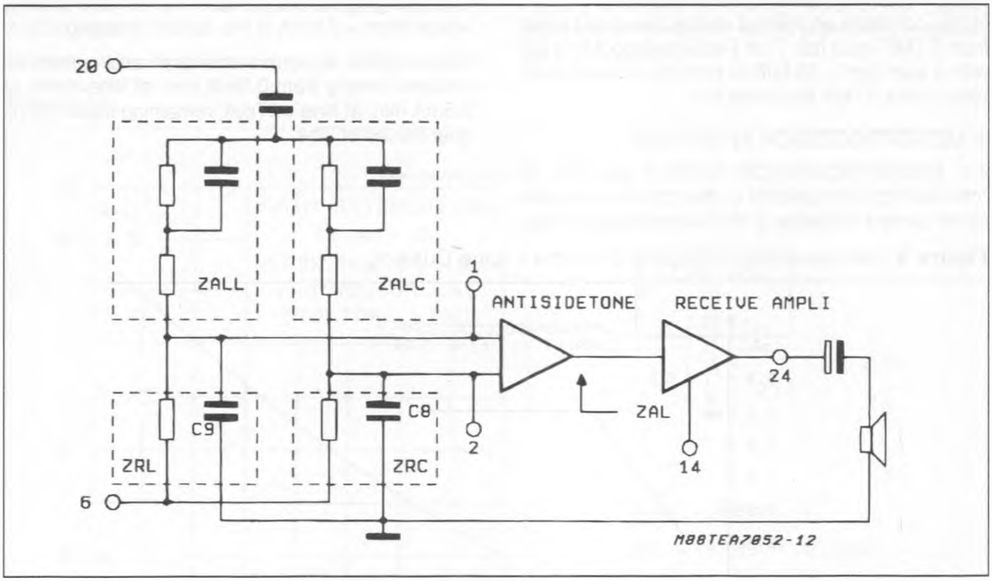
2.3. SENDING MUTE. In normal speech operation (Vmute < 0.8V), the signal at Microphone Input (pin 8) is amplified to Vline (pin 20) with the gains Gec (short line), Gel (long line) or intermediate, depending on Iline.

In sending mute condition (Vmute > 1.6V) these gains are reduced of at least 60dB. In the same condition DTMF input (pin 7) is activated, with gain Gmf to the line independent from Iline.

2.4. ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented at pin 5 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2.).

3. RECEIVE CHAIN

Figure 8.



3.1. A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 24, have a reduction of 6dB when Iline moves from 27mA to 42mA.

3.2. SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize sidetone both at long and short lines.

Before entering pins 1 and 2, the received signal is attenuated by two attenuating networks :

- Zall / Zrl to pin 1 for long lines sidetone compensation,
- Zalc / Zrc to pin 2 for short lines sidetone compensation.

Zrl and Zrc define the total receive gains :

a) $\frac{V\,24}{V\,20} = Grl \times \frac{Zrc}{Zrl + Zall}$ for long lines

b) $\frac{V\,20}{V\,24} = Grc \times \frac{Zrc}{Zrc + Zalc}$ for short lines

Zall and Zalc define the sidetone compensation of the circuit.

The equivalent balancing impedance is given by the formula :

$$Zal = K \times Zalc + (1 - K) \times Zall$$

where K = 0 at Iline = 27mA or lower (long line)

K varies from 0 to 1 with Iline between 27mA and 42mA,

K = 1 at Iline = 42mA or higher (short line).

Calculations to define Zall and Zalc are :

a) $Zall = 70 \times R5 \times \frac{Zline(long) // Zext // Zint // Zout}{Zout}$

b) $Zalc = 70 \times R5 \times \frac{Zline(short) // Zext // Zint // Zout}{Zout}$

where :

- Zext = R6 // C4 // (Zelectret) (at pin 20)
- Zint = 10Kohms // 8.5nF (internal impedance)
- Zout = 10.65 x Z4 (at pin 3 ; see paragr. 2.2.)
- Zline (short) and (long) are the impedances of the line at 0Km and 3.5Km.
- R5 = 5.1Kohm ± 1 %

3.3. AC Impedance. The total AC impedance of the circuit to the line is :

Zpar = Zout//Zint//Zext//Zalc//Zall (see par. 2.2. and 3.2.)

= Zout//Zint//Zext (Zalc, Zall Zpar)

3.4. RECEIVE MUTE (and confidence level). When the receive channel is muted (Vpin 14 > 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from DTMF input (pin 7) to Receive Output (pin 24) with a gain Gmf = 38.5dB to provide acoustic feedback of the DTMF transmission.

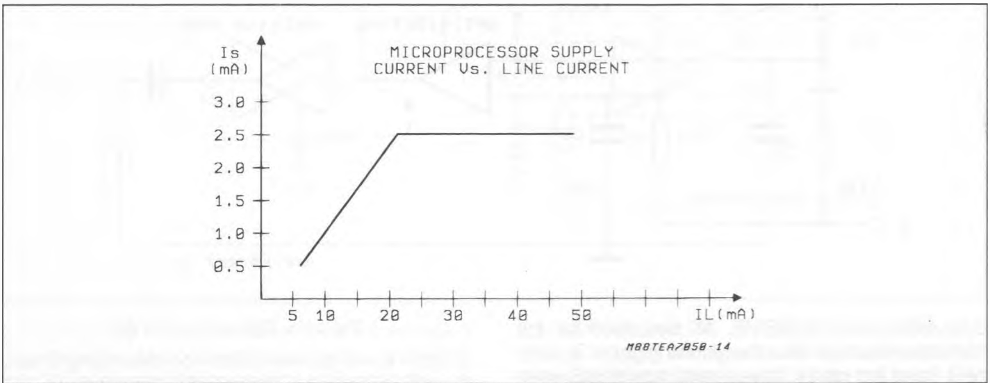
4. MICROPROCESSOR INTERFACE

4.1. MICROPROCESSOR SUPPLY (pin 23). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 23) to charge quickly the external capacitor C3.

This charging current is : Icpm = 0.7 x (Iline - Idem), where Idem = 2.6mA is the current charging C1.

Vmp = 3.95V in normal operation and current increases linearly from 0.5mA min, at Iline=6mA, to 2.5mA min, at Iline = 27mA, remaining stable for higher values of Iline.

Figure 9 : Microprocessor Supply Current vs. Line Current.

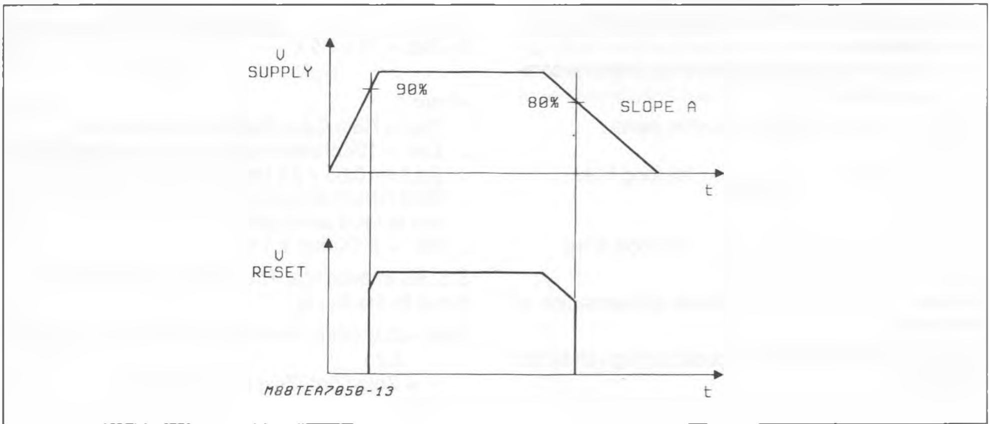


4.2. MICROPROCESSOR RESET (pin 16). The Microprocessor Reset becomes active when Vmp overcomes 85 % of its nominal level.

It becomes low when Vmp undergoes 84 %.

Slope A is related to C3, I1mp (internal consumption) and to the external load (microprocessor or dialer).

Figure 10.

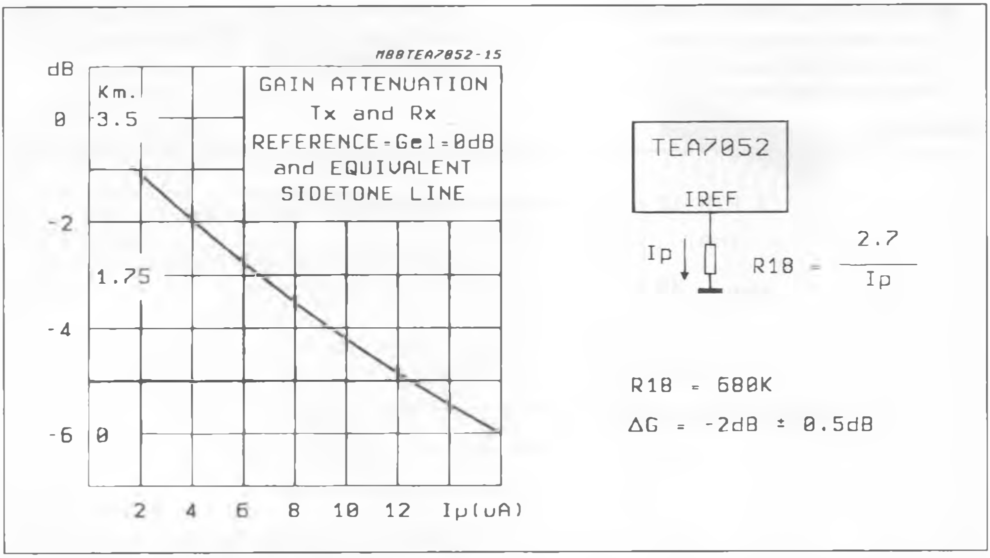


5. PUBLIC / PRIVATE

5.1. A.G.C. OFF (pin 10). An external resistor, R18, applied between pin 10 and ground disconnects the AGC control.

Sending, receiving gain and sidetone compensation are now independent of the line length and the value of the current Ip, flowing through R18, defines the length of the line for which sidetone is optimized (Ip = 2.7V / R18).

Figure 11.



5.2. SECRET FUNCTION FOR PRIVATE (pins 11 & 14). The two separate Mute pins allow "Secret Function" (only microphone muted).

As the two controls have different threshold levels, they can be operated :

a) separately through two different control logic,

b) connected in short circuit with a three levels logic (Vm = 0V speech mode ; Vm = 1.8V microph mute ;
Vm = 3V all mute).

6. POWER MANAGEMEN AND HANDS-FREE INTERFACE

6.1. Power Management (pin 12). Most of the DC current available from the line will be delivered by the speech circuit at the output Isource (pin 12) through an internal current generator.

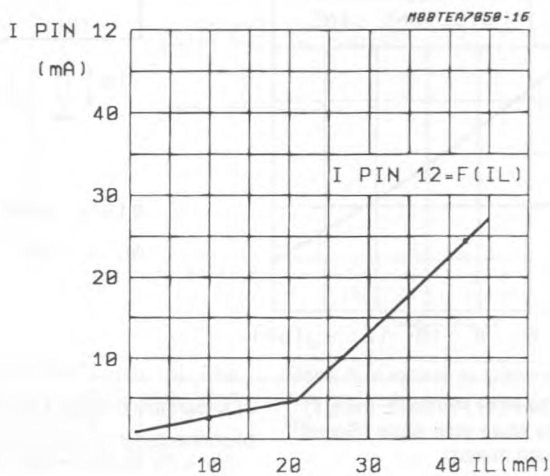
Typical values of this current, Iea, are :
- Iea = (0.3 x Iline) for Iline < 22mA
- Iea = (0.9 x Iline 13mA) for Iline > 22mA

(ex : Iline = 16mA then Iea = 4.8mA
Iline = 30mA then Iea = 14.0mA
Iline = 60mA then Iea = 41.0mA

The voltage level at pin 12 must be defined by an external regulator (i.e. : zener) and, if necessary, filtered with a capacitor (47 to 220 microF).

In case Vline (at pin 20) approaches V at pin 12, then the internal current source switches off and its DC current is shunt to ground through an internal complementary generator, thus avoiding and negative effect on the AC and DC impedances of the telephone set application.

Figure 12.



6.2. EXTRA RECEIVE OUTPUT (pin 4). The Extra Receive Signal is active also in Receive Mute condition, so allowing the transit of the receive signal from the speech circuit to an external hands-free system even when the earpiece is muted.

The gain at this pin is 30dB lower than standard Receive Output (pin 24).