Signetics

TDA8443, TDA8443A
RGB/YUV Switch

Preliminary Specification

Linear Products

DESCRIPTION

The TDA8443/8443A is intended to be used in color TV sets which have more than one base-band video source. The IC has two sets of inputs. The first (Inputs 1) is intended for the internal video signals (R-Y), Y, (B-Y), and the associated synchronization pulse coming from the color decoder; the second (Inputs 2) is intended for external video signals R, G, B, and the associated synchronization pulse coming from the accessory inputs. The latter ones (Inputs 2) can also consist of the video signals (R-Y), Y, (B-Y), and the associated synchronization pulse. The RGB signals at Inputs 2 can also be matrixed internally into the luminance signal Y and the color-difference signals (R-Y) and (B-Y) before they become available at the outputs. By means of I^2C bus mode or manual control (control by DC voltages), one of these inputs can be selected and will be available at the outputs. The IC contains three pins for programming the sub-address; this means that within one TV set the system can be expanded up to seven ICs. The TDA8443 is designed to be used with the CCTV levels, while the TDA8443A is designed to be used for the standard decoder signal levels.

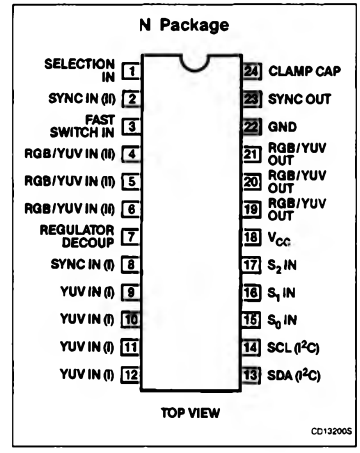
FEATURES

- **Two RGB/YUV selectable clamped inputs with associated sync**
- **An RGB/YUV matrix**
- **3-State switching with an OFF state**
- **Four amplifiers with selectable gain**
- **Fast switching to allow for mixed mode**
- **I^2C or non-I^2C mode (control by DC voltages)**
- **Slave receiver in the I^2C mode**
- **External OFF command**
- **System expansion possible up to 7 devices**

APPLICATIONS

- **TV receivers**
- **Video switching**

PIN CONFIGURATION



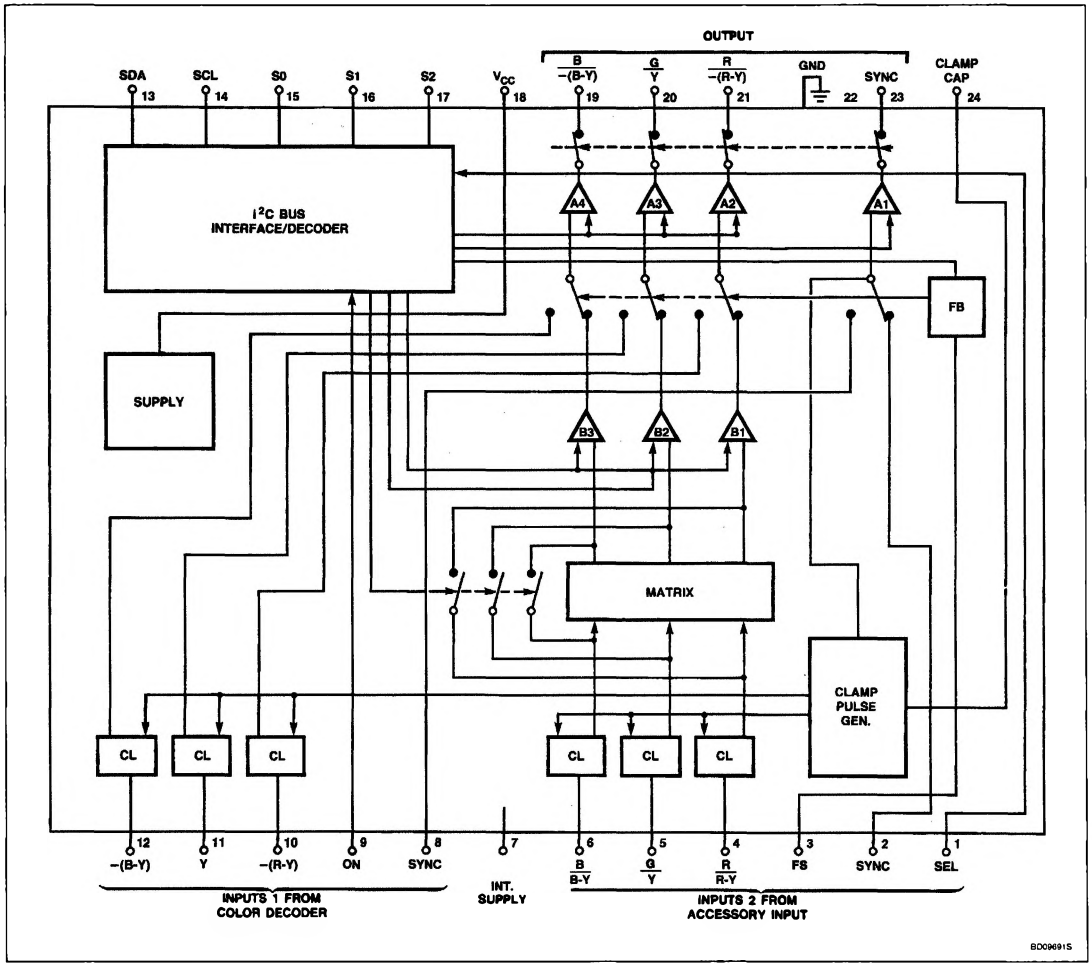
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101)	0 to +70°C	TDA8443N
24-Pin Plastic DIP (SOT-101)	0 to +70°C	TDA8443AN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNIT
T_{STG}	Storage temperature range		−65 to +150	°C
T_A	Operating ambient temperature range		0 to +70	°C
V_{18-7}	Supply voltage		14	V
P_D	Total power dissipation			W
T_{JMAX}	Maximum junction temperature		125	°C
V_{SDA}	Input voltage range	Pin 13	−0.3 to 14	V
V_{SCL}		14	−0.3 to 14	V
		other pins	−0.3 to V_{CC}+0.3	V
I_{OMAX}	Maximum output current		TBD	mA

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = 12V$, unless otherwise specified.

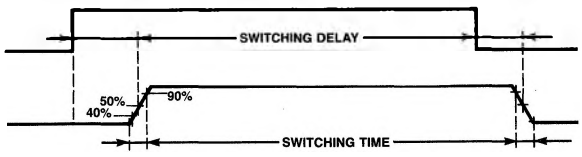
SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{18-7}	Supply voltage	10		13.2	V
I_{18}	Supply current		TBF	TBF	mA
RGB/YUV channels					
	Absolute gain difference with respect to programmed value		0	10	%
	Relative gain difference between any 2 channels of one input		0	5	%
I_{IN}	Input current		TBF	0.3	μA
Z_{OUT}	Output impedance		TBF	30	Ω
	3dB bandwidth (mode 0 or 2)		10		MHz
	3dB bandwidth mode 1		10		MHz
	Mutual time difference at output if all inputs of one source are connected together		TBF	25	ns
	Maximum output amplitude of YUV signals	2.8			V_{P-P}
	Crosstalk between inputs of same source, at 5MHz[1]			−30	dB
	Crosstalk between different sources			−50	dB
	Isolation (OFF state) at 10MHz	50			dB
	Differential gain at nominal output signals: R-Y = $1.05V_{P-P}$ B-Y = $1.33V_{P-P}$ Y = $0.34V_{P-P}$			10	%
S/N	Signal-to-noise ratio at nominal input	50			dB
BW	Bandwidth = 5MHz[2]				
	Supply voltage rejection[3]	50			dB
	DC level of outputs during clamp		5.3		V
Sync channels					
	Gain difference with respect to programmed value			10	%
BW	3dB bandwidth		TBF		MHz
	Input amplitude of sync pulse for proper operation of clamp pulse generator	0.2		2.5	V_{P-P}
Z_{OUT}	Output impedance		TBF	30	Ω
	Maximum output amplitude (undistorted)	2.5			V_{P-P}
	DC level on top of sync pulse at output	TBF	1.8	TBF	V
I^2C bus inputs/outputs					
	SDA input (Pin 13)				
	SCL input (Pin 14)				
V_{IH}	Input voltage High	3		V_{CC}	V
V_{IL}	Input voltage Low	−0.3		1.5	V
I_{IH}	Input current High			10	μA
I_{IL}	Input current Low			10	μA
	SDA output (open-collector)				
V_{OL}	Output voltage Low at IO-L = 3mA			0.4	V
I_{OL}	Maximum output sink current		5		mA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ and $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sub-address inputs S0 (Pin 15), S1 (Pin 16), S2 (Pin 17)					
V_{IH}	Input voltage High	3		V_{CC}	V
V_{IL}	Input voltage Low	−0.3		0.4	V
I_{IH}	Input current High			TBF	μA
I_{IL}	Input current Low			TBF	μA
Fast switching pin					
V_{3-7}	Input voltage High	1		3	V
V_{3-7}	Input voltage Low	−0.3		0.4	V
I_3	Input current High			TBF	μA
I_3	Input current Low			TBF	μA
	Switching delay[4]			TBF	
	Switching time[4]			TBF	
SEL pin					
V_{1-7}	Input voltage High	3		V_{CC}	V
V_{1-7}	Input voltage Low	−0.3		0.4	V
I_1	Input current High			TBF	μA
I_1	Input current Low			TBF	μA
ON pin					
V_{9-7}	Input voltage High	3		V_{CC}	V
V_{9-7}	Input voltage Low	−0.3		1.5	V
I_9	Input current High			TBF	μA
I_9	Input current Low			TBF	μA

NOTES:

1. Crosstalk is defined as the ratio between the output signal originating from another input and the nominal output signal on the same output.
2. $S/N = 20\log \frac{V_{OP-P}}{V_O \text{ noise RMS } B = 5MHz}$.
3. Supply voltage rejection $= 20\log \frac{V_R \text{ supply}}{V_R \text{ on output}}$.
4. Fast switching input signal
   Output signal: YUV
   Input : 0V input 1, mode 2
   0.75V RGB input 2, mode 1



FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs: input 1 from the color decoder (color difference signals), and input 2 from the accessory input, RGB, or possibly YUV, both with associated synchronization inputs.

In the RGB mode, the signals are matrixed internally to color difference signals for further processing in a control circuit (e.g., TDA8461).

The inputs are clamped, thus the clamp pulse is internally derived from the sync signals. The outputs can be made high-ohmic (OFF) in order to be able to put several circuits in parallel.

Control

The circuit can be controlled by an I^2C bus or directly by DC voltages. The fast switching input can be operated by Pin 16 of the accessory input.

I^2C BUS MODE

The protocol for the TDA8443 for I^2C bus mode is:

STA	A6	A5	A4	A3	A2	A1	A0	R/W	AC	D7	D6	D5	D4	D3	D2	D1	D0	AC	STO

STA : Start condition
A6 : 1 } fixed address bits
A5 : 1 }
A4 : 0 }
A3 : 1 }
A2 : Sub-address bit set by S2
A1 : Sub-address bit set by S1
A0 : Sub-address bit set by S0
R/W : Read/Write bit (= 0 only write mode allowed)

AC : Acknowledge, generated by the TDA8443
D7 : MOD1 } mode control bits, see Table 2
D6 : MOD0 }
D5 : G2 }
D4 : G1 } gain control bits, see Table 4
D3 : G0 }
D2 : PRIOR, priority bit
D1 : ON/OFF bit
D0 : ON/OFF active bit

Table 1. Sub-Addressing

SLAVE ADDRESS BITS			ADDRESS SELECT PINS		
A2	A1	A0	S2	S1	S0
0	0	0	GND	GND	GND
0	0	1	GND	GND	V_{CC}
0	1	0	GND	V_{CC}	GND
0	1	1	GND	V_{CC}	V_{CC}
1	0	0	V_{CC}	GND	GND
1	0	1	V_{CC}	GND	V_{CC}
1	1	0	V_{CC}	V_{CC}	GND
1	1	1	V_{CC}	V_{CC}	V_{CC}

NOTE:
Non-I^2C bus operation, see Table 5.

Table 2. Mode Control

MOD1	MOD0	MODE	FUNCTION
0	0	0	Inputs 2 are selected directly
0	1	1	Inputs 2 are selected via RGB/YUV matrix
1	0	2	Inputs 1 are selected directly
1	1	3	Reserved; not to be used

Table 3. Priority Fast Switching Action

PRIOR	FS	MODE SELECTED
0	X	As set by mode control (Table 2)
1	0.4V	Mode 2
1	1 - 3V	Mode 1 if mode 1 is selected Mode 0 if mode 0 or 2 is selected

Table 4. Gain Settings (see Block Diagram)

G2	G1	G0	TDA8443/C3			TDA8443A/C3	
			A1	A2, A3, A4	B1, B3	B1, B3	B2
0	0	0	1	1	−0.6	−1	0.45
0	0	1	1	1	1	1	1
0	1	0	Reserved; not to be used				
0	1	1	1	1	−0.6	−1	0.45
1	0	0	2	2	−0.6	−1	0.45
1	0	1	2	1	1	1	1
1	1	0	2	2	1	1	1
1	1	1	2	1	−0.6	−1	0.45

NOTES:

Matrix equations: relations between output and input signals of the matrix

$Y = 0.3R + 0.59V + 0.11B$

$R\text{-}Y = 0.7R - 0.59V - 0.11B$

$B\text{-}Y = -0.3R - 0.59V + 0.89B$

ON BIT

ON	FUNCTION
0	OFF, no output signal, outputs high-ohmic
1	ON, normal functioning

OFFACT-ON (Pin 9) Function

OFFACT	ON	FUNCTIONING
0	L	OFF
0	H	In accordance with last defined D7 – D1 (may be entered while OFF = L)
1	X	In accordance with last defined D7 – D1

POWER-ON RESET

When the circuit is switched on in the I^2C mode, bits D0 – D7 are set to zero.

Table 5. Non-I^2C Bus Mode (S2 = S1 = S0 = 0)

CONTROL			MODE SWITCHED BY FS	GAIN SETTINGS				
				TDA8443			TDA8443A	
SDA	SCL	SEL		A1	A4, A3, A2	B1, B3	B1, B3	B2
L	L	L	2/0	1	1	1	1	1
L	L	H	2/0	1	2	1	1	1
L	H	L	2/1	1	1	−0.6	−1	0.45
L	H	H	2/0	1	1	−0.6	−1	0.45
H	L	L	2/0	2	1	1	1	1
H	L	H	2/0	2	2	1	1	1
H	H	L	2/1	2	1	−0.6	−1	0.45
H	H	H	2/0	2	1	−0.6	−1	0.45

Fast Switching Input

F S	MODE SELECTED
⩽0.4V	Mode 2
1 – 3V	Mode 0 or 1 as set by control

ON Input

ON	FUNCTION
L	OFF, no output signal, outputs high-ohmic
H	Functioning as determined in Table 5

I²C BUS LOAD CONDITIONS

4kΩ pull-up resistor to +5V; 200pF capacitor to GND.

All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	RATING			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			µs
t_{SU}, t_{STA}	Start condition setup time	4			µs
t_{HD}, t_{STA}	Start condition hold time	4			µs
t_{LOW}	SCL, SDA Low period	4			µs
t_{HIGH}	SCL High period	4			µs
t_R	SCL, SDA rise time			1	µs
t_F	SCL, SDA fall time			0.3	µs
t_{SU}, t_{DAT}	Data setup time (write)	1			µs
t_{HD}, t_{DAT}	Data hold time (write)	1			µs
t_{SU}, t_{CAC}	Acknowledge (from TDA8443) setup time			2	µs
t_{HD}, t_{CAC}	Acknowledge (from TDA8443) hold time	0			µs

NOTE:
Timings t_{SU}, t_{DAT} and t_{HD}, t_{DAT} deviate from the I²C bus specification.
After reset has been activated, transmission may only be started after 50µs delay.

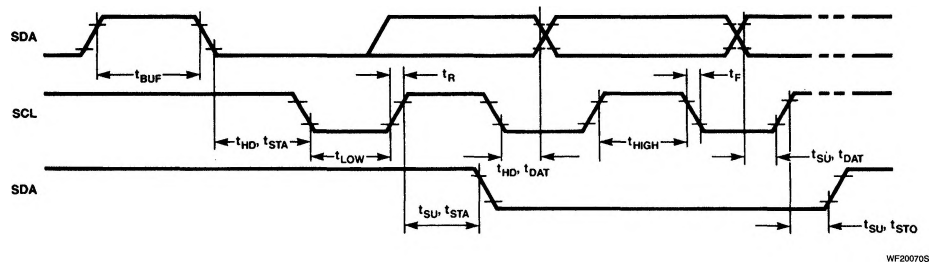


Figure 1. I²C Timing Diagram

Table 6. Application Information

INPUT 1	INPUT 2	OUTPUT	MODE	G2	G1	G0
YUV/S 0.34/−1.33/−1.05/0.3		YUV/S 0.34/−1.33/−1.05/0.6	2	1	1	1
	RGB/S 0.75/0.75/0.75/0.3		1	1	1	1
YUV/S 0.34/−1.33/−1.05/0.3			2	1	0	0
	RGB/S 0.75/0.75/0.75/0.3	YUV/S 0.68/−2.66/−2.1/0.6	1	1	0	0
YUV/S 0.34/−1.33/−1.05/0.3		YUV/S 0.34/−1.33/−1.05/0.6	2	1	0	1
	YUV/S 0.34/−1.43/−1.05/0.3		0	1	0	1
YUV/S 0.34/−1.33/−1.05/0.3		YUV/S 0.68/−2.66/−2.1/0.6	2	1	1	0
	YUV/S 0.34/−1.33/−1.05/0.3		0	1	1	0

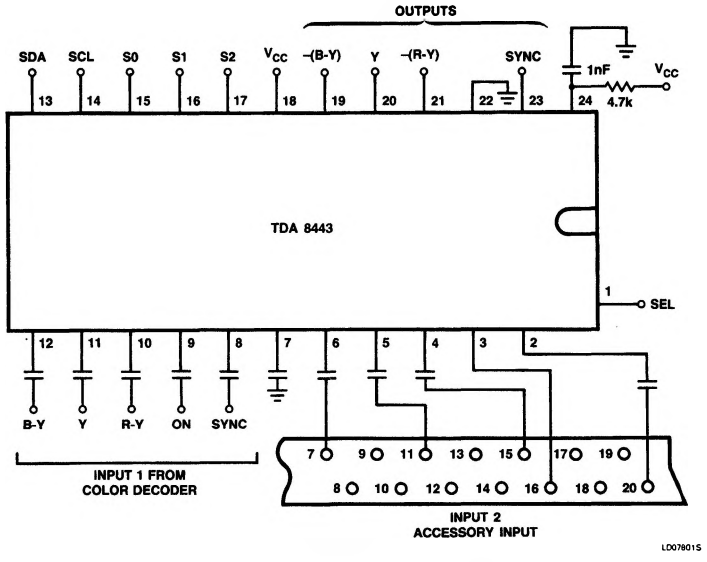


Figure 2. Application of the TDA8443