LINEAR INTEGRATED CIRCUITS



TV SIGNAL IDENTIFICATION CIRCUIT AND AFC INTERFACE

The TDA4431 and the TDA4433 are monolithic integrated circuits in a 14 lead dual-in-line plastic package. They integrate the following functions:

- TV signal identificator - Sync. separator - Threshold detector - Digital Interface - Voltage regulator

They are intended for use in Electronic Program Memory tuning systems, the TDA4431 in conjunction with M193B1, while the TDA4433 with M293B1. The circuits features are:

- Identification of true TV stations only.
- Low impedance output of the identification signal.
- Digital control signal for automatic search and AFC operation.
- Thermal compensation of the voltage regulator.

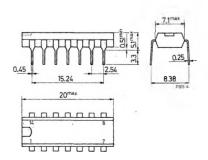
ABSOLUTE MAXIMUM RATINGS

V.	Supply voltage (pin 1)	16	v
V ₃	Voltage at pin 3	16	v
V ₁₃	Voltage at pin 13	–5 to +6	v
12	Pin 2 current (TDA4431)	± 1	mΑ
1 ₆ ;12	Pin 6 and pin 2 current (TDA4433)	1	mΑ
I ₁₀	Pin 10 current	2	mΑ
I ₁₁	Pin 11 current	2	mΑ
I_{12}^{11}	Pin 12 current	± 2	mΑ
P _{tot}	Total power dissipation at $T_{amb} \leq 70^{\circ}C$	800	mW
T _{stg} , T _j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBERS: TDA 4431 TDA 4433

MECHANICAL DATA

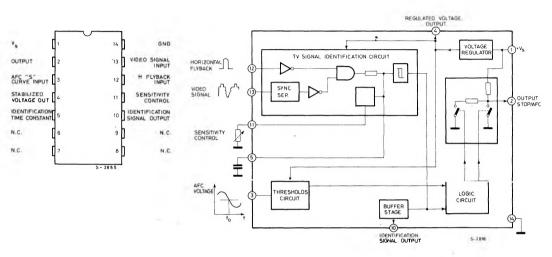
Dimensions in mm



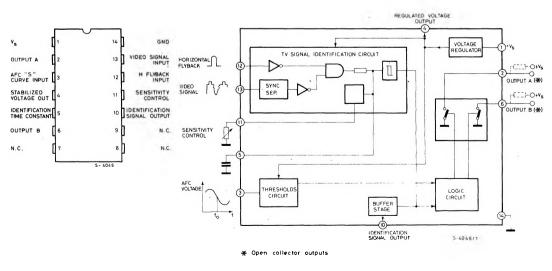


CONNECTION AND BLOCK DIAGRAM (TDA4431)

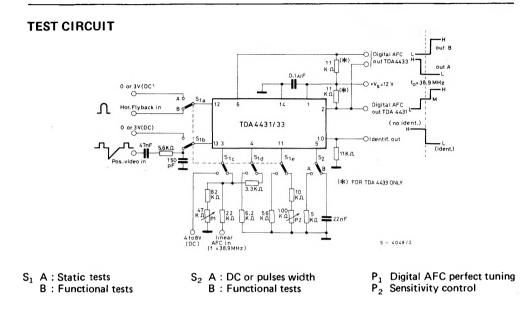
(Top view)



CONNECTION AND BLOCK DIAGRAM (TDA4433) (Top view)







THERMAL DATA

R _{thj-amb}	Thermal resistance junction-ambient	max	100	°C/W
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ELECTRICAL CHARACTERISTICS (refer to the test circuit; $V_s = 12V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Parameter		Test conditions	Min.	Тур.	Max.	Unit
Vs	Supply voltage range (pin 1)		10.8		14.5	V
۱ _s	Supply current (pin 1)	V _s = 1 4 .5V			30	mA
V ₂	Output voltage: low	f _{tuning} < f _o			0.8	V
	medium	$f_{tunins} = f_0$ V _s = 10.8 to 14.5	5.5		8.5	v
	high (TDA 44 31)	f _{tuning} > f _o	V _s -0.5		-	v
V ₂	Output voltage	$f_{tuning} < f_0 I_2 = 1mA$	V _s -0.5			v
		f _{tuning} = f _o			0.8	v
	(TDA4433)	f _{tuning} > f _o			0.8	v



ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit	
V ₆	Output voltage		$f_{tuning} < f_0 $ $I_6 = 1$	1mA			0.8	v
			$f_{tuning} = f_0 \qquad I_6 = 1$	1mA			0.8	V
	(TDA 4433)		f _{tuning} > f _o		V _s -0.5			V
1 ₂	Output current (TDA4431)						± 25	μA
V ₃	Input voltage ra	ange			4		8	V
V _{3U}	Upper threshold (see fig. 2)	d voltage			V ₄ -25	∨₄	V ₄ +25	mV
V _{3L}	Lower threshol (see fig. 2)	d voltage			V ₄ -425	V₄-400	V ₄ -375	mV
R ₃	Input resistance	e	V ₃ = V ₄		1.4			MΩ
V ₄	Regulated volta	ige	I ₄ = 1mA			6.6		v
14	Output current						1	mA
R ₄	Output differer	ntial resistance				60		Ω
$\frac{\Delta V_4}{\Delta T_s}$	Regulated volta	age thermal drift			·		± 2	mV/°C
V ₁₀	Identification	no identification	I ₁₀ = 1mA		V _s -1.3	-		v
	output voltage	identification					20	m∨
R ₁₀	Output resistan	ce				100		Ω
V ₁₂	Switch off thre	shold voltage					1	v
I ₁₂	Input flyback o	urrent			0.5		1.5	mA
R ₁₂	Input resistance	9	V ₁₂ = 3V			10		κΩ
t _{fly}	Flyback pulse of	duration			10		17	μsec.
t	Time delay bet edges of flybac sync. pulse				0		3.5	μ sec.
V ₁₃	Video input sig (peak to peak)	nal			2.5		4.5	v
V ₁₃	Sync. pulse am (above black le				0.52			v
R ₁₃	Input resistance	9					1.5	KΩ



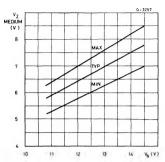
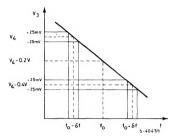


Fig. 1 - Medium output Voltage Vs. Supply voltage.

Fig. 2 - Digital AFC threshold voltage vs. frequency.



Input Voltage	TDA4431	τι	DA4433
(V ₃)	Output voltage	Output voltage	Output voltage
	(V ₂)	(V ₂)	(V ₆)
V ₃ > V ₄	Low level	High level	Low level
$V_4-0.4V < V_3 < V_4$	Medium level	Low level	Low level
$V_3 < V_4-0.4V$	High level	Low level	High level

APPLICATION INFORMATION (refer to the block diagram)

TV signal identification circuit:

The circuit recognizes only TV signals by checking logically during one line the coincidence between the horizontal flyback pulse and the pulse detected by a sync. separator.

The signal identification is carried out by charging the capacitor connected to pin 5; when the capacitor voltage overcomes a fixed threshold voltage, a Schmitt trigger switches and enables the AFC control. If a TV signal is recognized, the capacitor is slightly charged every line and its voltage reaches the threshold after a number of line which is defined by the value of the capacitor itself. The sensitivity of the identification circuit, hence the number of lines required to charge the capacitor, can be adjusted by means of the resistor connected between pin 11 and ground.

When the identification has been made, a signal (level L) is available at pin 10.



Threshold circuit:

The circuit detects 3 ranges of AFC voltage and in combination with the TV signal identification circuit drives the electronic switches.

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With a correct TV signal, the output levels corresponding to the 3 ranges are:

	TDA4431	TDA4433		
	(V ₂)	(V ₂)	(∨ ₆)	
f _o – δ f	L	н	L	
fo	м	L	L	
$f_0 + \delta f$	н	L	н	

L = Low level M = Medium level H = High level

Note that the output levels are different for the two devices.

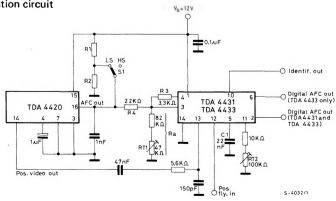
The TDA4431 provides three output levels: low (L), medium (M) and high (H). The output at pin 2 remains at medium level if no video signal is applied at the input or if a video signal is applied but is not identified as a true TV signal.

The TDA 4433 has two separate outputs which can have only two states, high (H) or low (L). The outputs at pin 2 and at pin 6 remain at a low level with no video signal input or with a video signal not identified as a true TV signal. Both pin 2 and pin 6 are open collector outputs and must be pulled-up to the positive supply voltage by external resistors.

Voltage Regulator

The circuit can deliver 1mA and it can be used as D/A converter reference to supply fine tuning voltage.

Fig. 3 - Application circuit



The passive components should be chosen as follows:

- R_1 and $R_2~$: these define the AFC response slope. For R_1 = R_2 = 5.1K Ω , the typical slope is 750/11 KHz/V (with AFC output unloaded).
- S_1 : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.
- R_3 and $R_4~~:$ the ratio $(R_3~+~R_4)/R_3$ defines the digital AFC width (δf) calculated from the linear AFC width ($2\Delta f$). With $V_s=12V$, the relation is:

$$\delta f = 0.036 (2\Delta f) \frac{R_3 + R_4}{R_3}$$

R_{T1} : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is:

$$R_{a} = 33 R_{3}$$

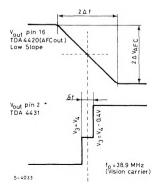
with $R_3 = 3.3K\Omega$, R_a can be a fixed resistor of 110K Ω .

 R_{T2} : by means of this trimmer it is possible to choose the better sensitivity. It is possible to put a fixed resistor at pin 11 in the range of 68 K Ω to 100 K Ω .

To make a better sensitivity adjustment of trimmer R_{T2} , it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field. Furthermore, the action of the syncs separator must be as quick as possible.

In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

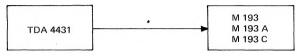
Fig. 4 - Linear and digital AFC



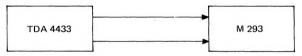


EPM SYSTEM CONFIGURATIONS

1) For 16 channels



2) For 32 channels



3) With microprocessor

