GENERAL DESCRIPTION

The TDA1540 is a monolithic integrated 14-bit digital to analogue converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85 dB in the audio band.

QUICK REFERENCE DATA

Supply voltages				
pin 4	V_{P1}	typ.	5	V
pin 7	V_{N1}	typ.	−5	V
pin 11	V_{N2}	typ.	−17	V
Signal-to-noise ratio (full scale sine-wave) at analogue output (pin 22)	S/N	typ.	85	dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB	
Current settling time	t_{cs}	typ.	0.5	μs
Maximum input bit rate at data input (pin 1)	BR_{max}	min.	12	Mbit/s
Maximum clock frequency at clock input (pin 28)	$f_{cl\,max}$	min.	12	MHz
Full scale temperature coefficient at analogue output (pin 22)	TC_{FS}	typ.	$\pm 30 \cdot 10^{-6}$	K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70	°C
Total power dissipation	P_{tot}	typ.	350	mW

PACKAGE OUTLINES

TDA1540D: 28-lead DIL; ceramic (cerdip) (SOT-135A).
TDA1540P: 28-lead DIL; plastic (SOT-117BE).

FUNCTIONAL DESCRIPTION

The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current 4 I of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an a.c. low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents I ($\bar{I}_1$), I ($\bar{I}_2$) and 2I ($\bar{I}_3$) (see Fig. 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Fig. 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be 0 V ± 10 mV. The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Fig. 4.

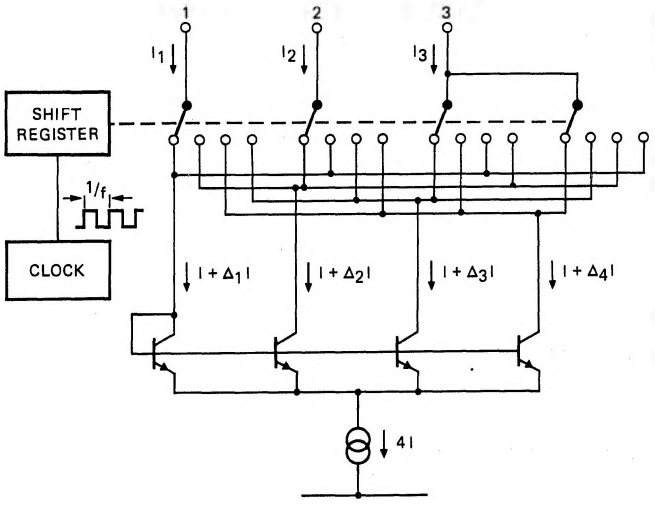

Fig. 1a Circuit diagram of one divider stage.

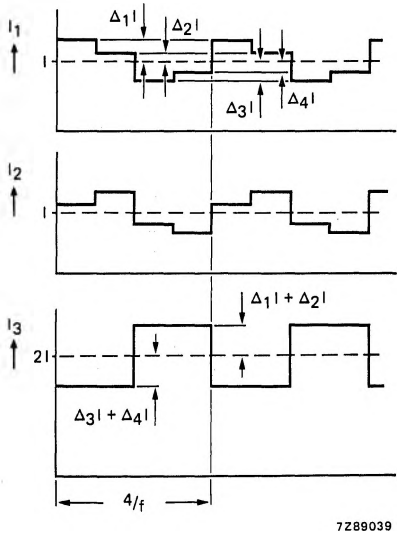

Fig. 1b Waveforms showing output currents I_1, I_2 and I_3 of Fig. 1a.

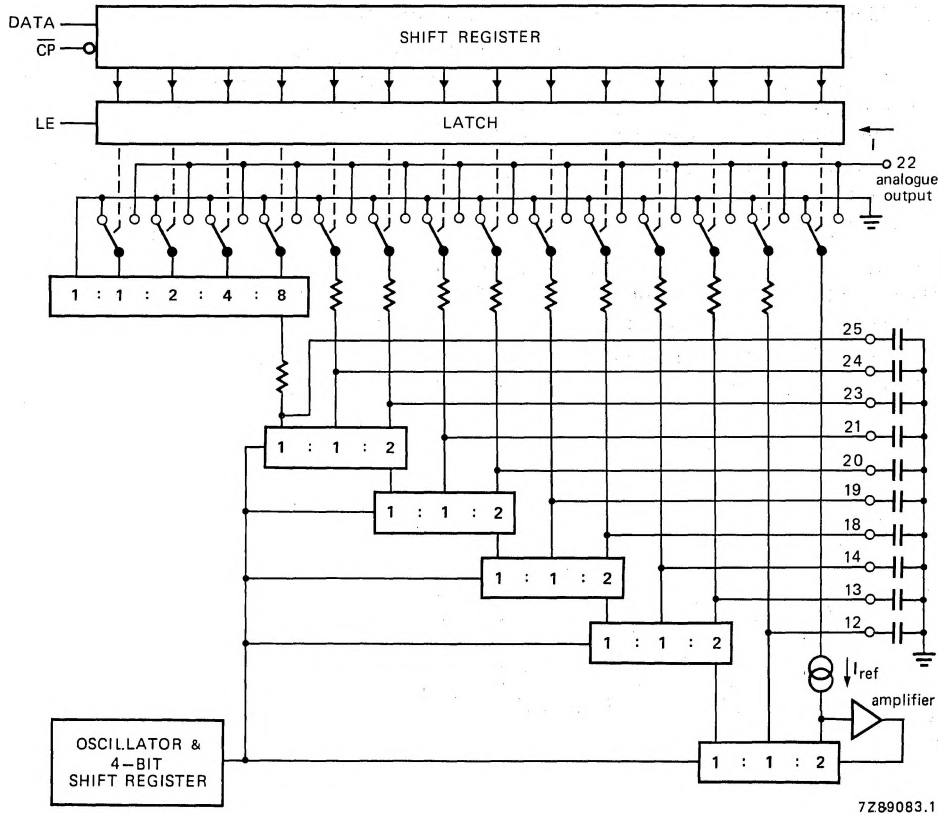

Fig. 2 Functional diagram showing cascading of current division stages.

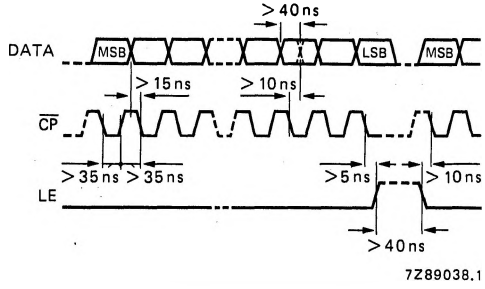

Fig. 3 Format of input signals.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages with respect to GND (pin 6)			
at pin 4	V_{P1}	max.	12 V
at pin 7	V_{N1}	max.	−12 V
at pin 11	V_{N2}	max.	−20 V
at pin 4 with respect to pin 11	$V_{P1}-V_{N2}$	max.	32 V
at pin 7 with respect to pin 11	$V_{N1}-V_{N2}$		−1 to + 20 V
Total power dissipation	P_{tot}	max.	600 mW
Storage temperature range	T_{stg}		−55 to + 125 °C
Operating ambient temperature range	T_{amb}		−25 to + 80 °C

CHARACTERISTICS (see application circuit Fig. 4)

T_{amb} = 25 °C; at typical supply voltages; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages with respect to GND (pin 6)					
at pin 4	V_{P1}	3	5	7	V
at pin 7	V_{N1}	−4.7	−5	−7	V
at pin 11	V_{N2}	−16.5	−17	−18	V
Supply currents					
at pin 4*	I_{P1}	–	12	14	mA
at pin 7	I_{N1}	–	−20	−24	mA
at pin 11	I_{N2}	–	−11	−13	mA
Power dissipation					
Total power dissipation	P_{tot}	–	350	410	mW
Temperature					
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

* When the output current is ½I_{FS} (½ full scale output current).

parameter	symbol	min.	typ.	max.	unit
Data input DATA (pin 1)					
Input voltage HIGH	V_{IH}	2.0	–	7.0	V
Input voltage LOW	V_{IL}	0	–	0.8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0.2	mA
Maximum input bit rate	BR_{max}	12	–	–	Mbits/s
Latch enable input LE (pin 2)					
Clock input $\overline{CP}$ (pin 28)					
Input voltage HIGH	V_{IH}	2.0	–	7.0	V
Input voltage LOW	V_{IL}	0	–	0.8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0.2	mA
Maximum clock frequency	f_{CPmax}	12	–	–	MHz
Oscillator (pins 8 and 9)					
Oscillator frequency at C_{8-9} = 820 pF	f_{osc}	100	160	200	kHz
Analogue output I_{out} (pin 22)					
Output voltage compliance	V_{OC}	−10	–	+ 10	mV
Full scale current	I_{FS}	3.8	4.0	4.2	mA
Zero scale current	$\pm I_{ZS}$	–	–	100	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 30 \times 10^{-6}$	–	K^{-1}
Settling time to ± ½LSB all bits on or off	t_{cs}	–	0.5	–	μs
Signal-to-noise ratio*	S/N	80	85	–	dB

* Signal-to-noise ratio within 20 Hz and 20 kHz of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

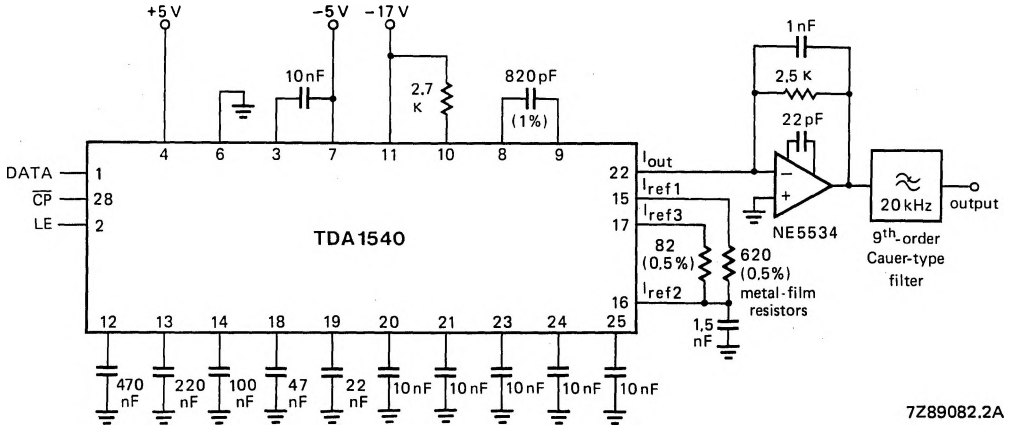

Fig. 4 Application circuit.

PINNING

1	DATA	data input
2	LE	latch enable input
3	V_{ref1}	voltage reference
4	V_{P1}	positive supply
5	i.c.*	frequency compensation on-chip operational amplifier
6	GND	ground
7	V_{N1}	negative supply
8	OSC1	oscillator capacitor
9	OSC2	
10	V_{ref2}	voltage reference
11	V_{N2}	negative supply
12	C1	decoupling binary weighted current sources
13	C2	
14	C3	
15	I_{ref1}	current reference sources
16	I_{ref2}	
17	I_{ref3}	
18	C4	decoupling binary weighted current sources
19	C5	
20	C6	
21	C7	
22	I_{out}	analogue output
23	C8	decoupling binary weighted current sources
24	C9	
25	C10	
26	i.c.*	voltage reference
27	i.c.*	voltage reference
28	$\overline{CP}$	clock pulse input

* i.c.: internally connected.

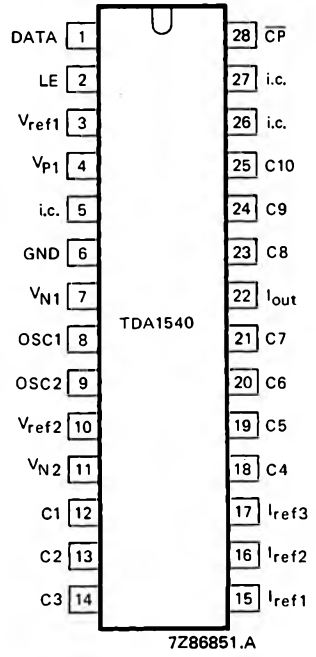

Fig. 5 Pinning diagram.