# LINEAR INTEGRATED CIRCUIT

**TDA1170N**

## LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

The TDA 1170N is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers. **Low-noise meakes this device particularly suitable for use in monitors.** The functions incorporated are:

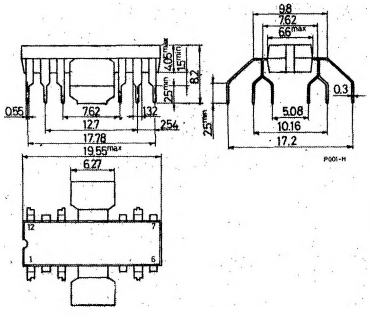
- synchronization circuit
- oscillator and ramp generator
- high power gain amplifier
- flyback generator
- voltage regulator

## ABSOLUTE MAXIMUM RATINGS

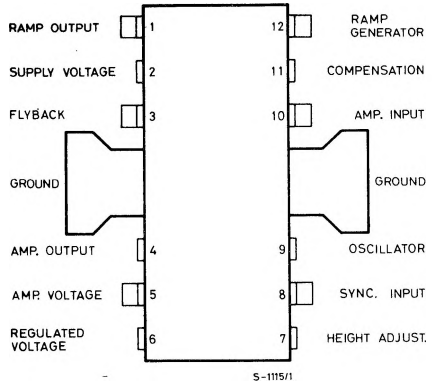
| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage at pin 2 | 35 | V |
| V4, V5 | Flyback peak voltage | 60 | V |
| V10 | Power amplifier input voltage | + 10 | V |
| | | - 0.5 | V |
| $I_o$ | Output peak current (non repetitive) at t = 2 msec | 2 | A |
| $I_o$ | Output peak current at f = 50 Hz t ⩽ 10 μsec | 2.5 | A |
| $I_o$ | Output peak current at f = 50 Hz t > 10 μsec | 1.5 | A |
| $I_3$ | Pin 3 DC current at V4 < V2 | 100 | mA |
| $I_3$ | Pin 3 peak to peak flyback current for f = 50 Hz, $t_{fly}$ ⩽ 1.5 msec | 1.8 | A |
| $I_8$ | Pin 8 current | ± 20 | mA |
| $P_{tot}$ | Power dissipation: at $T_{tab}$ = 90°C | 5 | W |
| | at $T_{amb}$ = 80°C (free air) | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

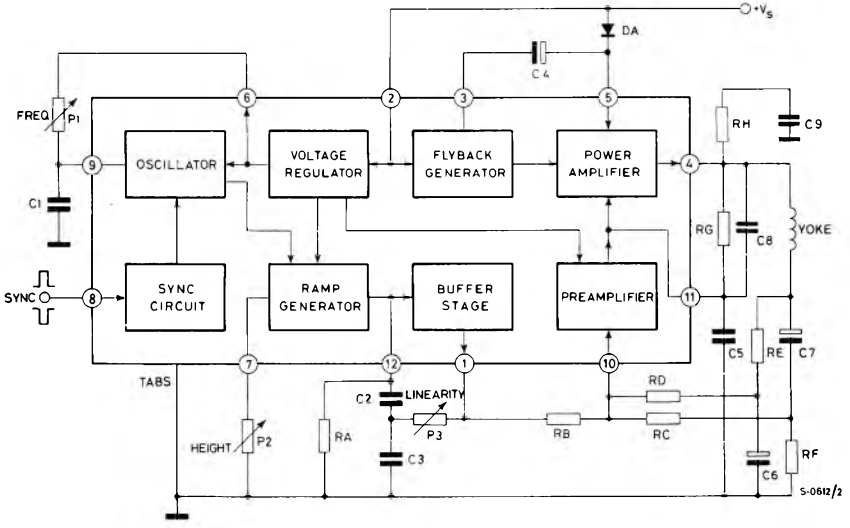
## MECHANICAL DATA

Dimensions in mm



## CONNECTION AND BLOCK DIAGRAMS




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max | 12 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70 | °C/W(°) |

(°) Obtained with tabs soldered to printed circuit with minimized copper area.

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuits, $V_s$ = 35V, $T_{amb}$= 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| $I_2$ | Pin 2 quiescent current | $I_3$ = 0 | | 7 | 14 | mA | 1b |
| $I_5$ | Pin 5 quiescent current | $I_4$ = 0 | | 8 | 15 | mA | 1b |
| $-I_9$ | Oscillator bias current | V9 = 1V | | 0.1 | 1 | μA | 1a |
| $-I_{10}$ | Amplifier input bias current | V10= 1V | | 1 | 7 | μA | 1b |
| $-I_{12}$ | Ramp generator bias current | V12= 0 | | 0.02 | 0.3 | μA | 1a |
| $-I_{12}$ | Ramp generator current | $I_7$ = 20 μA V12= 0 | 19 | 20 | 24 | μA | 1b |
| $\frac{\Delta I_{12}}{I_{12}}$ | Ramp generator non-linearity | ΔV12= 0 to 12V<br>$I_7$ = 20 μA | | 0.2 | 1 | % | 1b |
| $V_s$ | Supply voltage range | | 10 | | 35 | V | – |
| V1 | Pin 1 saturation voltage to ground | $I_1$ = 1 mA | | 1 | 1.4 | V | – |
| V3 | Pin 3 saturation voltage to ground | $I_3$ = 10 mA | | 1.7 | 2.6 | V | 1a |
| V4 | Quiescent output voltage | $V_s$= 10V R1= 10 KΩ<br>R2 = 10 KΩ | 4.17 | 4.4 | 4.63 | V | 1a |
| | | $V_s$= 35V R1= 30 KΩ<br>R2 = 10 KΩ | 8.35 | 8.8 | 9.25 | V | 1a |
| V4L | Output saturation voltage to ground | $-I_4$= 0.1A | | 0.9 | 1.2 | V | 1c |
| | | $-I_4$= 0.8A | | 1.9 | 2.3 | V | 1c |
| V4H | Output saturation voltage to supply | $I_4$ = 0.1A | | 1.4 | 2.1 | V | 1d |
| | | $I_4$ = 0.8A | | 2.8 | 3.2 | V | 1d |
| V6 | Regulated voltage at pin 6 | | 6.1 | 6.5 | 6.9 | V | 1b |
| V7 | Regulated voltage at pin 7 | $I_7$ = 20 μA | 6.2 | 6.6 | 7 | V | 1b |
| $\frac{\Delta V6}{\Delta V_s}$ ; $\frac{\Delta V7}{\Delta V_s}$ | Regulated voltage drift with supply voltage | $\Delta V_s$= 10 to 35V | | 1 | | mV/V | 1b |
| V10 | Amplifier input reference voltage | | 2.07 | 2 2 | 2.3 | V | – |
| R8 | Pin 8 input resistance | V8 ⩽ 0.4V | 1 | | | MΩ | 1a |

Fig. 1 - DC test circuits

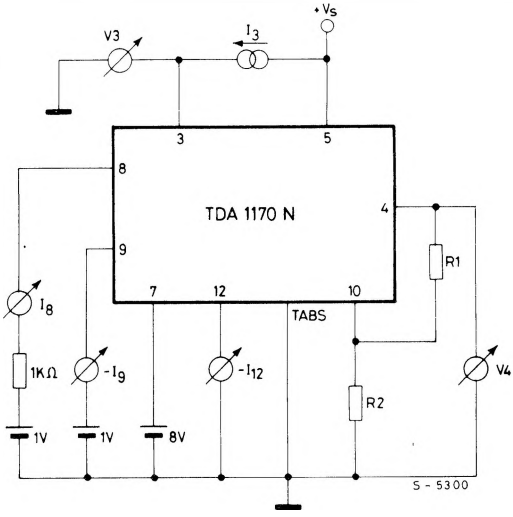



Fig. 1a

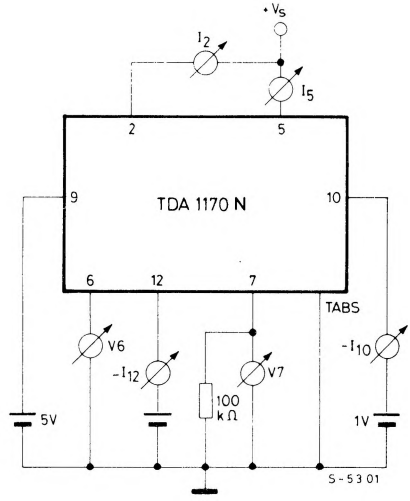



Fig. 1b

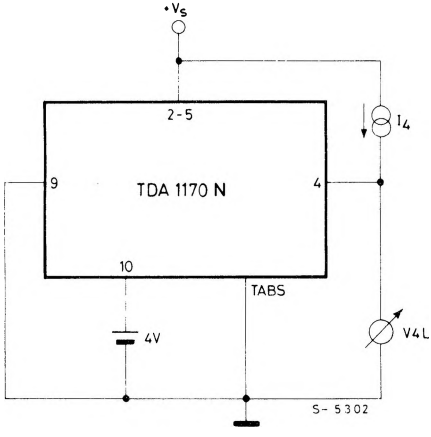



Fig. 1c

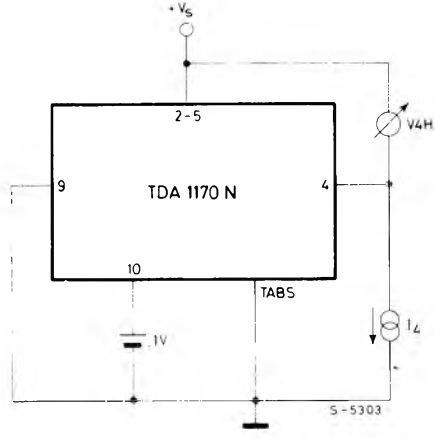



Fig. 1d

## ELECTRICAL CHARACTERISTICS (Refer to the AC test circuit, $V_S$ = 25V; f = 50 Hz; $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | |
| $I_s$ | Supply current | $I_y$ = 1 App | | 140 | | mA |
| $I_8$ | Sync. input current (positive or negative) | | 500 | | | μA |
| V4 | Flyback voltage | $I_y$ = 1 App | | 51 | | V |
| $t_{fly}$ | Flyback time | $I_y$ = 1 App | | 0.7 | | ms |
| $V_{oN}$ | Peak to peak output noise | Bw = 20 ÷ 20.000 Hz | | | 50 | mV |
| $f_o$ | Free running frequency | (P1 + R1) = 300 KΩ<br>C2 = 0.1 μF | | 52.4 | | Hz |
| | | (P1 + R1) = 360 KΩ<br>C2 = 100 nF | | 43.7 | | Hz |
| Δf | Synchronization range | $I_8$ = 0.5 mA | 14 | | | Hz |
| $\frac{\Delta f}{\Delta V_s}$ | Frequency drift with supply voltage | $V_s$ = 10 to 35V | | 0.005 | | Hz/V |
| $\left\lvert\frac{\Delta f}{\Delta T_{tab}}\right\rvert$ | Frequency drift with tab temperature | $T_{tab}$ = 40 to 120°C | | 0.01 | | Hz/°C |

Fig. 2 - AC test circuit

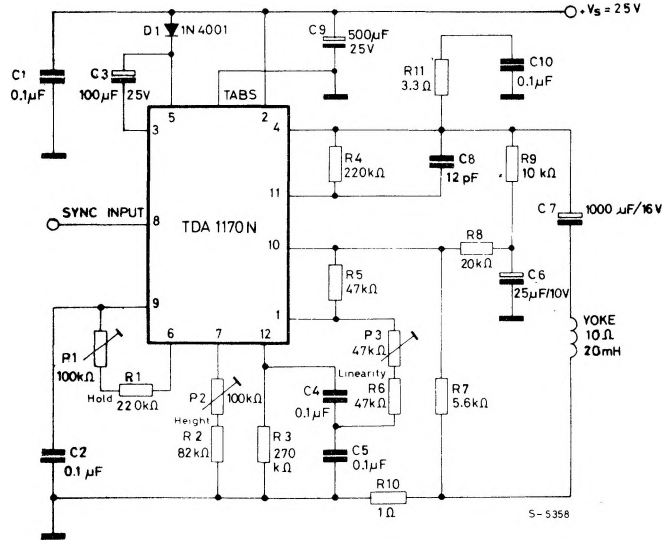


Fig. 3 - PC board and component layout of the AC test circuit (1:1 scale)