#### TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

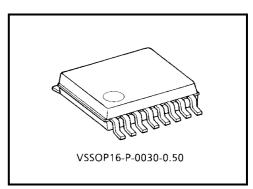
# **TC7MB3253FK**

#### Dual 1-of-4 FET Multiplexer/Demultiplexer

The TC7MB3253FK is high-speed CMOS dual 1-4 Multiplexer/Demultiplexer. The low on resistance of the switch allows connections to be made with minimal propagation delay time.

This device consists of two individual two-inputs multiplexer/demultiplexer with common select inputs (S1, S0). The A inputs is connected to the corresponded B1~B4 outputs determined by the combination both the select inputs (S1, S0) and output enable  $(\overline{OE})$ . When the output enable  $(\overline{OE})$  input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

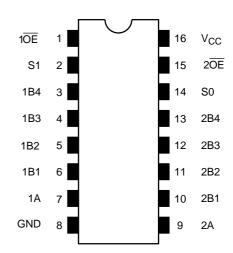


Weight: 0.02 g (typ.)

#### **Features**

- Operating voltage:  $V_{CC} = 4.5 \sim 5.5 \text{ V}$
- High speed:  $t_{pd} = 0.25 \text{ ns (max)}$
- Low on resistance:  $RON = 5 \Omega$  (typ.)
- ESD performance: Machine model >  $\pm 200 \text{ V}$ Human body model >  $\pm 2000 \text{ V}$ 
  - Compatible with TTL outputs (control inputs)
- Package: VSSOP (US16)
- Pin compatible with the 74xx253 type. Functionally equivalent to (FST/CBT) 3253.

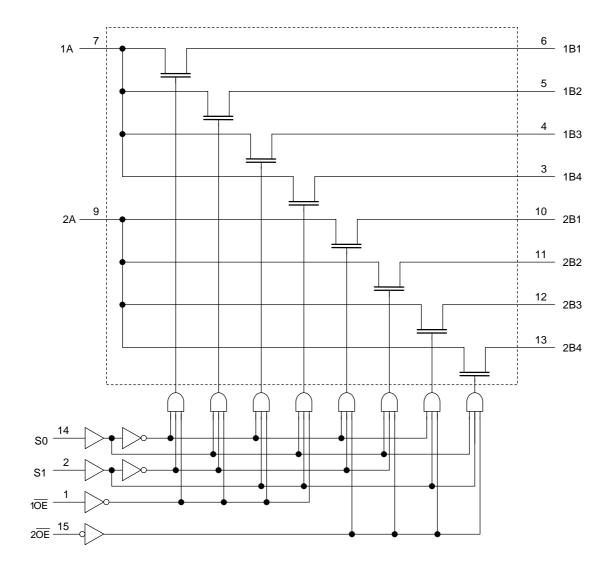
#### Pin Assignment (top view)



# **Truth Table**

Inputs			Function	
ŌĒ	S1	S0	1 diletion	
L	L	L	A port = B1 port	
L	L	Н	A port = B2 port	
L	Н	L	A port = B3 port	
L	Н	Н	A port = B4 port	
Н	Х	Х	Disconnect	

# **System Diagram**



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### **Maximum Ratings**

Characteristics	Symbol	Rating	Unit	
Power supply range	V <sub>CC</sub>	-0.5~7.0	V	
DC input voltage	V <sub>IN</sub>	-0.5~7.0	V	
DC switch voltage	Vs	-0.5~7.0	V	
Input diode current	I <sub>IK</sub>	-50	mA	
Continuous channel current	IS	128	mA	
Power dissipation	PD	180	mW	
DC V <sub>CC</sub> /GND current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA	
Storage temperature	T <sub>stg</sub>	-65~150	°C	

# **Recommended Operating Conditions**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	4.5~5.5	V
Input voltage	V <sub>IN</sub>	0~5.5	V
Switch voltage	Vs	0~5.5	V
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

#### **Electrical Characteristics**

### DC Characteristics ( $Ta = -40 \sim 85$ °C)

Characteristics		Symbol	nbol Test Condition			Min	Typ. (Note1)	Max	Unit
		Syllibol			V <sub>CC</sub> (V)				
Input voltage	"H" level	V <sub>IH</sub>	_		4.5~5.5	2.0	_		V
input voitage	"L" level	V <sub>IL</sub>	_		4.5~5.5	_		0.8	V
Input leakage cu	rrent	I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5 V		4.5~5.5		_	±1.0	μΑ
Power off leakage current		loff	A, B, $\overline{OE} = 0 \sim 5.5 \text{ V}$		0		_	±1.0	μΑ
Off-state leakage current (switch off)		I <sub>SZ</sub>	A, B = $0 \sim 5.5 \text{ V}$ , $\overline{\text{OE}} = \text{V}_{\text{CC}}$		4.5~5.5	_	_	±1.0	μА
On resistance (Note2)			$V_{IS} = 0 V$	$I_{IS} = 64 \text{ mA}$	4.5	_	5	7	
		R <sub>ON</sub>		$I_{IS} = 30 \text{ mA}$	4.5	_	5	7	Ω
			V <sub>IS</sub> = 2.4 V, I <sub>IS</sub> = 15 m/	A	4.5	_	10	15	
Increase in I <sub>CC</sub> per input		Icc	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$		5.5			10	μА
		Δl <sub>CC</sub>	V <sub>IN</sub> = 3.4 V (one input)		5.5	_		2.5	mA

Note 1: Typical values are at  $V_{CC} = 5 \text{ V}$ ,  $Ta = 25^{\circ}C$ .

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

### AC Characteristics ( $Ta = -40 \sim 85$ °C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time	t <sub>pLH</sub>	Figure 1, Figure 2 (Note3)	4.5		0.25	ns
(bus to bus)	t <sub>pHL</sub>	rigure 1, rigure 2 (Notes)	4.5	_	0.23	115
Propagation delay time	t <sub>pLH</sub>	Figure 4 Figure 2	4.5		F 2	
(S to bus)	t <sub>pHL</sub>	Figure 1, Figure 2	4.5	_	5.3	ns
Output enable time	t <sub>pZL</sub>	Figure 4 Figure 2	4.5		F 0	
( OE to bus)	t <sub>pZH</sub>	Figure 1, Figure 3	4.5	_	5.3	ns
Output enable time	t <sub>pZL</sub>	Figure 4 Figure 2	4.5		<b>5</b> 2	
(S to bus)	t <sub>pZH</sub>	Figure 1, Figure 3	4.5	_	5.3	ns
Output disable time	t <sub>pLZ</sub>	Figure 4 Figure 2	4.5			
( OE to bus)	t <sub>pHZ</sub>	Figure 1, Figure 3	4.5	_	5.3	ns
Output disable time	t <sub>pLZ</sub>	Figure 4 Figure 2	4.5		<b>5.0</b>	
(S to bus)	t <sub>pHZ</sub>	Figure 1, Figure 3	4.5		5.3	ns

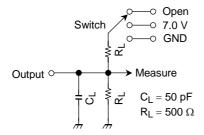
Note 3: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

### **Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Control pin input capacitance ( $\overline{\text{OE}}$ , S)	C <sub>IN</sub>	(Note4)	5.0	3	pF
Switch terminal capacitance (B1~4)	C <sub>I/O</sub>	$\overline{OE} = V_{CC}$ (Note4)	5.0	10	pF
Switch terminal capacitance (A)	C <sub>I/O</sub>	$\overline{OE} = V_{CC}$ (Note4)	5.0	31	pF

Note 4: This parameter is guaranteed by design.

#### **AC Test Circuit**



Parameter	Switch		
t <sub>pLH</sub> , t <sub>pHL</sub>	Open		
t <sub>pLZ</sub> , t <sub>pZL</sub>	7.0 V		
t <sub>pHZ</sub> , t <sub>pZH</sub>	Open		

Figure 1

#### **AC Waveform**

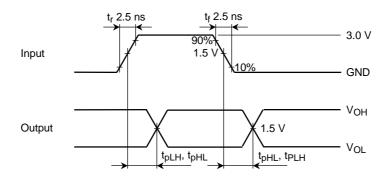


Figure 2 t<sub>pLH</sub>, t<sub>pHL</sub>

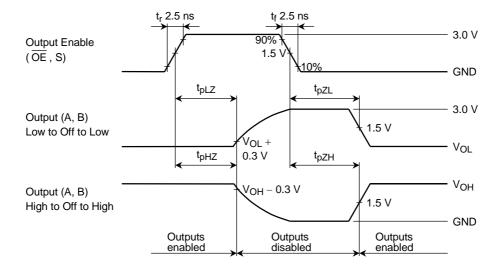
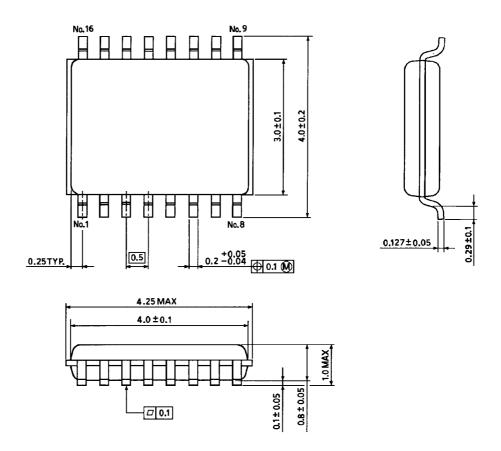


Figure 3  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$ 

# **Package Dimensions**



Weight: 0.02 g (typ.)

2001-09-12

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