TOSHIBA COMPANION CHIP FOR TMPR3922U

TC6358TB(PLUM2)

TECHNICAL DATA

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TOSHIBA COMPANION CHIP FOR TMPR3922U

PLUM2

1. General description

The PLUM2 is a companion chip for TMPR3922. The PLUM2 connect to TMPR3922, integrated digital ASSP for the Personal Information Communicator(PIC).

Figure 3.1 shows a block diagram of PLUM2. The PLUM2 and TMPR3922 consists of the PIC system support logic. The PLUM2 consists of a LCD / CRT controller, PCMCIA controller, Smartmedia controller, I/O bus controller and USB controller.

2. Features

(1) LCD / CRT Controller

● LCDC

Panel : STN / DSTN / TFT

Display : 640 x 480 , 800 x 600

Pixel : 8bit / pixel or 16bit / pixel

Color	:	STN/DSTN	256 color out of 64K	8bit / pixel
			64K color	16bit / pixel
		TFT	256 color out of 256K	8bit / pixel
			64K color	16bit / pixel
Mono	:	STN/DSTN	64grayscale	8bit / pixel

● CRT

Display : 640 x 480 , 800 x 600

Color : 256 color out of 256K 8bit / pixel

64K color 16bit / pixel

RAMDAC : Analog RGB = 6 : 6 : 6

● Function

Simultaneous display CRT / LCD : Ghost image / Same image

BitBlt engine

VRAM : SGRAM (8Mbit / 16Mbit)

Power control function using CKE / CLK

(2) PCMCIA ··· Support 2 slot

PCMCIA Type2

3V / 5V

(3) Smartmedia support ··· Support 1 slot

3V / 5V

(4) I / O bus

ISA-like bus

8 / 16bit

(5) USB ··· Support 2 port

USB Host support

3. System configuration

3.1. System configuration

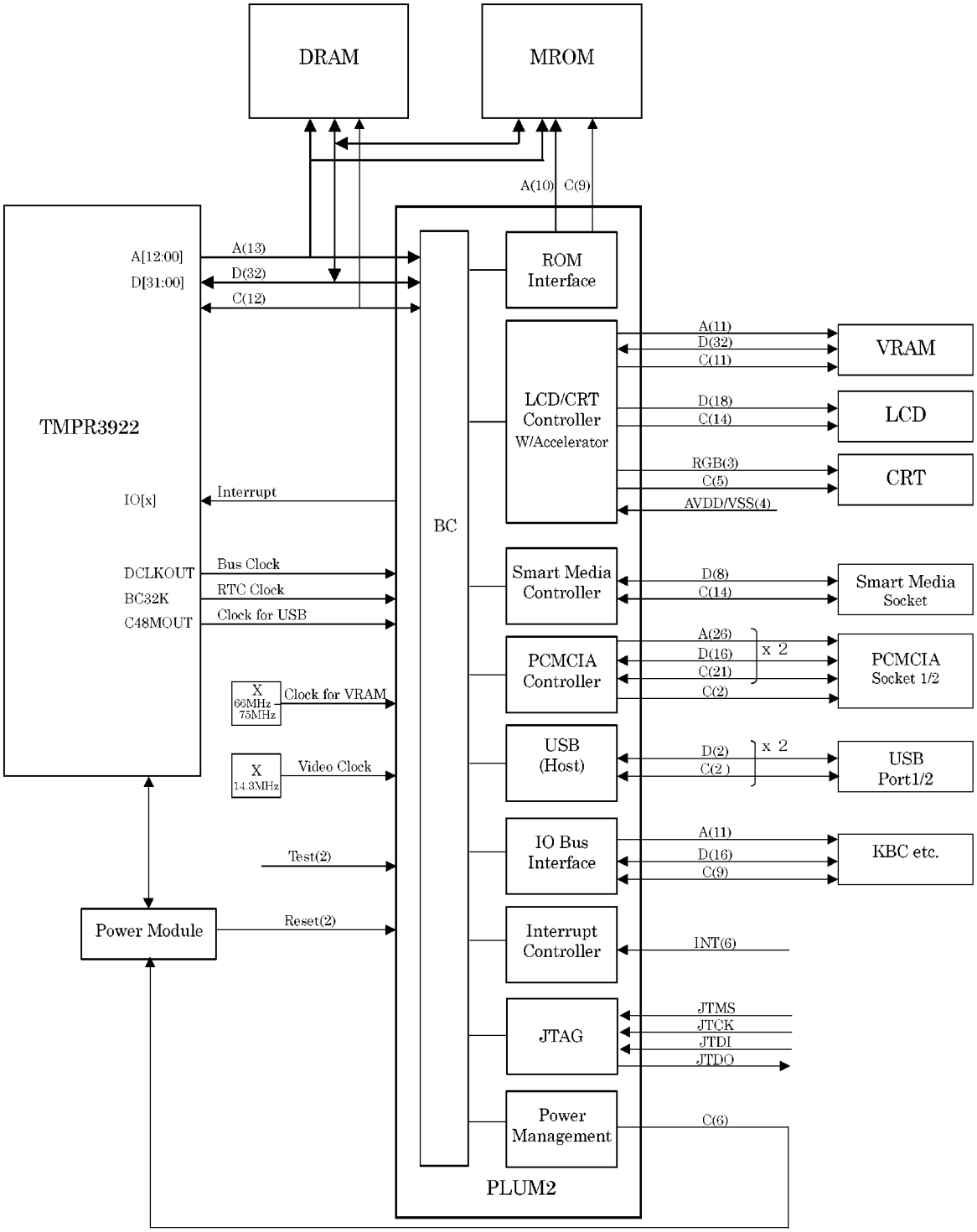
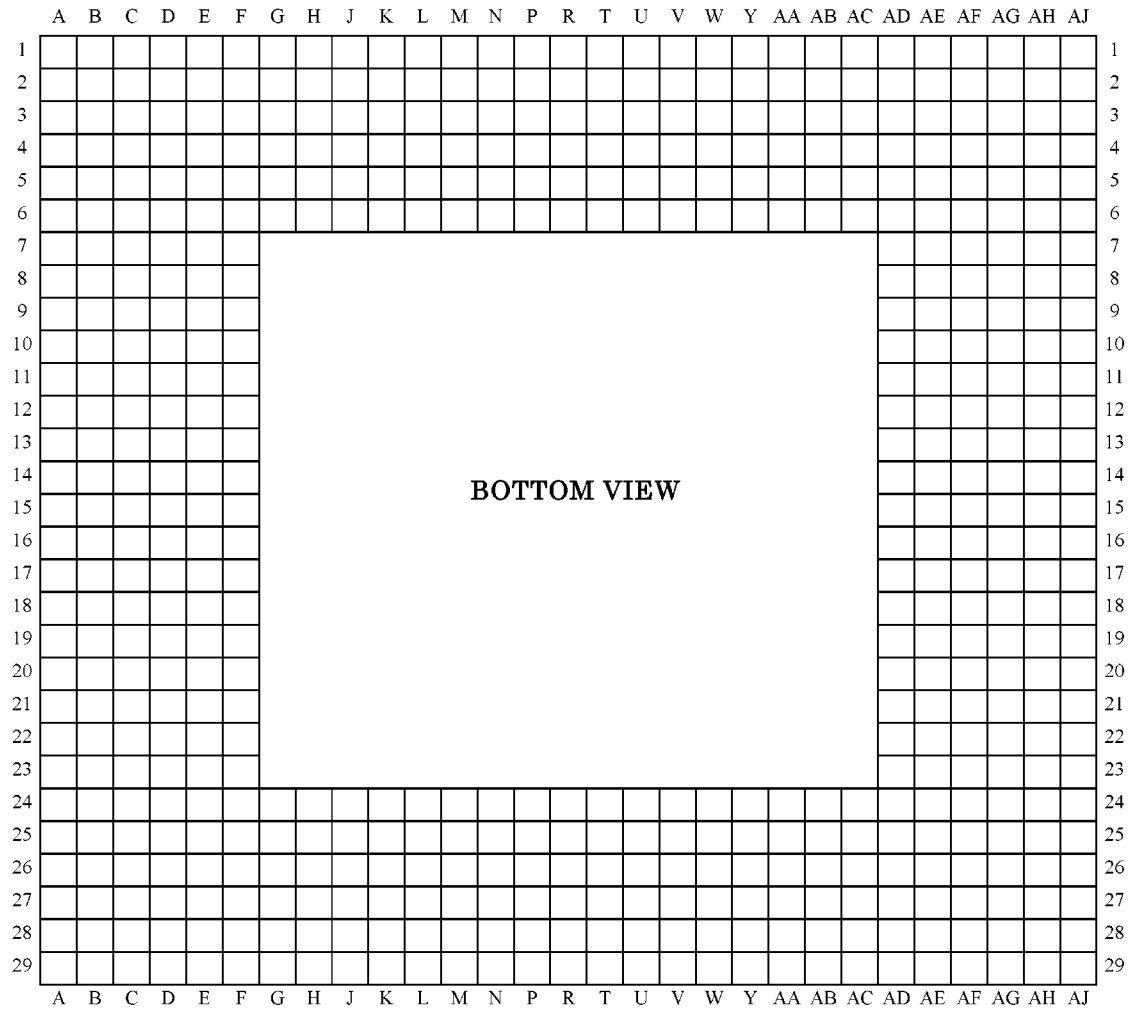


Figure 3.1 SYSTEM BLOCK DIAGRAM

4. Pin description

4.1. Pin assignment



* Active-low signal

NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME
A01	MROMA[17]	C01	IO5BHE*	E01	IO5ADR[09]	G01	IO5ADR[01]	M01	IO5DAT[00]
A02	MROMA[14]	C02	IO5WR*	E02	IO5ADR[10]	G02	IO5ADR[02]	M02	IO5DAT[01]
A03	MRCS[06]*	C03	MROMA[19]	E03	IO5CS[04]*	G03	IO5ADR[07]	M03	IO5DAT[02]
A04	MRCS[03]*	C04	MROMA[15]	E04	IO5RD*	G04	IO5CS[01]*	M04	IO5DAT[03]
A05	DBGCS*	C05	MRCS[07]*	E05	VDDS	G05	VDD	M05	VDD
A06	RMCS03*	C06	MRCS[02]*	E06	VDD	G06	GND	M06	GND
A07	RMDAT[06]	C07	DBGWAIT	E07	NC	G24	APLLVSS2	M24	GND
A08	CLKBUS	C08	RMMCS1*	E08	VDDS	G25	VDDS	M25	VDDS
A09	RMDAT[04]	C09	RMDAT[05]	E09	VDD	G26	LCDGD[16]	M26	VRCS[00]*
A10	RMDAT[00]	C10	RMDAT[03]	E10	VDDS	G27	VRDAT[28]	M27	VRCS[01]*
A11	RMDAT[13]	C11	RMDAT[15]	E11	NC	G28	VRDAT[27]	M28	VRDQM[00]
A12	RMDAT[09]	C12	RMDAT[11]	E12	VDD	G29	VRDAT[26]	M29	VRDQM[01]
A13	RMALE	C13	RMCS00*	E13	VDDS	H01	IO5DAT[13]	N01	IO5INT[00]
A14	RMADR[10]	C14	RMADR[12]	E14	VDD	H02	IO5ADR[00]	N02	IO5INT[01]
A15	RMADR[06]	C15	RMADR[08]	E15	VDDS	H03	IO5ADR[03]	N03	IO5INT[03]
A16	RMADR[05]	C16	RMADR[03]	E16	NC	H04	IO5ADR[08]	N04	IO5INT[02]
A17	RMADR[01]	C17	RMCAS[02]*	E17	VDD	H05	NC	N05	VDDS
A18	RMDAT[24]	C18	RMCAS[00]*	E18	VDDS	H06	GND	N06	GND
A19	RMDAT[26]	C19	RMDAT[29]	E19	VDD	H24	GND	N24	GND
A20	RMDAT[28]	C20	RMDAT[17]	E20	VDDS	H25	NC	N25	VDD
A21	RMDAT[16]	C21	RMDAT[21]	E21	VDD	H26	LCDGD[17]	N26	TEST[1]
A22	RMDAT[19]	C22	LCDGD[07]	E22	VDDS	H27	VRDAT[25]	N27	VRADR[10]
A23	RMDAT[23]	C23	LCDGD[04]	E23	NC	H28	VRDAT[24]	N28	VRDQM[02]
A24	CLKMEM	C24	LCDGD[01]	E24	VDD	H29	VRDAT[23]	N29	VRDQM[03]
A25	LCDGD[02]	C25	LCDDEN	E25	APLLVDD	J01	IO5DAT[10]	P01	TEST[0]
A26	LCDFP	C26	BKLOFF	E26	PWRCNT[02]	J02	IO5DAT[12]	P02	IO3INT[01]
A27	CLKVIDEO	C27	APLLLP	E27	LCDGD[12]	J03	IO5DAT[15]	P03	IO3INT[00]
A28	IO5CLRL*	C28	PWRCNT[00]	E28	LCDGD[13]	J04	IO5ADR[04]	P04	INTO
A29	APLLVSS1	C29	LCDGD[09]	E29	VRDAT[31]	J05	VDDS	P05	NC
B01	MROMA[21]	D01	IO5CS[02]*	F01	IO5ADR[05]	J06	GND	P06	GND
B02	MROMA[18]	D02	IO5CS[03]*	F02	IO5ADR[06]	J24	GND	P24	GND
B03	MROMA[13]	D03	MROMA[22]	F03	IO5CS[00]*	J25	VDD	P25	NC
B04	MRCS[05]*	D04	MROMA[20]	F04	IO5WAIT*	J26	VRDAT[22]	P26	VRADR[09]
B05	MRCS[00]*	D05	MROMA[16]	F05	NC	J27	VRDAT[21]	P27	VRADR[08]
B06	RMMWA*	D06	MROMOE*	F06	NC	J28	VRDAT[20]	P28	VRADR[07]
B07	RMDAT[07]	D07	MRCS[04]*	F07	GND	J29	VRDAT[19]	P29	VRADR[06]
B08	RCLR*	D08	MRCS[01]*	F08	NC	K01	IO5DAT[06]	R01	VDD
B09	PCLR*	D09	RMMCS0*	F09	GND	K02	IO5DAT[09]	R02	SMCIN*
B10	RMDAT[01]	D10	CLKRTC	F10	GND	K03	IO5DAT[11]	R03	SMCD*
B11	RMDAT[14]	D11	RMDAT[02]	F11	GND	K04	IO5DAT[14]	R04	SMDT[04]
B12	RMDAT[10]	D12	RMDAT[12]	F12	GND	K05	VDD	R05	UVCC3
B13	RMRD*	D13	RMDAT[08]	F13	GND	K06	GND	R06	GND
B14	RMADR[11]	D14	RMWT*	F14	NC	K24	GND	R24	GND
B15	RMADR[07]	D15	RMADR[09]	F15	GND	K25	VDDS	R25	VDDS
B16	RMADR[02]	D16	RMADR[04]	F16	GND	K26	VRDAT[18]	R26	VRADR[05]
B17	RMADR[00]	D17	RMCAS[03]*	F17	GND	K27	VRDAT[17]	R27	VRADR[04]
B18	RMCAS[01]*	D18	RMDAT[25]	F18	GND	K28	VRDAT[16]	R28	VRADR[03]
B19	RMDAT[27]	D19	RMDAT[30]	F19	NC	K29	VRCKE	R29	VRADR[02]
B20	RMDAT[31]	D20	RMDAT[20]	F20	GND	L01	IO5DAT[04]	T01	SMDT[05]
B21	RMDAT[18]	D21	LCDGD[06]	F21	GND	L02	IO5DAT[05]	T02	SMDT[03]
B22	RMDAT[22]	D22	LCDGD[03]	F22	NC	L03	IO5DAT[07]	T03	SMDT[06]
B23	LCDGD[08]	D23	LCDGD[00]	F23	GND	L04	IO5DAT[08]	T04	SMDT[02]
B24	LCDGD[05]	D24	LCDDSP	F24	NC	L05	VDDS	T05	VDD
B25	LCDCLK	D25	LCDOFF	F25	NC	L06	NC	T06	NC
B26	LCDLP	D26	APLLRO	F26	LCDGD[14]	L24	NC	T24	NC
B27	IO5CLRH	D27	PWRCNT[01]	F27	LCDGD[15]	L25	VDD	T25	VDD
B28	APLLAGS	D28	LCDGD[11]	F28	VRDAT[30]	L26	VRRAS*	T26	VRADR[00]
B29	IO5PWR	D29	LCDGD[10]	F29	VRDAT[29]	L27	VRCAS*	T27	VRDAT[00]
						L28	VRWE*	T28	VRDAT[01]
						L29	VRCLK	T29	VRADR[01]

* Active-low signal

NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME
U01	SMDT[07]	AB01	C2VCC5*	AD01	C2VS[01]*	AF01	C2DATL[07]	AH01	C2IOR*
U02	SMDT[01]	AB02	C2CD[02]*	AD02	C2DATH[03]	AF02	C2DATH[07]	AH02	C2ADR[17]
U03	SMVS	AB03	C2DATL[04]	AD03	C2DATH[05]	AF03	C2ADR[09]	AH03	C2ADR[20]
U04	SMDT[00]	AB04	C2DATL[06]	AD04	C2OEN*	AF04	C2ADR[18]	AH04	C2ADR[22]
U05	UVCC3	AB05	VDD	AD05	NC	AF05	C2WEN*	AH05	C2ADR[24]
U06	GND	AB06	NC	AD06	NC	AF06	C2ADR[21]	AH06	C2ADR[05]
U24	GND	AB24	NC	AD07	GND	AF07	C2ADR[23]	AH07	C2ADR[03]
U25	VDDS	AB25	VDDS	AD08	NC	AF08	C2ADR[25]	AH08	C2REG*
U26	VRDAT[05]	AB26	LCDLUM[1]	AD09	GND	AF09	C2ADR[04]	AH09	C2BVD[01]
U27	VRDAT[04]	AB27	DACG	AD10	GND	AF10	C2BVD[02]	AH10	C2DATL[01]
U28	VRDAT[03]	AB28	IREF	AD11	GND	AF11	C2DATH[01]	AH11	C2WP
U29	VRDAT[02]	AB29	LCDLEV[3]	AD12	NC	AF12	USBD2M	AH12	NC
V01	SMWP*	AC01	C2CD[01]*	AD13	GND	AF13	USBD1P	AH13	USBOC1
V02	SMRDY	AC02	C2VS[02]*	AD14	NC	AF14	CLKUSB	AH14	USBPWR2
V03	SMWE*	AC03	C2DATL[05]	AD15	GND	AF15	C1VPPG	AH15	C1VCC5*
V04	SMRE*	AC04	C2EN[01]*	AD16	GND	AF16	C1DATL[05]	AH16	C1DATL[04]
V05	VDD	AC05	UVCC2	AD17	GND	AF17	C1DATL[07]	AH17	C1DATL[06]
V06	GND	AC06	GND	AD18	GND	AF18	C1ADR[10]	AH18	C1EN[01]*
V24	GND	AC24	GND	AD19	NC	AF19	C1IOW*	AH19	C1OEN*
V25	VDD	AC25	VDD	AD20	GND	AF20	C1ADR[14]	AH20	C1ADR[09]
V26	VRDAT[09]	AC26	JTCK	AD21	GND	AF21	C1ADR[16]	AH21	C1ADR[13]
V27	VRDAT[08]	AC27	LCDLUM[0]	AD22	NC	AF22	C1ADR[07]	AH22	C1WEN*
V28	VRDAT[07]	AC28	EXTVREF	AD23	GND	AF23	C1ADR[05]	AH23	C1BSY*
V29	VRDAT[06]	AC29	VREF	AD24	NC	AF24	C1ADR[03]	AH24	C1ADR[15]
W01	SMALE			AD25	NC	AF25	C1BVD[02]	AH25	C1ADR[24]
W02	SMCE*			AD26	C1CD[02]*	AF26	C1DATH[00]	AH26	C1RST
W03	SMCLE			AD27	JTMS	AF27	C1DATH[01]	AH27	C1ADR[02]
W04	SMPWR2*			AD28	JTDI	AF28	C1VS[01]*	AH28	C1BVD[01]
W05	NC			AD29	JTDO	AF29	C1VS[02]*	AH29	C1DATL[01]
W06	GND			AE01	C2DATH[06]	AG01	C2ADR[10]	AJ01	C2ADR[08]
W24	GND			AE02	C2DATH[04]	AG02	C2ADR[11]	AJ02	C2ADR[14]
W25	NC			AE03	C2EN[02]*	AG03	C2ADR[13]	AJ03	C2BSY*
W26	VRDAT[14]			AE04	C2IOW*	AG04	C2ADR[19]	AJ04	C2ADR[15]
W27	VRDAT[13]			AE05	VDD	AG05	C2ADR[16]	AJ05	C2ADR[07]
W28	VRDAT[12]			AE06	UVCC2	AG06	C2ADR[12]	AJ06	C2RST
W29	VRDAT[10]			AE07	NC	AG07	C2ADR[06]	AJ07	C2ADR[02]
Y01	SMWPIN*			AE08	VDD	AG08	C2WAIT*	AJ08	C2ADR[00]
Y02	SMSTDN*			AE09	UVCC2	AG09	C2ADR[01]	AJ09	C2DATH[00]
Y03	SMPWR1*			AE10	VDD	AG10	C2DATL[00]	AJ10	C2DATL[02]
Y04	CDAUD			AE11	NC	AG11	C2DATH[02]	AJ11	UVCC2
Y05	VDDS			AE12	VDD	AG12	USBD2P	AJ12	NC
Y06	GND			AE13	NC	AG13	USBD1M	AJ13	USBOC2
Y24	APVS[02]			AE14	VDDS	AG14	USBPWR1	AJ14	CDSHDN*
Y25	APVD[02]			AE15	VDD	AG15	C1VPVC	AJ15	C1VCC3*
Y26	LCDLEV[4]			AE16	NC	AG16	C1DATH[03]	AJ16	C1DATL[03]
Y27	LCDLEV[1]			AE17	UVCC1	AG17	C1DATH[05]	AJ17	C1DATH[04]
Y28	VRDAT[15]			AE18	VDD	AG18	C1DATH[07]	AJ18	C1DATH[06]
Y29	VRDAT[11]			AE19	VDD	AG19	C1ADR[11]	AJ19	C1EN[02]*
AA01	C2VCC3*			AE20	UVCC1	AG20	C1ADR[08]	AJ20	C1IOR*
AA02	C2VPVC			AE21	VDD	AG21	C1ADR[19]	AJ21	C1ADR[17]
AA03	C2VPPG			AE22	UVCC1	AG22	C1ADR[22]	AJ22	C1ADR[18]
AA04	C2DATL[03]			AE23	NC	AG23	C1ADR[23]	AJ23	C1ADR[20]
AA05	UVCC2			AE24	VDD	AG24	C1ADR[25]	AJ24	C1ADR[21]
AA06	GND			AE25	UVCC1	AG25	C1WAIT*	AJ25	C1ADR[12]
AA24	APVS[01]			AE26	C1DATL[02]	AG26	C1ADR[01]	AJ26	C1ADR[06]
AA25	APVD[01]			AE27	C1CD[01]*	AG27	C1DATL[00]	AJ27	C1ADR[04]
AA26	DACB			AE28	VSYNC	AG28	C1DATH[02]	AJ28	C1REG*
AA27	DACR			AE29	HSYNC	AG29	C1WP	AJ29	C1ADR[00]
AA28	LCDLEV[2]								

AA29	LCDLEV[0]								

■ TMPR3922 System Bus Interface

NAME	I/O	LEVEL	DESCRIPTION
RMDAT<31:00>	I/O	3.3V	System Data bus. These pins are connected to **D[31:0]** of TMPR3922.
RMADR<12:00>	I	3.3V	Multiplexed Address bus. These pins are connected to **A[12:0]** of TMPR3922.
RMALE	I	3.3V	Address latch enable for upper address bus. This pin is connected to **ALE** of TMPR3922. Plum2 latches upper address internally and generates **MROMA<22:13>** for ROM interface.
RMRD*	I	3.3V	Read signal. This pin is connected to **RD*** of TMPR3922.
RMWT*	I	3.3V	Write signal. This pin is connected to **WE*** of TMPR3922.
RMCS03*	I	3.3V	Chip select 3. This pin is connected to **CS3*** of TMPR3922.
RMCS00*	I	3.3V	Chip select 0. This pin is connected to **CS0*** of TMPR3922.
RMCAS<03:00>*	I	3.3V	CAS and Write enable signal. These pins are connected to **CAS3-0*** of TMPR3922.
RMMCS1*	I	3.3V	32 bit bus Chip select 1. This pin is connected to **MCS1*** of TMPR3922.
RMMCS0*	I	3.3V	32 bit bus Chip select 0. This pin is connected to **MCS0*** of TMPR3922.
RMMWA*	O	3.3V	32 bit bus wait 1. This pin is connected to **MCS0WAIT* and MCS1WAIT*** of TMPR3922

* Active-low signal

■ ROM Interface

NAME	I/O	LEVEL	DESCRIPTION
MROMA<22:13>	O	3.3V	Mask ROM upper addresses.
MRCS<07:00>*	O	3.3V	Mask ROM chip select signals.
MROMOE*	O	3.3V	Mask ROM output enable.

* Active-low signal

■ Video RAM Interface

NAME	I/O	LEVEL	DESCRIPTION
VRDAT<31:00>	I/O	3.3V	VRAM data.
VRADR<10:00>	O	3.3V	VRAM address
VRRAS*	O	3.3V	VRAM Row Address Strove
VRCAS*	O	3.3V	VRAM Column Address Strobe
VRWE*	O	3.3V	VRAM Write enable
VRCLK	O	3.3V	VRAM Clock
VRCS<01:00>*	O	3.3V	VRAM Chip Select
VRDQM<03:00>	O	3.3V	VRAM Output Enable/Data Mask
VRCKE	O	3.3V	VRAM Clock Enable

* Active-low signal

■ LCD Interface

NAME	I/O	LEVEL	DESCRIPTION
LCDGD<17:00>	O	3.3V	Graphics/video output
LCDCLK	O	3.3V	LCD clock
LCDDEN	O	3.3V	LCD display enable
LCDLP	O	3.3V	Line pulse
LCDFP	O	3.3V	Field pulse
LCDDSP	O	3.3V	LCD display enable timing
LCDOFF	O	3.3V	LCD off
BKLOFF	O	5V	Back Light off
LCDLEV<4:0>	O	OD	LCD contrast bit 4 - 0
LCDLUM<1:0>	O	5V	LCD luminance bit 1 - 0

OD: Open Drain

■ CRT Interface

NAME	I/O	LEVEL	DESCRIPTION
HSYNC	O	5V	H-Sync
VSYNC	O	5V	V-Sync
DACR	O	-	DAC Analog output R
DACG	O	-	DAC Analog output G
DACB	O	-	DAC Analog output B
IREF	O	-	Current Reference control
VREF	O	-	Voltage Reference
EXTVREF	I	-	External VREF input
APVD<02:01>	I	-	Analog VDD
APVS<02:01>	I	-	Analog VSS

■ PCMCIA1

NAME	I/O	LEVEL	DESCRIPTION
C1DATL<07:00>	I/O	3.3/5V	PCMCIA Lower data
C1DATH<07:00>	I/O	3.3/5V	PCMCIA Upper data
C1ADR<25:00>	O	3.3/5V	PCMCIA address
C1RST	O	3.3/5V	PCMCIA reset
C1EN<02:01>*	O	3.3/5V	PCMCIA enable
C1IOR*	O	3.3/5V	PCMCIA I/O read
C1IOW*	O	3.3/5V	PCMCIA I/O write
C1OEN*	O	3.3/5V	PCMCIA Output enable
C1WEN*	O	3.3/5V	PCMCIA Write enable
C1REG*	O	3.3/5V	PCMCIA Attribute select
C1BSY*	I	3.3/5V	PCMCIA Busy
C1BVD<02:01>	I	3.3/5V	PCMCIA Battery voltage detect
C1VS<02:01>*	I	3.3V	PCMCIA Voltage sense
C1CD<02:01>*	I	3.3V	PCMCIA Card detect
C1WP	I	3.3/5V	PCMCIA Write protect
C1WAIT*	I	3.3/5V	PCMCIA Wait
C1VPPG	O	3.3V	Voltage select
C1VPVC	O	3.3V	Voltage select
C1VCC5*	O	3.3V	Voltage select
C1VCC3*	O	3.3V	Voltage select

* Active-low signal

■ PCMCIA 2

NAME	I/O	LEVEL	DESCRIPTION
C2DATL<07:00>	I/O	3.3/5V	PCMCIA Lower data
C2DATH<07:00>	I/O	3.3/5V	PCMCIA Upper data
C2ADR<25:00>	O	3.3/5V	PCMCIA address
C2RST	O	3.3/5V	PCMCIA reset
C2EN<02:01>*	O	3.3/5V	PCMCIA enable
C2IOR*	O	3.3/5V	PCMCIA I/O read
C2IOW*	O	3.3/5V	PCMCIA I/O write
C2OEN*	O	3.3/5V	PCMCIA Output enable
C2WEN*	O	3.3/5V	PCMCIA Write enable
C2REG*	O	3.3/5V	PCMCIA Attribute select
C2BSY*	I	3.3/5V	PCMCIA Busy
C2BVD<02:01>	I	3.3/5V	PCMCIA Battery voltage detect
C2VS<02:01>*	I	3.3V	PCMCIA Voltage sense
C2CD<02:01>*	I	3.3V	PCMCIA Card detect
C2WP	I	3.3/5V	PCMCIA Write protect
C2WAIT*	I	3.3/5V	PCMCIA Wait
C2VPPG	O	3.3V	Voltage select
C2VPVC	O	3.3V	Voltage select
C2VCC5*	O	3.3V	Voltage select
C2VCC3*	O	3.3V	Voltage select

* Active-low signal

■ PCMCIA1/2 Common

NAME	I/O	LEVEL	DESCRIPTION
CDSHDN*	O	3.3V	Shut down
CDAUD	O	3.3V	Audio

* Active-low signal

■ SmartMedia Interface

NAME	I/O	LEVEL	DESCRIPTION
SMDT<07:00>	I/O	3.3/5V	Smartmedia data
SMCE*	O	3.3/5V	Smartmedia chip enable
SMWE*	O	3.3/5V	Smartmedia write enable
SMRE*	O	3.3/5V	Smartmedia read enable
SMCLE	O	3.3/5V	Smartmedia command latch enable
SMALE	O	3.3/5V	Smartmedia address latch enable
SMWP*	O	3.3/5V	Smartmedia write protect
SMWPIN*	I	3.3/5V	Smartmedia write protect from card
SMRDY	I	3.3/5V	Smartmedia ready
SMCD*	I	3.3/5V	Smartmedia card detect
SMCIN*	I	3.3/5V	Smartmedia card insert
SMVS	I	3.3/5V	Smartmedia voltage sense
SMPWR1*	O	3.3V	Smartmedia power 1
SMPWR2*	O	3.3V	Smartmedia power 2
SMSTDN*	O	3.3V	Smartmedia shutdown

* Active-low signal

■ USB Interface

NAME	I/O	LEVEL	DESCRIPTION
USBD1P	I/O	-	USB Port 1 data(+)
USBD1M	I/O	-	USB Port 1 data(-)
USBOC1*	I	5V	Port 1 Over Current detection input
USBD2P	I/O	-	USB Port 2 data(+)
USBD2M	I/O	-	USB Port 2 data(-)
USBOC2*	I	5V	Port 2 Over Current detection input
USBPWR1*	O	3.3V	USB Port1 Power control
USBPWR2*	O	3.3V	USB Port2 Power control

* Active-low signal

■ 5V 16/8-bit I/O Bus

NAME	I/O	LEVEL	DESCRIPTION
IO5DAT<15:00>	I/O	5V	16 bit Data bus for I/O devices.
IO5ADR<10:00>	O	5V	Address bus for I/O devices.
IO5CS<4:0>*	O	5V	I/O Chip select
IO5WR*	O	5V	I/O Write enable
IO5RD*	O	5V	I/O Read enable
IO5BHE*	O	5V	I/O Byte Enable
IO5WAIT*	I	5V	I/O Wait

* Active-low signal

■ Interrupt

NAME	I/O	LEVEL	DESCRIPTION
INTO	O	3.3V	Interrupt output to TMPR3922
IO5INT<03:00>	I	5V	Interrupt input for 16/8 bit I/O devices (5V Input).
IO3INT<01:00>	I	3.3V	Auxiliary Interrupt (3V Input).

■ Power Management

NAME	I/O	LEVEL	DESCRIPTION
IO5PWR	O	3.3V	Power Supply control of 16/8 bit IO Bus
PWRCNT<02:00>	O	3.3V	Power Control signals
IO5CLRH	O	5V	Clear signals for 16/8 bit I/O devices(Active High)
IO5CLRL*	O	5V	Clear signals for 16/8 bit I/O devices(Active Low)

* Active-low signal

■ Clear and Clock

NAME	I/O	LEVEL	DESCRIPTION
PCLR*	I	3.3V	Power on clear. This signal should be active at least Xms after cold start.
RCLR*	I	3.3V	Resume clear. This signal should be active during suspend mode.
CLKRTC	I	3.3V	This clock input pin should be connected to **BC32K** of TMPR3922. This clock is used to detect interrupt during suspend mode.
CLKBUS	I	3.3V	This clock input pin should be connected to **DCLKOUT** of TMPR3922. This clock generates system bus interface timing in PLUM2.
CLKMEM	I	3.3V	Clock for VRAM control. 66MHz – 75MHz
CLKUSB	I	3.3V	USB 48MHz clock input. This clock input pin should be connected to C48MOUT of TMPR3922.
CLKVIDEO	I	3.3V	PLL input for Video clock. This clock input pin should be connected to the external video clock generator (14.31818MHz).
APLLVDD	I		VDD for Analog PLL
APLLVSS <02:01>	I		VSS for Analog PLL
APLLRO	I		VCO Center Frequency Set Resistor Connection
APLLLP	I		Loop Filter Capacitor Connection
APLLAGS	I		Analog Sense pin for connection of external components

* Active-low signal

■ Test

NAME	I/O	LEVEL	DESCRIPTION
TEST<01:00>	I	3.3V	Test pin. These signals should be connected to VSS.

■ Debug board interface

NAME	I/O	LEVEL	DESCRIPTION
DBGCS*	O	3.3V	Debug board chip select
DBGWAIT	I	3.3V	Debug Wait control

* Active-low signal

■ JTAG

NAME	I/O	LEVEL	DESCRIPTION
JTDI	I	3.3V	Data is serially scanned in through this pin.
JTDO	O	3.3V	Data is serially scanned in through this pin.
JTMS	I	3.3V	JTAG command signal, indicating the incoming serial data is command data.
JTCK	I	3.3V	The processor outputs a serial clock on JTCK. On the rising edge of JTCK, both JTDI and JTMS are sampled.

■ Power Supply

NAME		LEVEL	DESCRIPTION
UVCC1		3.3/5V	Input PCMCIA slot1 VCC
UVCC2		3.3/5V	Input PCMCIA slot2 VCC
UVCC3		3.3/5V	Input SmartMedia VCC
VDDS		5V	Input Power Supply 5V
VDD		3.3V	Input Power Supply 3.3V
GND		GND	Signal Ground
NC		-	Not Connected

5. Operation explanation

5.1. Memory map

5.1.1. Features

MASKROM uses CS0 of TX3922.

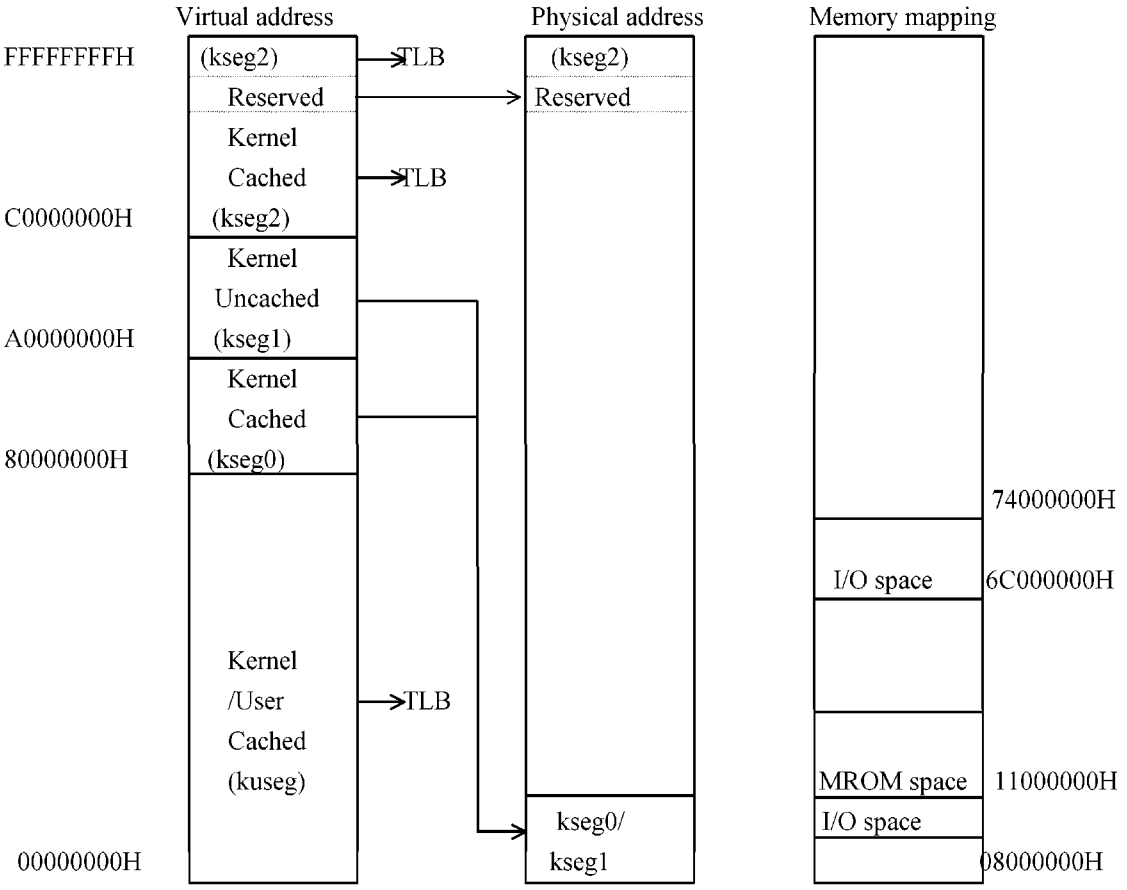
To access uses VRAM, PCMCIA, I/O bus, SmartMedia by the wait control

use MCS0, 1 piece of space of TX3922.

DRAM follow the memory mapping which TX3922 set.

DRAM directly in TX3922 Because it is possible to connect, there is not a control by Plum2, being necessary.

As for the space for I/O to use in other Plum2, use CS3 of TX3922.



5.1.2. Details in the MROM space

Physical address	Capacity	Bank Capacity			
		4MB	8MB	16MB	
1FC00000H-1FFFFFFFH	4MB	MROM7	MROM 7	MROM 7	Boot ROM
1F800000H-1FBFFFFFH	4MB	MROM6			
1F400000H-1F7FFFFFH	4MB	MROM5	MROM6		
1F000000H-1F3FFFFFH	4MB	MROM4			
1EC00000H-1EFFFFFFH	4MB	MROM3	MROM5	MROM6	
1E800000H-1EBFFFFFH	4MB	MROM2			
1E400000H-1E7FFFFFH	4MB	MROM1	MROM4		
1E000000H-1E3FFFFFH	4MB	MROM0			
1D800000H-1DFFFFFFH	8MB	Reserved	MROM3	MROM5	
1D000000H-1D7FFFFFH	8MB	Reserved	MROM2		
1C800000H-1CFFFFFFH	8MB	Reserved	MROM1	MROM4	
1C000000H-1C7FFFFFH	8MB	Reserved	MROM0		
11000000H-1DFFFFFFH	176MB	Reserved			

5.1.3. Details in the I/O space (MCS0, 1 The access with Wait)

Physical address	Capacity	Device
70000000H-73FFFFFFH	64MB	MCS1 PCMCIA
6E000000H-6FFFFFFFH	32MB	MCS0 PCMCIA
6D000000H-6DFFFFFFH	16MB	MCS0 PCMCIA
6C800000H-6CFFFFFFH	8MB	MCS0 PCMCIA
6C700000H-6C7FFFFFH	1MB	MCS0 PCMCIA (I/O)
6C600000H-6C6FFFFFH	1MB	MCS0 PCMCIA (I/O)
6C41A000H-6C5FFFFFH		Reserved
6C419000H-6C419FFFH	4KB	MCS0 Debugging support
6C418000H-6C418FFFH	4KB	MCS0 SmartMedia
6C416000H-6C417FFFH		Reserved
6C410000H-6C415FFFH	24KB	MCS0 I/O Bus
6C404000H-6C40FFFFH		Reserved
6C403000H-6C403FFFH	4KB	MCS0 USB
6C402000H-6C402FFFH	4KB	MCS0 BitBlt
6C401000H-6C401FFFH	4KB	MCS0 Color palette CRT
6C400000H-6C400FFFH	4KB	MCS0 color palette LCD
6C000000H-6C3FFFFFH	4MB	MCS0 VRAM

5.1.4. The details in the I/O space (It is not in CS3, Wait).

Physical address	Capacity	Function block
10809000H-10BFFFFFH		Reserved
10808000H-10808FFFH	4KB	Interrupt controller
10807000H-10807FFFH	4KB	Power controller
10806000H-10806FFFH	4KB	I/O bus controller
10805000H-10805FFFH	4KB	PCMCIA
10804000H-10804FFFH	4KB	Reserved
10803000H-10803FFFH	4KB	Reserved
10802000H-10802FFFH	4KB	Reserved
10801000H-10801FFFH	4KB	Display controller
10800000H-10800FFFH	4KB	Bus controller

5.2. Internal register

5.2.1. PLUM register (no wait)

LCD/CRT controller 10801000H-10801FFFH Refer to Register Specification of Plum Display Spec	
PCMCIA controller 10805000H-10805FFFH Refer to the register specification of PCMCIA Controller for Plum2	
I/O bus controller 10806000H-10806FFFH	
offset	register
000	IOXBSZ I/O bus width setting
004	IOXCCNT I/O bus wait control 1 (Number of wait from the access beginning)
008	IOXACNT I/O bus wait control 2 (Number of wait in access)
00C	IOXSCNT I/O bus wait control 3 (Number of wait during access)
010	IDEMODE IDE mode setting
Power controller 10807000H-10807FFFH	
offset	register
000	PWRCONT power control
004	CLKCONT clock control
008	MROMCNT mask ROM control
00C	INPENA Input signal enable
010	RESETC reset control
100	TESTMD Test mode set
interrupt controller 10808000H-10808FFFH	
offset	register
000	INTSTA interrupt status
004	INTIEN Interrupt enable
100	EXTINTS Outside input interrupt status 1
104	EXTINTM Outside input interrupt status 2 (After the mask)
110	EXTIEN outside input interrupt mask
200	PCCINTS PC card I/O interrupt status 1
204	PCCINTM PC card I/O interrupt status 2 (After the mask)
210	PCCIEN The PC card I/O interrupt mask
220	PCCLKSL The PC card I/O interrupt detection clock setting
310	USBIEN USB host controller interrupt mask
410	SMIEN SmartMedia interrupt enable
ID register 1080B000H	
offset	register
000	PLUM ID

5.2.2. PLUM register (wait control)

LCD / the CRT Controller 6C402000H-6C402FFFH Refer to Register Specification of Plum Display Spec	
USB host controller 6C403000H-6C403FFFH Refer to USB Host Controller for PLUM2 Specification	
SmartMedia controller 6C418000H-6C418FFFH	
offset	Register
000	SSDATA SSFDC data transfer
004	SSMODE SSFDC access mode setting
008	SSSTAT SSFDC status
00C	SSINTS SSFDC interrupt status 1
010	SSINTM SSFDC interrupt status 2 (Behind the mask)
014	SSIEN SSFDC interrupt enable
018	SSPOWER SSFDC power control
01C	ECCCONT SSFDC ECC control
020	ECCPAR1 SSFDC line parity data1 (0-255)
024	ECCPAR2 SSFDC column parity data 1(0-255)
028	ECCPAR3 SSFDC line parity data2 (256-511)
02C	ECCPAR4 SSFDC column parity data 1(256-511)
030	SSWAIT SSFDC wait control

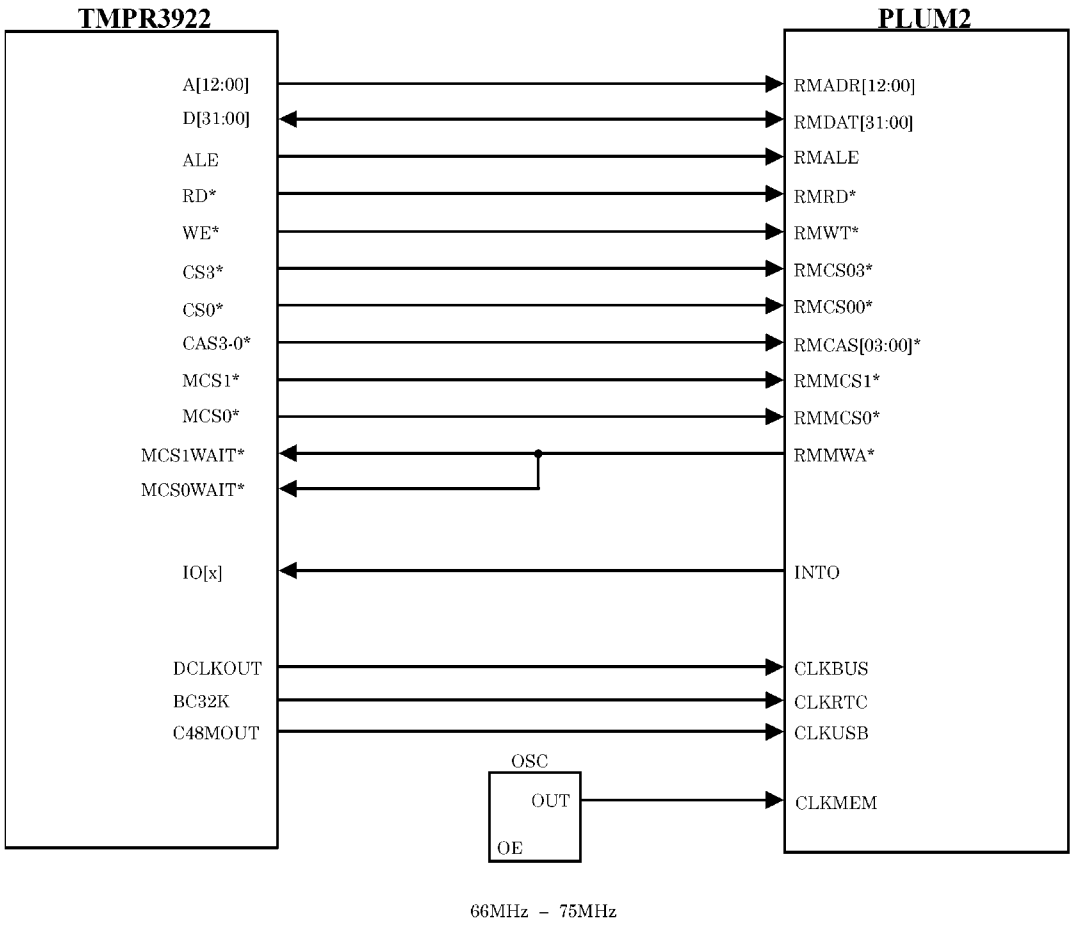
5.3. Bus interface

5.3.1. Features

The interface with the memory bus of TX3922 as the bus interface function and the latch of the address which is output from TX3922, Decoding of the address, Selection to each block , Output of the signal, Function of the Wait output to TX3922.

Figure in 5.3.1 Connection example with TX3922 is shown.

5.3.2. Connection between TMPR3922 and PLUM2



* Active-low signal

Note 1:TMPR3922 must be Little Endian Mode.

Figure 5.3.1

5.4. Memory controller

5.4.1. Features

It does an interface between TX3922 and ROM.

It outputs only higher rank address (MROMA22-13). Lower rank address (A12-2) use the address of TX3922.

MROM, OTPROM (the substitution of MROM), EPROM can correspond to the correspondence.

5.4.2. Correspondence memory specification

(1) MROM

The MROM capacity does the choice of 4 MB / 8 MB / 16MB by the MROMSL bit of the MROM control register.

MROMSL=0 1 4MB Bank × 8

MROMSL=0 0 8MB Bank × 8

MROMSL=1 X 16MB Bank × 8

The default condition It is a 8-MB unit. (MROMSL=0 0)

Memory specification

Capacity	Access time	Voltage	Word composition
1M word×32bit	100ns/50ns	3.3V	32bit× 1
2M word×32bit	100ns/50ns	3.3V	32bit× 1
4M word×32bit	100ns/50ns	3.3V	32bit× 1

Memory mapping (In case of the 4-MB unit)

Physical address	Capacity	Remarks
1FC00000H-1FFFFFFFH	4MB	Boot ROM
1F800000H-1FBFFFFFH	4MB	
1F400000H-1F7FFFFFH	4MB	
1F000000H-1F3FFFFFH	4MB	
1EC00000H-1EFFFFFFH	4MB	
1E800000H-1EBFFFFFH	4MB	
1E400000H-1E7FFFFFH	4MB	
1E000000H-1E3FFFFFH	4MB	

Memory mapping (In case of the 8-MB unit)

Physical address	Capacity	Remarks
1F800000H-1FFFFFFFH	8MB	Boot ROM
1F000000H-1F7FFFFFH	8MB	
1E800000H-1EFFFFFFH	8MB	
1E000000H-1E7FFFFFH	8MB	
1D800000H-1DFFFFFFH	8MB	
1D000000H-1D7FFFFFH	8MB	
1C800000H-1CFFFFFFH	8MB	
1C000000H-1C7FFFFFH	8MB	

Memory mapping (In case of the 16-MB unit)

Physical address	Capacity	Remarks
1F000000H-1FFFFFFFH	16MB	Boot ROM
1E000000H-1EFFFFFFH	16MB	
1D000000H-1DFFFFFFH	16MB	
1C000000H-1CFFFFFFH	16MB	

In case of this mode, MROMCS0 becomes MROMA23(The highest rank address).
It doesn't use MROMCS3-1.

(2) OTPROM

Memory specification

Capacity	Access time	Voltage	Word composition
1M word×16 bit	100ns/50ns	5V	16bit×2

Memory mapping

MROM and the same

(3) EPROM (For the debugging)

Memory specification

Capacity	model	Access time	Voltage	Word composition
512K word×8bit	TC57400AD-150		5V	8bit×4

Memory mapping

Physical address	capacity	Remarks
1FC00000H-1FDFFFFFH	2MB	

(4) ROM access

The burst reed of MROM, OTPROM go above 1 wait.
Also, set the setting of the number of wait with the memory configuration register of TX3922.

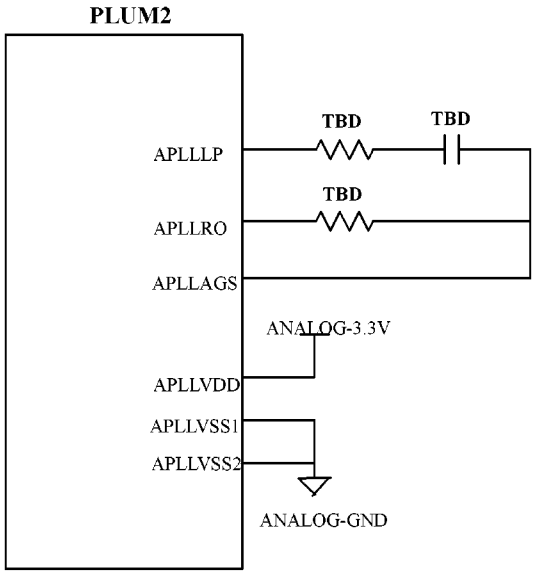
5.5. System clock control

The clock in the table below must be inputted as the clock for PLUM2. Also, it generates a video clock. Because it is It has PLL.

5.5.1. Clock pin

CLKRTC	This clock input pin connects with **BC32K** of TMPR3922. This clock is used to detect interrupt during suspend mode.
CLKBUS	This clock input pin connects with **DCLKOUT** of TMPR3922. This clock generates system bus interface timing in PLUM2.
CLKMEM	This clock input pin connects with **BCLK** of TMPR3922. It uses as the clock for VRAM. **BCLK** can set a period by the divider in TMPR3922. It makes the memory bandwidth small and it can be made low power. Also, this terminal can input the outside oscillator directly, too.
CLKUSB	This clock input pin connects with **C48MOUT** of TMPR3922. It uses as clock (48MHz) for USB.
CLKVIDEO	PLL input for Video clock. This clock input pin connects with the external video clock generator (14.31818MHz). The PLL input clock is the 12 MHz clock which made the clock of USB clock × 1/4 inside and can use, too. When using a clock, as for this terminal, a pull be downed.

5.5.2. Having-within PLL



Note that: APLLVDD and APLLVSS are ANALOG power supply signals. ANALOG power line/power Plane MUST separate form DIGITAL power line/power plane by using resistance and/or inductor.

5.6. Plum2 Display Controller Specification

5.6.1. Feature

(1)Support display

TFT	640 x 480, 800 x 600		RGB 6:6:6
DSTN	640 x 480, 800 x 600	70Hz,120Hz	RGB 1:1:1
STN	640 x 240, 640 x 480, 800 x 600	70Hz	RGB 1:1:1
CRT	640 x 480, 800 x 600	60Hz,72Hz,75Hz	

(2)Simultaneous display
CRT and Flat panel
Same image or different image

(3)DSTN panel color control
256K color support using frame dithering

(4)Memory map
1M,2M,4M Byte SGRAM
8-bit per pixel (SVGA compatible index color)
16-bit per pixel (SVGA compatible RGB565)
Linear addressing

(5)80MHz DAC for CRT output
256 entry 18-bit Palette (LCD and CRT)
6-bit DAC x 3
Video clock PLL (25MHz - 50MHz)

(6)BitBlt Accelerator
Color fill
Source copy
Transparent
Color expansion for text
(1bpp Mask map) Future support
Command FIFO 512 commands

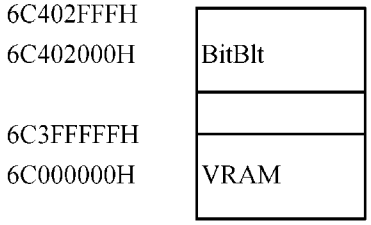
5.6.2. The address mapping

The inner register

The base address of LCD / the CRT Controller		10801000H
The base address of the color palette	LCD	6C400000H
	CRT	6C401000H

The access by VRAM, BitBlt

It accesses from the space of MCS0.



When accessing VRAM, BitBlt, it does respectively from the above space.

5.6.3. VRAM Memory Size

Area	Type	640x480		800x600	
		8bpp	16bpp	8bpp	16bpp
On Screen	1 Screen area	300KB	600KB	472KB	940KB
	2 Screen area	600KB	1200KB	944KB	1880KB
Off Screen work area	DSTN	84K		116K	
	FIFO	4K			
	USB	32K			
	Driver	20K			

5.6.4. On Screen VRAM format

(1)8bit per pixel Color index

Pixel displayed Left to right corresponding to VRAM byte address low to high

(2)RGB565 16-bit per pixel

Pixel displayed Left to right corresponding to VRAM word address low to high

Each pixel must be arranged in word boundary.

	upper byte		lower byte
Bit number	15-11	10-5	4-0
Bit width	5	6	5
Color	Red	Green	Blue

(3)8-bit per pixel monochrome

Pixel displayed Left to right corresponding to VRAM byte address low to high

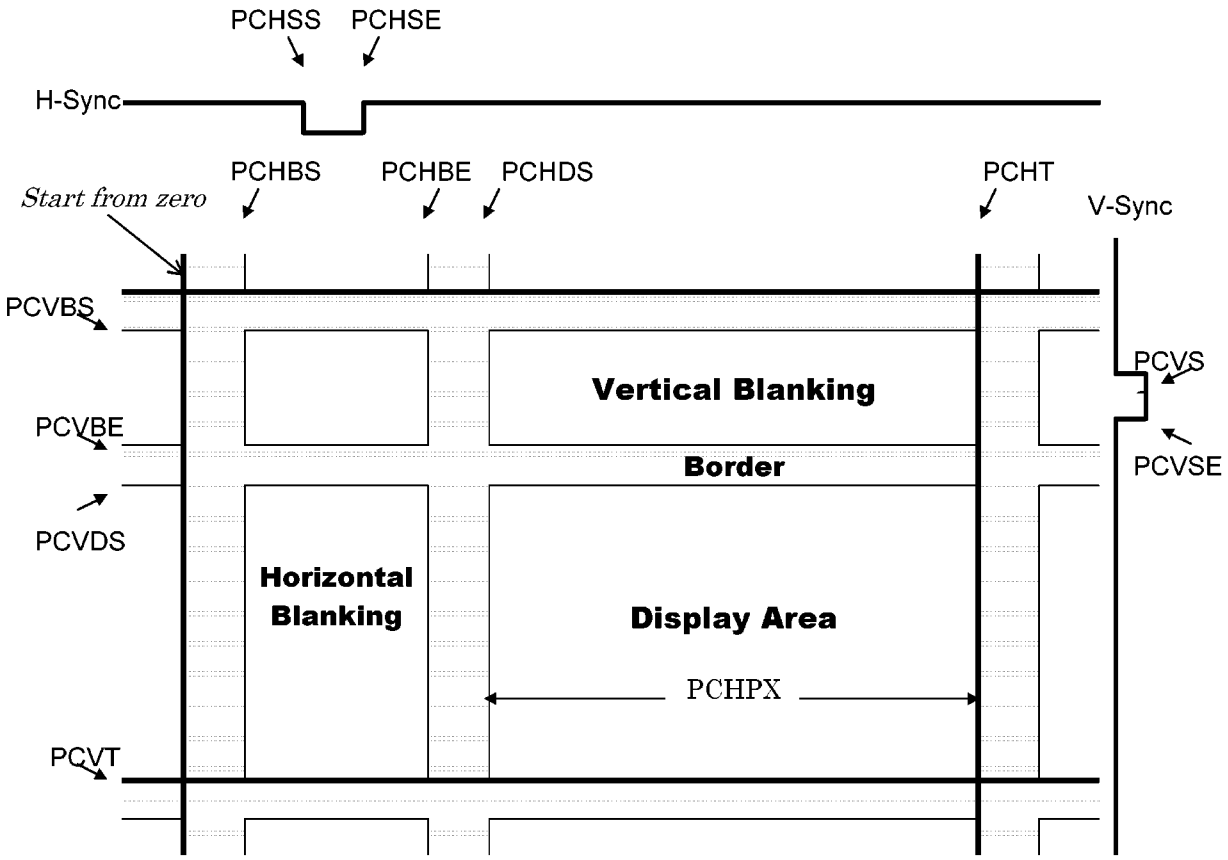
Color Palette format

256 indexed color palette is mapped on the memory space of 256K double word.
each double word data format is defined below.

Bit number	31-24	23-16	15-8	7-0
Bit width	8	8	8	8
Color	not used	Red	Green	Blue

5.6.5. Display timing control parameters

Display timing can be flexibly specified by Display timing control register.
Following figure shows relation between register and display timing.

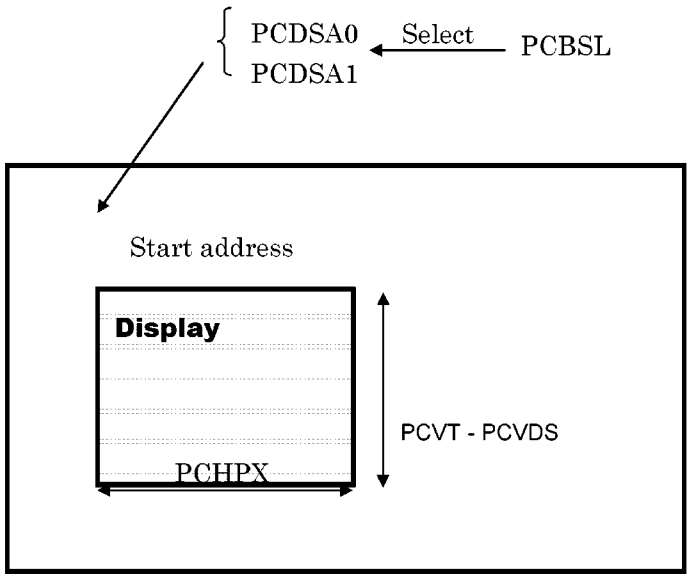


CRT Register	LCD Register	Comment
PCHT	PLHT	Horizontal total
PCHPX	PLHPX	Number of Horizontal Pixel
PCHDS	PLHDS	Horizontal display start position
PCHSS	PLHSS	Horizontal Sync start position
PCHSE	PLHSE	Horizontal Sync end position
PCHBS	PLHBS	Horizontal Blanking start position
PCHBE	PLHBE	Horizontal Blanking end position
PCVT	PLVT	Vertical total
PCVDS	PLVDS	Vertical display start position
PCVSS	PLVSS	Vertical Sync start position
PCVSE	PLVSE	Vertical Sync end position
PCVBS	PLVBS	Vertical Blanking start position
PCVBE	PLVBE	Vertical Blanking end position

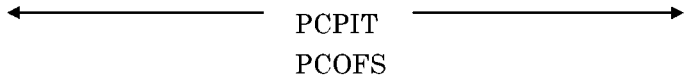
There are 2 sets of these registers for CRT and LCD independently.

5.6.6. Display address parameters

VRAM linear address is mapped to 2-dimensional area by turn back screen offset point.
Display address registers are used to specify Display rectangle area in the 2-D VRAM area.



2 Dimensional VRAM area



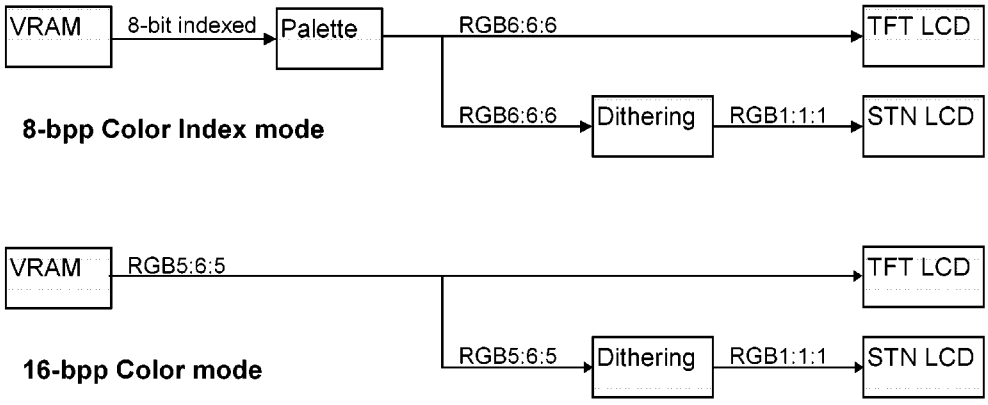
CRT Register	LCD Register	Comment
PCBSL	PLBSL	Buffer select 0:PxDSA0 1:PxDSA1
PCDSA0	PLDSA0	Display start address 0
PCDSA1	PLDSA1	Display start address 1
PCPIT	PLPIT	Horizontal Address Pitch
PCOFS	PLOFS	Horizontal Address Offset (= PxPIT for NI)

Note Using 2 registers PGPIT and PGOFS for interlaced display.
Set the same value for Non interlaced display.

There are 2 sets of these registers for CRT and LCD independently.

5.6.7. SVGA 8/16-bpp graphics support

Following figure shows the video format converting to display flat panel.



It is possible to display 256 colors at the same time in 8bpp mode. Index is converted to 18-bit RGB Color that is possible express 256K color. 16bpp mode is direct color mode. RBG5:6:5. enables to display 64K color simultaneously.

5.6.8. Interrupt

Supported interrupt

(1)V-Blanking Start (Determined by PLVT,PCVT)

(2)V-Blanking End (Determined by PLVDS,PCVDS)

(3)Display line

Generate interrupt if display scanning count is matched with the *Interrupt Line Number Register.*

(4)BitBlt command complete

Interrupt enable is specified in BitBlt command descriptor and if this flag is enabled generate interrupt when complete the command operation.

(5)BitBlt FIFO threshold

Generate interrupt if number of pending BitBlt commands in the FIFO is matched *Interrupted Command Entry Register.* This interrupt informs to processor to be able to set new BitBlt commands in the FIFO.

(6)VRAM Self refresh timing

Generate interrupt if VRAM controller start self refresh.

Interrupt control

All graphics interrupts are controlled by two registers to simplify interrupt routine.

(1)Interrupt enable register (Status enable and Line enable)

(2)Interrupt status register

Each bit of these two registers assigned same kind of interrupt source. Any bit of the status register is cleared by writing 1 to specified bit and interrupt line is also cleared if there are no other interrupt. Status bit of writing 0 is not changed.

5.6.9. BitBlt

Feature

(1)BitBlt Type

Source copy

Solid color fill

Transparent BitBlt

(2)Source pixel format

1bpp / Same as destination

Color expansion for 1bpp source (Font)

(3)Destination pixel format

8bpp 16bpp

(4)Command FIFO

Create command FIFO in off screen area of the VRAM

Fixed FIFO size 4K byte enable queuing maximum 511 commands

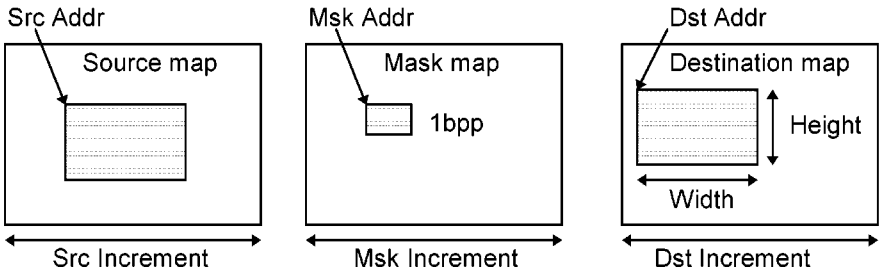
(5)Dual driver support

Independent control from LCD and CRT driver

(6)Mask map

1bpp map to inhibit destination write (Transparent)

Rectangle area parameters

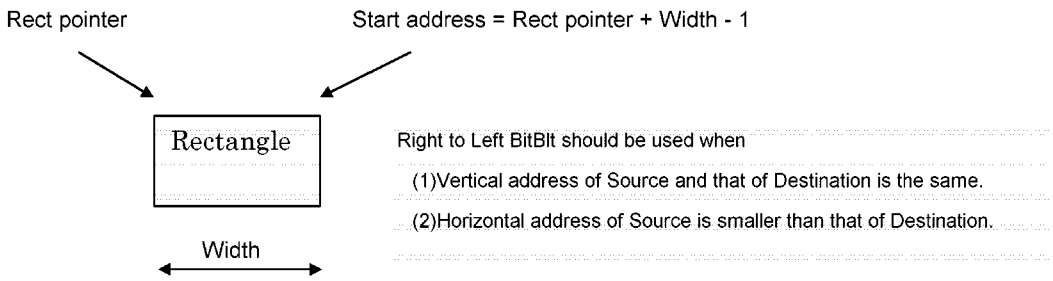


Rectangle size (pixel width and height) of source and mask are same as that of destination.

Right to Left BitBlt

Horizontal left scroll need *Right to Left BitBlt*. Driver should check this case to calculate start address from right side corner both source and destination to perform Right to Left BitBlt.

Note Color expansion BitBlt scanned from Right to Left is not supported.
Masked Right to Left BitBlt is not supported



Masked BitBlt

1bpp format

Mask bits from LSB to MSB corresponding to Destination Left to Right pixel.

Must start form bit 0 Byte aligned.

Bit value 0 means no source value is written to destination, 1 means write enable. BitBlt command format

BitBlt command format

Command descriptor is 8-byte per command fixed length format

BitBlt commands are stored in the FIFO reserved at off screen area of the VRAM.

Executable commands

Bit	63:40	39:36	35:32	31:20	19:8	7	6	5	4	3	2:0
Bit-width	24	4	4	12	12	1	1	1	1	1	3
BitBlt command	Addr	rsv	Type	Width	Height	rsv (*3op)	TE	Int	Dev	Com	

D63-40 : Dst address 24-bit Dest. start pixel address

D39:36 : rsv

D35-32 : Dst data type

D35 : Vertical Offset select	0:Register offset	1: Rectangle Width
D34 : Memory select	0:VRAM	1(*System memory)
D33 : Vertical Direction	0:Top to Bottom	1:Bottom to Top

D31-20 : Rectangle Width Specify number of pixels

D19-8 : Rectangle Height Specify number of pixels

D7 : rsv

D6 : (*3-ops Enable)

D5 : Transparent enable Color matched with Transparent color is not written

D4 : Interrupt enable Interrupt when BitBlt complete the command.

D3 : Device select 0:LCD 1:CRT

D2-0 : Command type 000:NOP 001:Color fill 010:Source Copy 011:Color Expansion

Expanded non executable commands

Bit	63:40	39:36	35:32	31:8	7:4	3	2:0
Bit-width	24	4	4	24	4	1	3
BitBlt command	Data2	Sel2	Type	Data1	Sel1	Dev	0

D63-36 : Data and Selection 2

D31-4 : Data and Selection 1

39:36	63:40	7:4	31:8
Sel2	Data2 field	Sel1	Data1 field
0	No data	0	No data
1	Color fill (24-bit RGB)	1	Trans Parent color (24-bit RGB)
2	Foreground Expand Color (RGB24)	2	Back ground Expand Color (RGB24)
3	Source address	3	Source vertical offset (Temporary)
4	Mask address	4	Mask vertical offset (Temporary)
5	rsv	5	Destination vertical offset (Temporary)
6	(*Pattern Number)	6	(*3 Raster Operation number)
7-15	rsv	7-15	Rsv

D35-32 : Data type valid when Src or Msk address of Data2 is selected

D35 : Vertical Offset select	0:Register offset	1: Rectangle Width
D34 : Memory select	0:VRAM	1(*System memory)
D33 : Vertical Direction	0:Top to Bottom	1:Bottom to Top

D3 : Device select 0:LCD 1:CRT

D2-0 : Expand command 000 NOP is used to expand command

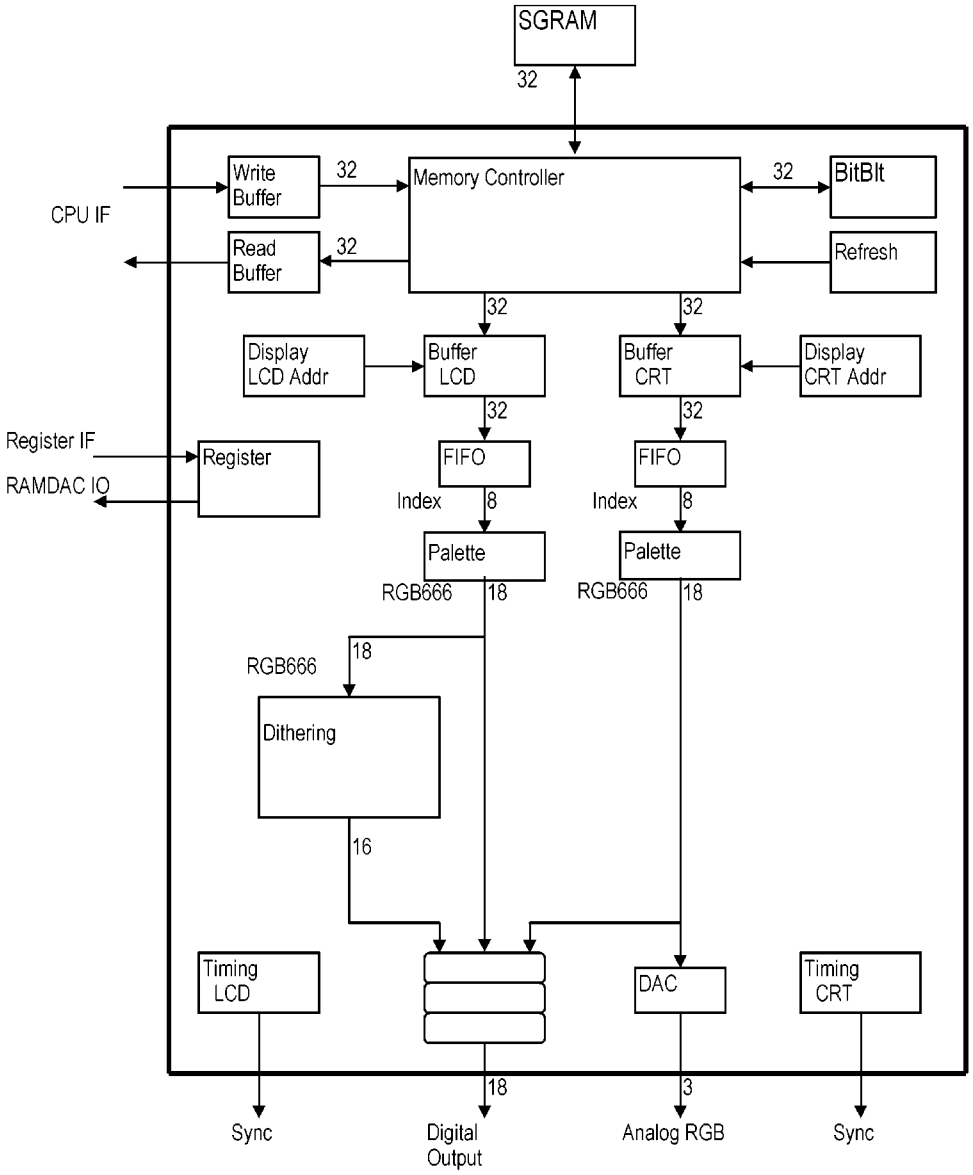
Note1 : Mask map is enabled by setting mask address and disabled after command execution.

Note2 : Vertical offset is specified unsigned value for both direction.

Note3 :Vertical offset can be selected one of 3 values Default ,Temporary and Rectangle width. Default vertical offset is assigned MMIO and initialized at setup. Temporary vertical offset is enabled by setting the register and disabled after command execution. Rectangle width is selected by setting D63 of the Type field. It can be selected individually from Source, Mask Destination.

Note4 : Items surrounded by (*) are future support.

5.6.10. Graphics Control Module Block Diagram


SGRAM
32
Write Buffer
32
Memory Controller
32
BitBlt
CPU IF
Read Buffer
32
Refresh
32
32
Display LCD Addr
Buffer LCD
Buffer CRT
Display CRT Addr
32
32
Register IF
Register
FIFO
FIFO
RAMDAC IO
Index
8
Index
8
Palette
Palette
RGB666
18
RGB666
18
18
RGB666
Dithering
16
Timing LCD
DAC
Timing CRT
18
3
Sync
Digital Output
Analog RGB
Sync

5.6.11. Register Specification

5.6.11.1 Graphics Memory mapped I/O

offset	31-24	23-16	15-08	07-00
003-000h	Interrupt Status Enable		PCI interrupt Enable	
007-004h			PCI interrupt status	
00B-008h			Buffer control	
00F-00Ch	VRAM control		VRAM control	
013-010h				Refresh control
017-014h				LCD clock source
01B-018h				CRT clock source
01F-01Ch	PLL Divider Parameter			PLL control
023-020h				
027-024h				
02B-028h				
02F-02Ch				
033-030h				
037-034h				
03B-038h				
03F-03Ch				
043-040h				LCD Control
047-044h				STN control
04B-048h				LCD Level
04F-04Ch				Luminance
053-050h		Off Screen Buffer Address		
057-054h				
05B-058h				
05F-05Ch				
063-060h				DAC control
067-064h		CRT Border color		
06B-068h				Palette snoop
06F-06Ch				
073-070h				
077-074h				
07B-078h				
07F-07Ch				Graphics Test
083-080h			LCD Horizontal Total	
087-084h			LCD Horizontal display start	
08B-088h	LCD H-Sync end		LCD H-Sync start	
08F-08Ch	LCD H-Blank end		LCD H-Blank end	
093-090h			LCD Horizontal number of Pixel	
097-094h			LCD Vertical total	
09B-098h			LCD Vertical display start	
09F-09Ch	LCD V-Sync end		LCD V-Sync start	
0A3-0A0h	LCD V-Blank end		LCD V-Blank end	
0A7-0A4h				
0AB-0A8h			Current display line number	
0AF-0ACh			Interrupt line number	
0B3-0B0h				LCD mode
0B7-0B4h				
0BB-0B8h				
0BF-0BCh		LCD test register		
0C3-0C0h				Buffer select
0C7-0C4h		LCD Display start address 0		
0CB-0C8h		LCD Display start address 1		
0CF-0CCh		LCD VRAM pitch 1		
0D3-0D0h		LCD VRAM pitch 2		
0D7-0D4h		LCD VRAM offset		
0DB-0D8h		LCD Lower Screen Address offset		
0DF-0DCh				Graphics mode
0E3-0E0h				
0E7-0E4h				
0EB-0E8h				
0EF-0ECh				
0F3-0F0h				
0F7-0F4h				
0FB-0F8h				
0FF-0FCh				

offset	31-24	23-16	15-08	07-00
103-100h			CRT Horizontal Total	
107-104h			CRT Horizontal display start	
10B-108h	CRT H-Sync end		CRT H-Sync start	
10F-10Ch	CRT H-Blank end		CRT H-Blank end	
113-110h			CRT Horizontal number of Pixel	
117-114h			CRT Vertical total	
11B-118h			CRT Vertical display start	
11F-11Ch	CRT V-Sync end		CRT V-Sync start	
123-120h	CRT V-Blank end		CRT V-Blank end	
127-124h				
12B-128h			Current display line number	
12F-12Ch			Interrupt line number	
133-130h				CRT mode
137-134h				
13B-138h				
13F-13Ch		CRTC test register		
143-140h				Buffer select
147-144h		CRT Display start address 0		
14B-148h		CRT Display start address 1		
14F-14Ch		CRT VRAM pitch 1		
153-150h		CRT VRAM pitch 2		
157-154h		CRT VRAM offset		
15B-158h				
15F-15Ch				Graphics mode
163-160h				
167-164h				
16B-168h				
16F-16Ch				
173-170h				
177-174h				
17B-178h				
17F-17Ch				
183-180h				
187-184h				
18B-188h				
18F-18Ch				
193-190h				
197-194h				
19B-198h				
19F-19Ch				
1A3-1A0h				
1A7-1A4h				
1AB-1A8h				
1AF-1ACh				
1B3-1B0h				
1B7-1B4h				
1BB-1B8h				
1BF-1BCh				
1C3-1C0h				
1C7-1C4h				
1CB-1C8h				
1CF-1CCh				
1D3-1D0h				
1D7-1D4h				
1DB-1D8h				
1DF-1DCh				
1E3-1E0h				
1E7-1E4h				
1EB-1E8h				
1EF-1ECh				
1F3-1F0h				
1F7-1F4h				
1FB-1F8h				
1FF-1FCh				

5.6.11.2 Common Control Register

Interrupt Status enable and IRQ line enable

I/O	Offset	Reg. Name	R/W	31:29	28	27:26	25:24	23:20	19:16	Initial
MMIO	000 00	POSEN	R W	0	SRF	CRTBLT	LCDBLT	CRTTIM	LCDTIM	00000000
			R/W	15:13	12	11:10	9:8	7:4	3:0	Initial
		POIEN	R W	0	SRF	CRTBLT	LCDBLT	CRTTIM	LCDTIM	00000000

D12-0 : Interrupts enable bits Writing 1 enables to generate INT to CPU.

D28-16 : Interrupt status enable bits Writing 1 enables to read status from POIST.

D0 : LCD V-Blanking Start

D1 : LCD V-Blanking End

D2 : LCD Display line See LCD Interrupted line register

D3 : rsv

D4 : CRT V-Blanking Start

D5 : CRT V-Blanking End

D6 : CRT Display line See CRT Interrupted line register

D7 : rsv

D8 : LCD BitBlt command After BitBlt command execution

D9 : LCD BitBlt FIFO count See Interrupt command count register

D10 : CRT BitBlt command After BitBlt command execution

D11 : CRT BitBlt FIFO count See Interrupt command count register

D12 : VRAM Self Refresh start

Interrupt Status

I/O	Offset	Reg. Name	R/W	31:13	12	11:10	9:8	7:4	3:0	Initial
MMIO	004 01	POIST	R W	0	SRF	CRTBLT	LCDBLT	CRTTIM	LCDTIM	00000000

D0 : LCD V-Blanking Start

D1 : LCD V-Blanking End

D2 : LCD Display line See LCD Interrupted line register

D3 : rsv

D4 : CRT V-Blanking Start

D5 : CRT V-Blanking End

D6 : CRT Display line See CRT Interrupted line register

D7 : rsv

D8 : LCD BitBlt command After BitBlt command execution

D9 : LCD BitBlt FIFO count See Interrupt command count register

D10 : CRT BitBlt command After BitBlt command execution

D11 : CRT BitBlt FIFO count See Interrupt command count register

D12 : VRAM Self Refresh start

Write 1 to any bit clears Status flag and Interrupt signal to the host.

Buffer Control

I/O	Offset	Reg. Name	R/W	31:16	15:8	7	6	5	4	3:2	1	0	Initial
MMIO	008 02	POBFC	R/W	0	WAIT	rsv	FLUSH	TMOFF	WBOFF	rsv	RBSL	RBOFF	00000000

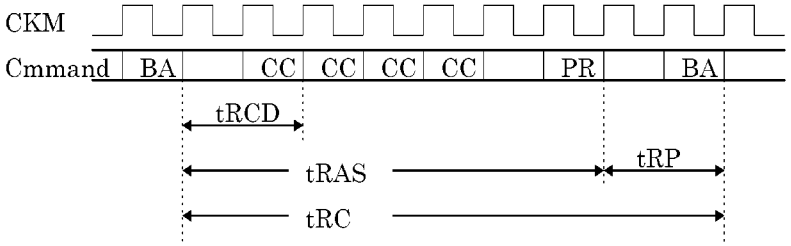
D0	: Read Buffer Off	0:Enable	1:Disable
D0	: Read Buffer Ready timing	0:Slow	1:Fast
D4	: Write Buffer Off	0:Enable	1:Disable
D5	: Time Out Off	0:Enable	1:off
D6	: Write Buffer Flash	0:Normal	1:Flash
D15-8	: Buffer wait count	Number of bus clock count (Test only)	

VRAM Control

I/O	Offset	Reg. Name	R/W	31	30	29:28	12	11	10:8	7	6:5	4	3	2:1	0	Initial
MMIO	00C 03	PORAM	R/W	RES	RUN	CKSL0	PD	BC	AS	CS	tRC	tRCD	tRP	tRAS	CL	00000000

D31	: Clear for memory circuit	0:Clear	1:Not clear			
D30	: SDRAM start running	0:Stop	1:Running			
D29-28	: Clock source select	00:CLKMEM	01:CLKUSB	10:PLL	11:CLKBUS/2	
D12	: Power Down mode	0: Disable	1: Enable			
D11	: Bank check enable	0:Enable	1:Disable			
D10	: Control Address select A10	0: Address 10	1: Precharge command			
D9	: Control Address select A9	0: Address 9	1: Precharge command			
D8	: Control Address select A8	0: Address 8	1: Precharge command			
D7	: Chip select type	0: Bank Address	1: 1 bank CS(0) = CS(1)			
	Bank address is determined by	D8=1: Bank is A10, D9=1: Bank is A11				
D6-5	: Active to Active	tRC	00:10CK	01:9CK	10:8CK	11:7CK
D4	: Active to Column Command	tRCD	0:3CK	1:2CK		
D3	: Precharge to Active	tRP	0:3CK	1:2CK		
D2-1	: Active to Precharge	tRAS	00:7CK	01:6CK	10:5CK	11:4CK
D0	: CAS Latency		0:3CK	1:2CK		

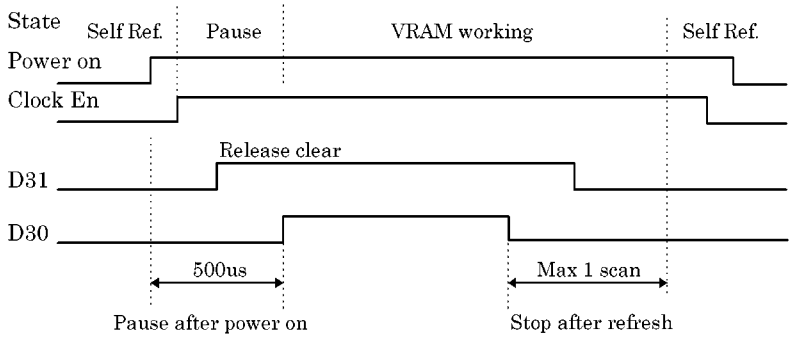
Set SDRAM control parameter. After that setting D30 of SDRAM start running bit initiate initialize command. To change control parameter, new parameter is written with D30 zero and then set D30 again.



BA:Bank active command
PR:Bank precharge command
CC:Column command

VRAM timing parapeter

D29:28	VRAM clock
00	CLKMEM Pin
01	CLKUSB
10	PLL
11	CLKBUS



VRAM Self refresh sequence

Sample setting of TOSHIBA SGRAM TC59G1632AFB

Memory Clock	50MHz	66MHz	74MHz	80MHz
AFB-80	02FF	02FF	02FF	02FF
AFB-10	02FF	02FF	02C4	----
AFB-12	02FF	02C4	----	----

VRAM Refresh Control

I/O	Offset	Reg. Name	R/W	31:3	2:0	Initial
MMIO	010 04	POREF	R/W	0	REFCNT	00000000

D2-0 : Number of refresh cycle per LCD Horizontal line Zero disable refresh.

LCD Clock Source select and control

I/O	Offset	Reg. Name	R/W	31:8	7	6	5:4	3	2	1	0	Initial
MMIO	014 05	POCKL	R/W	0	LCDR	SYNC	Sel	Div	Gate	EN	Run	00000000

D7 : LCDC running =1:LCD controller not cleared for VRAM refresh when D0=0

D6 : LCD/CRT synchronous =1:CRTC clear released by LCDC

D5:4 : Clock Select 00:PLL 01:CLKVIDEO 10:CLKUSB 11:CLKUSB/2

D5-4	LCD clock
00	PLL
01	CLKVIDEO Pin
10	CLKUSB Pin 48MHz
11	CLKUSB / 2 24MHz

D3 : LCD clock divide 0:Through 1:Divided by 2

D2 : LCD clock stop enable 0:Always clocking 1:Clock stop enable

D1 : LCD clock enable 0:Stop 1:Enable

D0 : LCD circuit clear 0:Clear 1:Running

LCD/CRT Synchronous clear release sequence

(1) Circuit cleared POCKL<06>=1,POCKL<00>=0, POCKC<00>=0

(2) Select same clock source for LCD/CRT

(3) CRTC clear release (still cleared) POCKC<00>=1

(4) LCDC clear release POCKL<00>=1

Both circuits are Synchronized by releasing clear at the same time.

CRT Clock Source select and control

I/O	Offset	Reg. Name	R/W	31:6	5:4	3	2	1	0	Initial
MMIO	018 06	POCKC	R/W	0	Sel	Div	Gate	EN	Run	00000000

D5:4 : Clock Select 00:PLL 01:CLKVIDEO 10:CLKUSB CLKUSB/2

D5-4	CRT clock
00	PLL
01	CLKVIDEO Pin
10	CLKUSB Pin 48MHz
11	CLKUSB / 2 24MHz

D3 : CRT clock divide 0:Through 1:Divided by 2

D2 : CRT clock stop enable 0:Always clocking 1:Clock stop enable

D1 : CRT clock enable 0:Stop 1:Enable

D0 : CRT circuit clear 0:Clear 1:Running

PLL Clock Source select and control

I/O	Offset	Reg. Name	R/W	31:24	23:20	19	18:16	2	1	0	Initial
MMIO	01C 07	POPLL	R/W	DIVN	DIVM	rsv	DIVO	EN	PWD Sel		00000000

D31:24 : PLL feedback frequency divider Set value - 1

D23:20 : PLL standard frequency divider Set value - 1

D19 : rsv

D18:16 : PLL output frequency divider

POPLL<18:16>	PLL output
000	Stop
001	VCO/2
010	VCO/4
100	VCO/6
110	VCO/8
111	VCO (for test)

VCO means PLL core output frequency

Base clock = 12 [MHz]

Resolution [Pixel]	Frame [Hz]	D31-24 Hex	D23-20 Hex	D18-16 Hex	VCO Freq. [MHz]	Standard [MHz]	Error [%]
640x480	60	3E	4	4	25.200	25.175	-0.099
	72,75	3E	3	4	31.500	31.500	0.000
	85	17	1	2	36.000	36.000	0.000
800x600	60	27	2	2	40.000	40.000	0.000
	72	31	2	2	50.000	50.000	0.000
	75	20	1	2	49.500	49.500	0.000

Base clock = 14.3182 [MHz]

Resolution [Pixel]	Frame [Hz]	D31-24 Hex	D23-20 Hex	D18-16 Hex	VCO Freq. [MHz]	Standard [MHz]	Error [%]
640x480	60	49	6	4	25.227	25.175	-0.208
	72,75	41	4	4	31.500	31.500	0.000
	85	13	1	2	35.795	36.000	0.568
800x600	60	42	5	2	39.972	40.000	0.071
	72	1B	1	2	50.114	50.000	-0.227
	75	52	5	2	49.517	49.500	-0.034

D2 : PLL input enable 0:Power down 1:PLL clock input enable

D1 : PLL Oscillation 0:Power down 1:Oscillation

D0 : Clock Select 0:12MHz (USB clock) 1:14.31818MHz(CLKVIDEO pin)

5.6.11.3 LCD Panel Control Register

LCD Control

I/O	Offset	Reg. Name	R/W	31:13	12	11	10	9	8	7:4	3	2	1	0	Initial
MMIO	040 10	PLCNT	R/W	0	rsv	DC	CK	OSC	DITH	Dither	CRT	MONO	TFT	2SC	00000000

D12 : Reserved must be **0**

D11 : DSTN control select **0**:normal 1: Use CRT for DSTN low

D10 : LCDCLK select **0**:Always clocking 1:Clock stop enable

D9 : Offscreen buffer enable **0**:Off 1:Use DSTN buffer on VRAM

D8 : Dither pattern enable 0:Off(Black and White) 1:Use dither pattern on VRAM

D7-4 : Dither control

D4	Dither level select	Possible color
0	64 level	256K
1	16 level	4096

D5	40h dither level select
0	Mapped
1	Half

D7-6	16bpp R0 bit select	16bpp B0 bit select
00	R5	B5
01	G5	G5
10	G0	G0
11	R0	B0

D3 : rsv

D2-0 : Digital output select

D3:CRT	D2:MONO	D1:TFT	D0:2SC	Digital output
0	**0**	**0**	**0**	Color STN
0	**0**	**0**	1	Color DSTN
0	**0**	1	x	TFT
0	1	x	x	Mono STN
1	x	x	x	CRT (for Test)

DSTN without offscreen memory is supported by using CRT circuit to display lower DSTN panel.

Setting bits D11=1 , D9 = 0 of this register and set CRT control register as follows

PCHT = 0

PCVT = 0

PCHPX = PLHPX

PCDSA0 = Lower DSTN display start address

PCDSA1 = Lower DSTN display start address

PCOFS = PLOFS

PCPIT1 = PLPIT1

PCPIT2 = PLPIT2

PCSNP = 1 (Palette snoop)

STN Control

I/O	Offset	Reg. Name	R/W	31:7	6	5:0	Initial
MMIO	044 11	PLSTN	R/W	0	SEL	MP	00000000

D6: : STN control mode 0:Inverted by Register 1:Inverted by Field Pulse

D5:0 : Period of M signal Number of horizontal count (for STN)

LCD Level control

I/O	Offset	Reg. Name	R/W	31:5	4:0	Initial
MMIO	048 12	PLLEV	R/W	0	LEV	00000000

D4-0 : LCD Level LCD panel level (5-bit value)

LCD Luminance control

I/O	Offset	Reg. Name	R/W	31:2	1:0	Initial
MMIO	04C 13	PLLUM	R/W	0	LUM	00000000

D1-0 : LCD Luminance LCD panel luminance (2-bit value)

DSTN Dither Pattern base address

I/O	Offset	Reg. Name	R/W	31:24	23:22	21:15	14:8	7:5	4:0	Initial
MMIO	050 14	PLDPA	R/W	ENDFRM	0	Base	Frame	Line	0	00000000

D31-24 : Frame period Set number of frames - 1 for dithering. maximum 128 frames.

D21-15 : Dither pattern base address

D14-8 : Next frame Set 01 for saving next frame pattern to offscreen buffer.

D7-5 : Low screen start lineSet line number lower screen start.

This buffer is enabled by setting PLCNT<08> =1.

DSTN VRAM Offscreen buffer address

I/O	Offset	Reg. Name	R/W	31:22	21:5	4:0	Initial
MMIO	054 15	PLOSA	R/W	0	OSA	0	00000000

D21-5 : DSTN off screen buffer address 4K byte boundary

This buffer is enabled by setting PLCNT<09>=1.

5.6.11.4 CRT Control Register

DAC control

I/O	Offset	Reg. Name	R/W	31:5	4	3	2	1	0	Initial
MMIO	060 18	PCDAC	W	0	VREFSL	DACPD	VREFPD	CMPPD	-	00000000
			R	0	VREFSL	DACPD	VREFPD	CMPPD	COMP	00000000

D4 : VREF select **0**:Internal 1:External

D3 : DAC Power down **0**:Power down 1:Enable DAC

D2 : VREF Power down **0**:Power down 1:Enable Voltage reference

D1 : Comp. Power down **0**:Power down 1:Enable Comparator

D0 : Comp. Status **0**:CRT disconnected 1:CRT connected

Sequence of detecting CRT connection

(1) Setting CRT display mode

(2) Set Horizontal display start PCHDS = **0000FFFF**h

(3) Set Horizontal blanking PCHBE,PCHBS = **0000FFFF**h

(4) Set Vertical blanking PCVBE,PCVBS= **0000FFFF**h

(5) Set Border color (Threshold value) PCBOC = **00004000**h

(6) DAC enable PCDAC = **000E**h

(7) Start Running CRTC POCKC = **00?3**h (? = clock source select)

(8) Read comparator status PCDAC

If PCDAC = 0Eh then CRT not connected

If PCDAC = 0Fh then CRT connected

CRT Border Color

I/O	Offset	Reg. Name	R/W	31:24	23:16	15:8	7:0	Initial
MMIO	064 19	PCBOC	R/W	0	BOCR	BOCG	BOCB	00000000

D23-16 : CRT Border Color Red 8-bit Red border color value

D15-8 : CRT Border Color Green 8-bit Green border color value

D7-0 : CRT Border Color Blue 8-bit Blue border color value

Palette snoop

I/O	Offset	Reg. Name	R/W	31:1	0	Initial
MMIO	068 1A	PCSNP	R/W	0	snoop	00000000

D0 : Palette snoop **0**:Separate 1:Both palette written by LCD palette port.

There are 2 palettes for LCD and CRT. Normally it work separately but setting this bit enables palette snooping. Data writing to LCD palette is also written to CRT palette. It save the time of setting palette twice if displaying one screen mode.

5.6.11.5 LCD Timing Register

Horizontal Total

I/O	Offset	Reg. Name	R/W	31:12	11:3	2:0	Initial
MMIO	080 20	PLHT	R/W	0	HT	0	00000000

D11-0 : Horizontal Total Number of Pixel - 1 (Lower 3 bits are zero)

Horizontal Display Start

I/O	Offset	Reg. Name	R/W	31:12	11:3	2:0	Initial
MMIO	084 21	PLHDS	R/W	0	HDS	0	00000000

D11-0 : H-display start Number of Pixel - 1 (Lower 3 bits are zero)

H-Sync Start / End

I/O	Offset	Reg. Name	R/W	31:28	27:19	18:16	15:12	11:3	2:0	Initial
MMIO	088 22	PLHSE,HSS	R/W	0	HSE	0	0	HSS	0	00000000

D11-0 : H-Sync width Number of Pixel - 1 (Lower 3 bits are zero)

D27-16 : H-Sync width Number of Pixel - 1 (Lower 3 bits are zero)

H-Blanking Start /End

I/O	Offset	Reg. Name	R/W	31:28	27:19	18:16	15:12	11:3	2:0	Initial
MMIO	08C 23	PLHBE,HBE	R/W	0	HBE	0	0	HBS	0	00000000

D11-0 : H-Blank width Number of Pixel - 1 (Lower 3 bits are zero)

D27-16 : H-Blank width Number of Pixel - 1 (Lower 3 bits are zero)

Horizontal Number of Pixel

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	090 24	PLHPX	R/W	0	HPX	00000000

D9-0 : H-Display width Number of Horizontal Pixels to display (Without H-Panning)

Changing display start address pixel by pixel, it enables Horizontal panning display.

In this case, set +4 value to this register.

Vertical Total

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	094 25	PLVT	R/W	0	VT	00000000

D9-0 : Vertical Total Number of lines - 1

Vertical Display Start

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	098 26	PLVDS	R/W	0	VDS	00000000

D9-0 : Vertical Display start Number of lines - 1

V-Sync Start / End

I/O	Offset	Reg. Name	R/W	31:26	25:16	15:10	9:0	Initial
MMIO	09C 27	PLVSE,VSS	R/W	0	VSE	0	VSS	00000000

D9-0 : V-Sync start position Number of lines - 1

D25-16 : V-Sync end position Number of lines - 1

V-Blanking Start / End

I/O	Offset	Reg. Name	R/W	31:26	25:16	15:10	9:0	Initial
MMIO	0A0 28	PLVBE,VBS	R/W	0	VBE	0	VBS	00000000

D9-0 : V-Blank start position Number of lines - 1

D25-16 : V-Blank end position Number of lines - 1

I/O	Offset	Reg. Name	R/W		Initial
MMIO	0A4 29	rsv	R/W		00000000

Current Line Number

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	0A8 2A	PLCLN	R	0	LINE	00000000

D9-0 : Current displaying line number.

Line number is defined start from zero

Read data is asynchronous. So it is necessary to read twice and compare if values are the same. If not the same try again.

Interrupt Line Number

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	0AC 2B	PLILN	R/W	0	LINE	00000000

D9-0 : Interrupt line number Specify progressive line number start from 0.

See Interrupt enable and Interrupt status register. If field mode bit 0 of the line number is ignored. If frame mode bit 0 of the line number is compared.

Mode

I/O	Offset	Reg. Name	R/W	31:2	1	0	Initial
MMIO	0B0 2C	PLMOD	R/W	0	VPOL	HPOL	00000000

D1 : V-Sync Polarity 0:Positive 1:Negative

D0 : H-Sync Polarity 0:Positive 1:Negative

LCD controller test

I/O	Offset	Reg. Name	R/W	31:16	15	14	13	12	11:0	Initial
MMIO	0BC 2F	PLTST	W	0	VSL	HSL	CMP	-	Data	00000000
I/O	Offset	Reg. Name	R/W	31:19	18:8			7:6	5:0	Initial
			R	0	TDCMP			0	TDCRC	00000000

for CRTC controller test

D15 : V-counter enable

D14 : H-counter enable

D13 : Comparator test read enable

D11-0 : Counter load data

5.6.11.6 LCD Graphics Register

Double Buffer Select

I/O	Offset	Reg. Name	R/W	31:1	0	Initial
MMIO	0C0 30	PLBSL	R/W	0	Sel	00000000

D0 : Display buffer select 0:Buffer0(PLDSA0) 1:Buffer1(PLDSA1)

Graphics Display Start Address

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	0C4 31	PLDSA0	R/W	0	Start0	00000000
MMIO	0C8 32	PLDSA1	R/W	0	Start1	00000000

D21-0 : VRAM display start address for Double buffer 0

D21-0 : VRAM display start address for Double buffer 1

This register is used for "Double Buffer Operation

VRAM Pitch 1

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	0CC 33	PLPIT1	R/W	0	Pitch	00000000

D21-0 : VRAM horizontal length 1 Byte length of the horizontal line

Next line address is calculated from sum of the current address and this register.

Pitch 1 is used to calculate line first address.

VRAM Pitch 2

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	0D0 34	PLPIT2	R/W	0	Pitch	00000000

D21-0 : VRAM horizontal length 2 Byte length of the horizontal line

Next line address is calculated from sum of the current address and this register.

Pitch 2 is used to calculate from 2nd address (except line first address).

Set the value Pitch 2 = LSB 5-bit zero of Pitch 1.

VRAM Offset

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	0D4 35	PLOFS	R/W	0	Offset	00000000

D21-0 : Next line offset Byte length of the horizontal line

Next line start address is calculated from sum of the current line start address and this register.

VRAM Lower Screen address offset

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	0D8 36	PLLSA	R/W	0	Offset	00000000

D21-0 : Lower screen offset Byte length of the horizontal line

Lower screen start address is calculated from sum of the upper screen start address and this register.

Graphics Mode

I/O	Offset	Reg. Name	R/W	31:5	5	4	3	2	1:0	Initial
MMIO	0DC 37	PLGMD	R/W	0	AT	rsv	CCON	PALON	GMODE	00000000

D5 : Address test mode 0:normal 1:test

D4 : rsv

D3 : Palette access enable 0:Palette off (through) 1:Palette enable

D2 : Palette input select 0:Processor 1:Display

D1:0 : Graphics mode 00:Disable(Stop VRAM read) 01:8bpp 10:16bpp 11:rsv

Changing Palette sequence

(1) Set Display off	D1,0=00
(2) Switch Palette mode Display to CPU	D3=0
(3) Change Palette of any index	
(4) Switch Palette mode CPU to Display	D3=1
(5) Enable display	D1,0 = 01 or 11

5.6.11.7 CRT Timing Register

Horizontal Total

I/O	Offset	Reg. Name	R/W	31:12	11:3	2:0	Initial
MMIO	100 40	PCHT	R/W	0	HT	0	00000000

D11-0 : Horizontal Total Number of Pixel - 1 (Lower 3 bits are zero)

Horizontal Display Start

I/O	Offset	Reg. Name	R/W	31:12	11:3	2:0	Initial
MMIO	104 41	PCHDS	R/W	0	HDS	0	00000000

D11-0 : H-display start Number of Pixel - 1 (Lower 3 bits are zero)

H-Sync Start / End

I/O	Offset	Reg. Name	R/W	31:28	27:19	18:16	15:12	11:3	2:0	Initial
MMIO	108 42	PCHSE,HSS	R/W	0	HSE	0	0	HSS	0	00000000

D11-0 : H-Sync width Number of Pixel -1 (Lower 3 bits are zero)

D27-16 : H-Sync width Number of Pixel - 1 (Lower 3 bits are zero)

H-Blanking Start /End

I/O	Offset	Reg. Name	R/W	31:28	27:19	18:16	15:12	11:3	2:0	Initial
MMIO	10C 43	PCHBE,HBE	R/W	0	HBE	0	0	HBS	0	00000000

D11-0 : H-Blank width Number of Pixel - 1 (Lower 3 bits are zero)

D27-16 : H-Blank width Number of Pixel - 1 (Lower 3 bits are zero)

Horizontal Number of Pixel

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	110 44	PCHPX	R/W	0	HPX	00000000

D9-0 : H-Display width Number of Horizontal Pixels to display (Without H-Panning)

Changing display start address pixel by pixel, it enables Horizontal panning display.

In this case, set +4 value to this register.

Vertical Total

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	114 45	PCVT	R/W	0	VT	00000000

D9-0 : Vertical Total Number of lines - 1

Vertical Display Start

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	118 46	PCVDS	R/W	0	VDS	00000000

D9-0 : Vertical Display start Number of lines - 1

V-Sync Start / End

I/O	Offset	Reg. Name	R/W	31:26	25:16	15:10	9:0	Initial
MMIO	11C 47	PCVSE,VSS	R/W	0	VSE	0	VSS	00000000

D9-0 : V-Sync start position Number of lines - 1

D25-16 : V-Sync end position Number of lines - 1

V-Blanking Start / End

I/O	Offset	Reg. Name	R/W	31:26	25:16	15:10	9:0	Initial
MMIO	120 48	PCVBE,VBS	R/W	0	VBE	0	VBS	00000000

D9-0 : V-Blank start position Number of lines - 1

D25-16 : V-Blank end position Number of lines – 1

I/O	Offset	Reg. Name	R/W	31:0	Initial
MMIO	124 49	rsv	R/W	0	00000000

Current Line Number

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	128 4A	PCCLN	R	0	LINE	00000000

D9-0 : Current displaying line number.

Line number is defined as progressive format

1st field : Even number start from zero

2nd field : Odd number start from one

Read data is asynchronous. So it is necessary to read twice and compare if values are the same. If not the same try again.

Interrupt Line Number

I/O	Offset	Reg. Name	R/W	31:10	9:0	Initial
MMIO	12C 4B	PCILN	R/W	0	LINE	00000000

D9-0 : Interrupt line number Specify progressive line number start from 0.

See Interrupt enable and Interrupt status register. If field mode bit 0 of the line number is ignored. If frame mode bit 0 of the line number is compared.

Mode

I/O	Offset	Reg. Name	R/W	31:2	1	0	Initial
MMIO	130 4C	PCMOD	R/W	0	VPOL	HPOL	00000000

D1 : V-Sync Polarity 0:Positive 1:Negative

D0 : H-Sync Polarity 0:Positive 1:Negative

CRT test

I/O	Offset	Reg. Name	R/W	31:16	15	14	13	12	11:0	Initial
MMIO	13C 4F	PCTST	W	0	VSL	HSL	CMP	-	Data	00000000
I/O	Offset	Reg. Name	R/W	31:19	18:8			7:6	5:0	Initial
			R	0	TDCMP			0	TDCRC	00000000

for CRTC controller test

D15 : V-counter enable

D14 : H-counter enable

D13 : Comparator test read enable

D11-0 : Counter load data

5.6.11.8 CRT Graphics Register

Double Buffer Select

I/O	Offset	Reg. Name	R/W	31:1	0	Initial
MMIO	140 50	PCBSL	R/W	0	Sel	00000000

D0 : Display buffer select 0:Buffer0(PCDSA0) 1:Buffer1(PCDSA1)

Graphics Display Start Address

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	144 51	PCDSA0	R/W	0	Start0	00000000
MMIO	148 52	PCDSA1	R/W	0	Start1	00000000

D21-0 : VRAM display start address for Double buffer 0

D21-0 : VRAM display start address for Double buffer 1

This register is used for "Double Buffer Operation

VRAM Pitch 1

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	14C 53	PCPIT1	R/W	0	Pitch	00000000

D21-0 : VRAM horizontal length 1 Byte length of the horizontal line

Next line address is calculated from sum of the current address and this register.

Pitch 1 is used to calculate line first address.

VRAM Pitch 2

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	150 54	PCPIT2	R/W	0	Pitch	00000000

D21-0 : VRAM horizontal length 2 Byte length of the horizontal line

Next line address is calculated from sum of the current address and this register.

Pitch 2 is used to calculate from 2nd address (except line first address).

Set the value Pitch 2 = LSB 5-bit zero of Pitch 1.

VRAM Offset

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	154 55	PCOFS	R/W	0	Offset	00000000

D21-0 : Next line offset Byte length of the horizontal line

Next display line start address is calculated from sum of the current line start address and this register.

Not used

I/O	Offset	Reg. Name	R/W	31:22	21:0	Initial
MMIO	158 56	PCLSA	R/W	0	rsv	00000000

Graphics Mode

I/O	Offset	Reg. Name	R/W	31:5	5	4	3	2	1:0	Initial
MMIO	15C 57	PCGMD	R/W	0	AT	rsv	CCON	PALON	GMODE	00000000

D5 : Address test mode **0**:normal 1:test

D4 : rsv

D3 : Palette access enable **0**:Palette off (through) 1:Palette enable

D2 : Palette input select **0**:Processor 1:Display

D1:0 : Graphics mode **00**:Disable(Stop VRAM read) 01:8bpp 10:16bpp 11:rsv

Changing Palette sequence

(1) Set Display off D1,0=00

(2) Switch Palette mode Display to CPU D3=0

(3) Change Palette of any index

(4) Switch Palette mode CPU to Display D3=1

(5) Enable display D1,0 = 01 or 11

5.6.11.9 BitBlt Memory mapped I/O (Wait controlled)

offset	31-24	23-16	15-08	07-00
003-000h				BitBlt control
007-004h		FIFO Base address		
00B-008h		FIFO Write address		
00F-00Ch				Command count
013-010h				Int com count
017-014h				
01B-018h				
01F-01Ch				
023-020h				LCD Color Depth
027-024h				LCD FIFO Int
02B-028h			LCD Src Vertical offset (Default)	
02F-02Ch			LCD Msk Vertical offset (Default)	
033-030h			LCD Dst Vertical offset (Default)	
037-034h				
03B-038h				
03F-03Ch				
043-040h				CRT Color Depth
047-044h				CRT FIFO Int
04B-048h			CRT Src Vertical offset (Default)	
04F-04Ch			CRT Msk Vertical offset (Default)	
053-050h			CRT Dst Vertical offset (Default)	
057-054h				
05B-058h				
05F-05Ch				
063-060h				
067-064h				
06B-068h				
06F-06Ch				
073-070h				
077-074h				
07B-078h				
07F-07Ch				

5.6.11.10 BitBlt Register

BitBlt Control

I/O	Offset	Reg. Name	R/W	31:4	4	3	2	1	0	Initial
MMIO	000 00	PBCNT	W	0	-	-	STPCK	FRST	BBEN	00000000
			R	0	HLT	CKOFF	STPCK	FRST	BBEN	00000000

D4 : Hlat status 0:BitBlt Halt 1:Running

D3 : Clock status 0:Clocking 1:Clock Stopped

D2 : Clock stop 0:Always clocking 1:Stop Enable

D1 : FIFO reset 0:Reset 1:Enable

D0 : BitBlt command enable 0:Disable(Halt) 1:Enable

Resetting D0 halt BitBlt after current command excution complete. Halt staus can be read from D4.

FIFO Base Address

I/O	Offset	Reg. Name	R/W	31:22	21:12	11:3	2:0	Initial
MMIO	004 01	PBFBA	W	0	FIFO Address	0	0	00000000
			R	0	FIFO Address	Command addr	0	00000000

D21-12 : FIFO Base address in the VRAM Size 4K byte.

D11-3 : FIFO command address BitBlt fetch command from this address

FIFO Write Address

I/O	Offset	Reg. Name	R/W	31:8	21:3	2:0	Initial
MMIO	008 02	PBFWA	R/W		FIFO Address	0	00000000

D21-3 : FIFO command write address

Driver use this register for saving FIFO write address.

FIFO Command Count

I/O	Offset	Reg. Name	R/W	31:9	8:0	Initial
MMIO	00C 03	PBFCC	R	0	FIFO count	00000000

D8-0 : The number of commands in the FIFO Maximum 511 commands.

Decrement when BitBlt fetch command form FIFO

Writing to this register is allowed only for diagnostic usage.

Interrupt Command Count

I/O	Offset	Reg. Name	R/W	31:9	8:0	Initial
MMIO	010 04	PBICC	R/W	0	FIFO count	00000000

D8-0 : FIFO threshold value to generate FIFO threshold interrupt

When pending count is decrement interrupt is generated if counter value is equal to this register.

LCD Color Depth

I/O	Offset	Reg. Name	R/W	31:2	1:0	Initial
MMIO	020 08	PBBPPL	R/W	0	BPP	00000000

D1-0: Color Depth 00:8bpp 01:16bpp 10:rsv 11:rsv

LCD Interrupt Command Count Enable

I/O	Offset	Reg. Name	R/W	31:1	0	Initial
MMIO	024 09	PBICEL	R/W	0	EN	00000000

D0 : FIFO count int enable 0:Disable 1:Enable

LCD Source Vertival Offset (Default)

I/O	Offset	Reg. Name	R/W	31:16	15:0	Initial
MMIO	028 10	PBSVOL	R/W	0	Offset	00000000

D15-0 : Source Default Vertical offset

Set positive value for both directions

This register initialized at setup and will not be modified.

LCD Mask Vertival Offset (Default)

I/O	Offset	Reg. Name	R/W	31:16	15:0	Initial
MMIO	02C 0A	PBMVOL	R/W	0	Offset	00000000

D15-0 : Mask Default Vertical offset

Set positive value for both directions

This register initialized at setup and will not be modified.

LCD Destination Vertival Offset (Default)

I/O	Offset	Reg. Name	R/W	31:16	15:0	Initial
MMIO	030 0B	PBDVOL	R/W	0	Offset	00000000

D15-0 : Destination Default Vertical offset

Set positive value for both directions

This register initialized at setup and will not be modified.

CRT Color Depth

I/O	Offset	Reg. Name	R/W	31:2	1:0	Initial
MMIO	040 10	PBBPPC	R/W	0	BPP	00000000

D1-0: Color Depth 00:8bpp 01:16bpp 10:rsv 11:rsv

CRT Interrupt Command Count Enable

I/O	Offset	Reg. Name	R/W	31:1	0	Initial
MMIO	044 11	PBICEC	R/W	0	EN	00000000

D0 : FIFO count int enable 0:Disable 1:Enable

CRT Source Vertival Offset (Default)

I/O	Offset	Reg. Name	R/W	31:16	15:0	Initial
MMIO	048 12	PBSVOC	R/W	0	Offset	00000000

D15-0 : Source Default Vertical offset

Set positive value for both directions

This register initialized at setup and will not be modified.

CRT Mask Vertival Offset (Default)

I/O	Offset	Reg. Name	R/W	31:16	15:0	Initial
MMIO	04C 13	PBMVOC	R/W	0	Offset	00000000

D15-0 : Mask Default Vertical offset

Set positive value for both directions

This register initialized at setup and will not be modified.

CRT Destination Vertival Offset (Default)

I/O	Offset	Reg. Name	R/W	31:16	15:0	Initial
MMIO	050 14	PBDVOC	R/W	0	Offset	00000000

D15-0 : Destination Default Vertical offset

Set positive value for both directions

This register initialized at setup and will not be modified.

5.7. PCMCIA controller

5.7.1. Features

- It is accessible to the register set as the memory accesses.
- It uses MCS0, MCS1 space for the access from TX3922.
- It is equipped with five Memory/Attribute, two I/O Window in every slot.
- The control of PCMCIA Card power chip [TPS2205 which is made by the TI company] of the external
- 3.3V/5V It corresponds to Card.
- Memory/Attribute Window is accessible in the memory space of a maximum of 64 MB.
- I/O Window is accessible in a maximum of 64KB I/O space.
- The PCMCIA V2.0/JEIDA V4.1 specification compatibility (It doesn't support Card-Bus, ZV-Port).

5.7.2. Address mapping

(1) Configuration register

The base address of the configuration register

The PCMCIA configuration register 10805000H

(2) The access by the PCMCIA controller

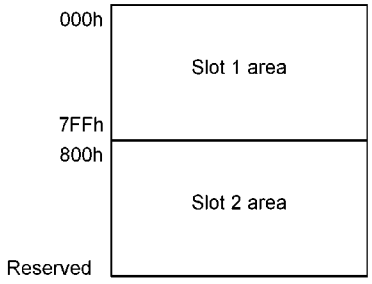
It accesses from the space of MCS.

73FFFFFFH	
70000000H	Memory Attribute
6E000000H	Memory Attribute
6D000000H	Memory Attribute
6C800000H	Memory Attribute
6C700000H	I/O
6C600000H	I/O

5.7.3. About the card register set and the slot register space

The PCMCIA card register set is the register group which controls the PCMCIA controller which is had by PLUM.

This register set is basically prepared every PCMCIA card slot and can access this register set like usual access by the memory.



There are 2 slots of PCMCIA to handle in PLUM2, and they divide 4 K bytes of PCMCIA register space in 2 and are using it as the area of the register set by each slot.

If that is, show by the lower rank address (12 bits)

000h-7FFh : Slot 1

800h-FFFh : Slot 2

It becomes.

It supposes that "Offset" to be defining here shows Offset from the base address (000h,800h) of each slot.

5.7.4. The classification of the register set

The PCMCIA card register set can be divided into two when roughly dividing it.

1. The register group which does detailed setting every slot (Offset 000h-0FCh URxxH is described in the specification)

   This register group can not be used if it doesn't set slot ON (Offset 100-h bit 7).

2. The register group which sets in config (Offset -110 h of 100h HRxxH is described in the specification)

   This area is accessible generally in the condition.

5.7.5. About the register function by the various mode

At the PCMCIA controller, it is PCMCIA Function Select Register By the mode which is shown by the bit of (Offset 0F8h), the function of the register can be changed.

008h (Power Control Register[UR02H])	The 3.3v mode can be supported.
058h (Additional General Register[UR16H])	CVS Pin(Voltage Sense Status Pin) The condition which is can be read.
01Ch (I/O Window Control Register[UR07H])	The I/O access timing can be changed.
04Ch,06Ch,08Ch,0ACh,0CCh (Memory Window n Control Register [UR13H,UR1BH,UR23H,UR2BH,UR33H])	The memory access timing can be changed.
0ECh (PCMCIA Card Timing Register [UR3BH])	The access timing to Card can be changed.

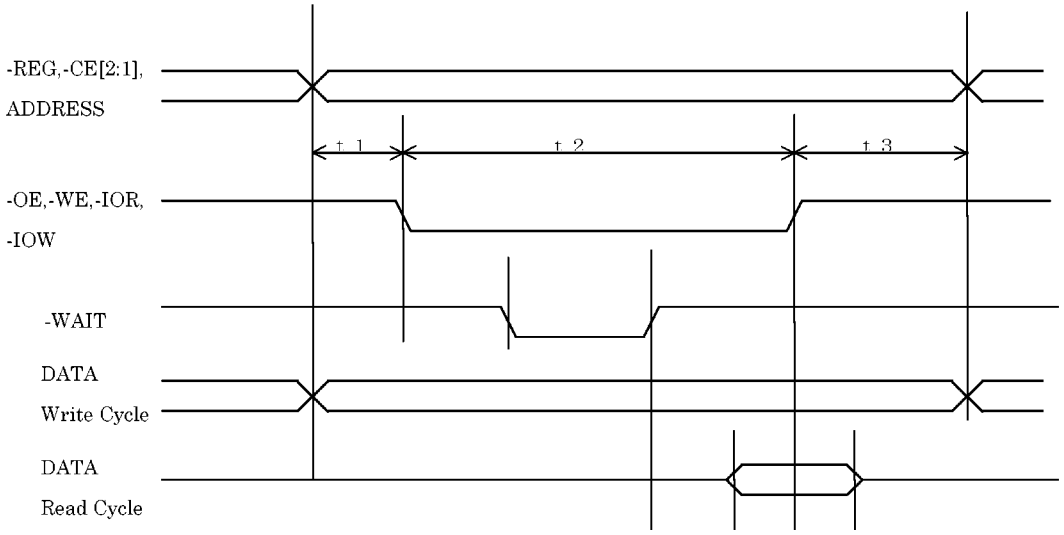
5.7.6. Access timing table

It gathers the access timing of the memory card, the I/O card.

memory access	t1	t2	t3
2 ISACLK Mode	6 CLKS	4 CLKS	2 CLK
3 ISACLK Mode	6 CLKS	8 CLKS	2 CLK
4 ISACLK Mode	6 CLKS	12 CLKS	2 CLK
5 ISACLK Mode	6 CLKS	16 CLKS	2 CLK
6 ISACLK Mode	6 CLKS	20 CLKS	2 CLK

IO access	t1	t2	t3
3 ISACLK Mode	7 CLKS	6 CLKS	2 CLK
4 ISACLK Mode	7 CLKS	10 CLKS	2 CLK
6 ISACLK Mode	7 CLKS	18 CLKS	2 CLK

The above CLK shows the number of system clock (CLKBUS / 2).



5.7.7. Register list

Register set < 1 >

PCMCIA Controller register set is shown below.

All of these registers are a register with 32 bit width.

Registers Table

offset	Register name		Register attribute
000h	Identification and Revision	[UR00H]	R(READ)/W(WRITE)
004h	Interface Status	[UR01H]	R
008h	Power Control	[UR02H]	R/W
00Ch	Interrupt and General Control	[UR03H]	R/W
010h	Card Status Change	[UR04H]	R/W
014h	Card Status Change Interrupt Control	[UR05H]	R/W
018h	Window Enable	[UR06H]	R/W
01Ch	I/O Window Control	[UR07H]	R/W
020h	I/O Window 0 Start Address	[UR08H]	R/W
024h	I/O Window 0 Stop Address	[UR09H]	R/W
030h	I/O Window 1 Start Address	[UR0CH]	R/W
034h	I/O Window 1 Stop Address	[UR0DH]	R/W
040h	Memory Window 0 Start Address	[UR10H]	R/W
044h	Memory Window 0 Stop Address	[UR11H]	R/W
048h	Memory Window 0 Offset Address	[UR12H]	R/W
04Ch	Memory Window 0 Control	[UR13H]	R/W
058h	Additional General Control	[UR16H]	R/W
060h	Memory Window 1 Start Address	[UR18H]	R/W
064h	Memory Window 1 Stop Address	[UR19H]	R/W
068h	Memory Window 1 Offset Address	[UR1AH]	R/W
06Ch	Memory Window 1 Control	[UR1BH]	R/W
078h	Global Control	[UR1EH]	R/W
080h	Memory Window 2 Start Address	[UR20H]	R/W
084h	Memory Window 2 Stop Address	[UR21H]	R/W
088h	Memory Window 2 Offset Address	[UR22H]	R/W
08Ch	Memory Window 2 Control	[UR23H]	R/W
0A0h	Memory Window 3 Start Address	[UR28H]	R/W
0A4h	Memory Window 3 Stop Address	[UR29H]	R/W
0A8h	Memory Window 3 Offset Address	[UR2AH]	R/W
0ACh	Memory Window 3 Control	[UR2BH]	R/W
0C0h	Memory Window 4 Start Address	[UR30H]	R/W
0C4h	Memory Window 4 Stop Address	[UR31H]	R/W
0C8h	Memory Window 4 Offset Address	[UR32H]	R/W

offset	Register name		Register attribute
0CCh	Memory Window 4 Control	[UR33H]	R/W
0ECh	PCMCIA Card Timing Register	[UR3BH]	R/W
0F0h	Reserved Register	[UR3CH]	R/W
0F8h	PCMCIA Function Control Register	[UR3EH]	R/W
0FCh	Special Mode Register	[UR3FH]	R/W
100h	Slot Control Register	[HR00H]	R/W
104h	Buffer Off Register	[HR01H]	R/W
108h	Card Detect Mode Register	[HR02H]	R/W
10Ch	Card Power Shut Down Register(Common)	[HR03H]	R/W

Register set < 2 >

Offset	31:24	23:16	15:08	07:00
000h				Identification and Revision
004h				Interface Status
008h				Power Control
00Ch				Interrupt and General ctrl
010h				Card Status Change
014h				Card Status Change Int ctrl
018h				Window Enable
01Ch				I/O Window Control
020h			I/O Window 0 Start Address	
024h			I/O Window 0 Stop Address	
028h				
02Ch				
030h			I/O Window 1 Start Address	
034h			I/O Window 1 Stop Address	
038h				
03Ch				
040h			Memory Window 0 Start Address	
044h			Memory Window 0 Stop Address	
048h			Memory Window 0 Offset Address	
04Ch	Memory Window 0 Control			
050h				
054h				
058h				Additional General Control
05Ch				
060h			Memory Window 1 Start Address	
064h			Memory Window 1 Stop Address	
068h			Memory Window 1 Offset Address	
06Ch	Memory Window 1 Control			
070h				
074h				
078h				Global Control
07Ch				
080h			Memory Window 2 Start Address	
084h			Memory Window 2 Stop Address	
088h			Memory Window 2 Offset Address	
08Ch	Memory Window 2 Control			
090h				
094h				
098h				
09Ch				
0A0h			Memory Window 3 Start Address	
0A4h			Memory Window 3 Stop Address	
0A8h			Memory Window 3 Offset Address	
0ACh	Memory Window 3 Control			
0B0h				
0B4h				
0B8h				
0BCh				

0C0h			Memory Window 4 Start Address	
0C4h			Memory Window 4 Stop Address	
0C8h			Memory Window 4 Offset Address	
0CCh	Memory Window 4 Control			
0D0h				
0D4h				
0D8h				
0DCh				
0E0h				
0E4h				
0E8h				
0ECh				PCMCIA Card Timing
0F0h				Reserved
0F4h				PCMCIA DMA Control
0F8h				PCMCIA Function Control
0FCh				Special Mode
100h				Slot Control
104h				Buffer Off
108h				Card Detect Mode
10Ch				Card Power Shut Down
110h				
114h				
118h				
11Ch				

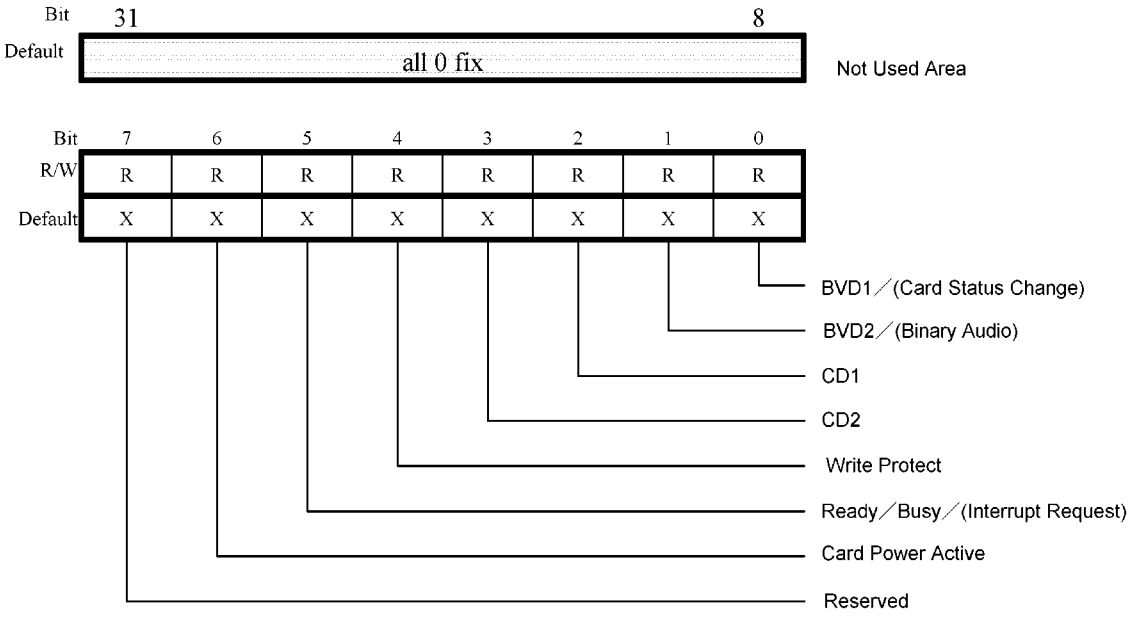
5.7.8. Details of the register

The register group which puts below exists every function block unit which is called a slot.

(Offset It excludes 078 h Global Control Register, TBD).

This controller is supporting these two slots.

(1)Interface Status Register (Offset 004h、[UR01H])



The description which can depend with the brackets is the terminal name when choosing (Offset setting 5 bits of D of 00Ch[UR03H] to 1) I/O card interface.

This register is the register of the read-only and can see the condition of each terminal as the Register data. (But, while the clock stops, the condition of each terminal can not be seen).

When a card isn't inserted by the inner gate, it is fixed on "H" about BVD2, Ready/Busy, Write Protect.

D7 (Reserved)

It is possible to read always "H".

D6 (Card Power Active)

The condition of the power which a card is supplied to can be read.

(It becomes "1" when a power is impressed by the card.)

D5 (Ready/Busy (/Interrupt Request))

When choosing a memory card interface, it becomes "1" in the Ready condition and it becomes "0" in the Busy condition.

At the time of the I/O card interface, it becomes "0" in case of the I/O interrupt (IREQZ) occurrence.

D4 (Write Protect)

It is effective only when choosing a memory card interface.

It becomes "1" at the time of the write protect and the non- write protect becomes "0" sometimes.

Incidentally, when choosing I/O card interface, it is possible to read "0". (When a card is inserted)

D3-D2 (CD1-CD2)

When detecting (inserted)a card, it becomes "1" and when not detected, it becomes "0".

D1 (BVD2(Binary Audio))

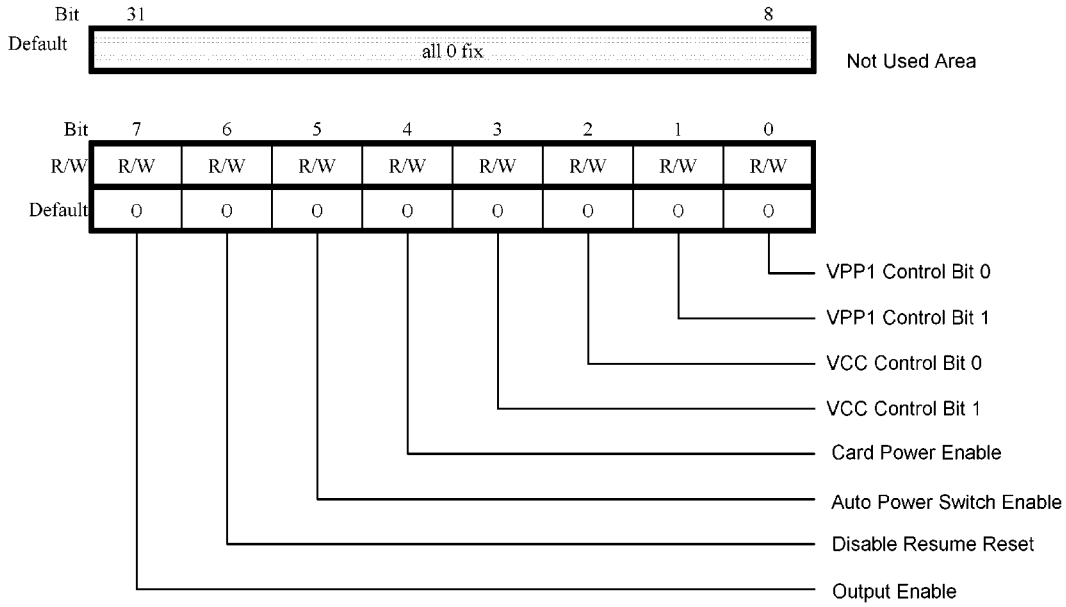
It shows the battery condition of the memory in the combination with BVD1 in case of the memory card interface. In case of the I/O card interface, it is possible to read Binary Audio.

D0 (BVD1(Card Status Change))

It shows the battery condition of the memory in the combination with BVD2 in case of the memory card interface. In case of the I/O card interface, it is possible to read Card Status Change (RIOUT) .

	Normal	Warning	Dead
BVD1 (D0)	1	1	0
BVD2 (D1)	1	0	X

(2) Power Control Register (Offset 008h、[UR02H])



With this register, it is doing the 3.3 V correspondence of the card power.

D7(Output Enable)

The output signal, all input/output signals to the card which is shown below the time when this bit is "0" become high impedance.

CE1#、CE2#、OE#、WE#/PGM#、IORD#、IOWR#、REG#、RESET、A25-00、D15-00

D6(Disable Resume Reset)

When this bit is "0" : All registers which should be cleared with the reset by the resumption have been cleared.(All registers of Offset:000h-0FCh[URxxH])

When this bit is "1" : In the reset in case of resumption, these registers aren't cleared and maintain contents in front of suspend.

D5(Auto Power Switch enable)

By the time when this bit is "1"

By CD1 "1" of CD2 is both output which controls a power by the slot at the time of enable.
(When the card exists)

By CD1 "0" of CD2 is both output which controls a power by the slot at the time of disable.
(When there is not a card)

By the time when this bit is "0"

Only when D4 is "1", it makes the output of the power control enable even if it is in the condition which a card isn't inserted in.

D4(Card Power Enable)

When this bit is "0" : Regardless of D3 to D0 setting, Vcc, Vpp1, Vpp2 become disable.
(It doesn't supply a slot with the power).

When this bit is "1" :

PCMCIA Function Control Register(Offset 0F8h[UR3EH]) D0 It is when being "1".

According to the setting of D3, D2 by Vcc

As for Vpp, according to the setting of D1, D0, the power control terminal changes.

(Table reference below)

PCMCIA Function Control Register(Offset 0F8h[UR3EH]) D0 It is when being "0".

At the time of Vcc=3.3 V in the following table, it becomes Vcc=0V. (※)

But, when D5 is "1" even if this bit meets in "1" and moreover a card isn't inserted in the slot, it doesn't supply a slot with the power.

PCMCIA Function Control Register(Offset 0F8h[UR3EH]) D0 It is when being "1".

(Vcc 3 V mode support)

Common Shut-Down	CARD ON*	02H Power Control Register						Terminal output					Power supply	
		5	4	3	2	1	0	SD	Vc3	Vc5	PPG	PVC	Vcc	Vpp
1	X	X	0	X	X	X	X	0	0	0	0	0	Hi-Z	Hi-Z
0	X	X	0	X	X	X	X	1	0	0	0	0	0	0
	X	0	1	It refers to the following table.				1	It refers to the following table.					
	1	1	1											
	0	1	1	X	X	X	X	1	0	0	0	0	0	0

* CARDON shows the condition which a card was inserted in at the time of "1".

* Common Shut-Down is common with both slots of PCMCIA and is used.
Refer to Card Power Shut-Down Control Register (Offset:10Ch[HR03H]).

D3-D2(Vcc Control bit)

Vcc power control

02H Power Control Register		Terminal output		Power supply
3	2	Vc3	Vc5	Vcc
0	0	0	0	0V
0	1	0	1	3.3V※
1	0	1	0	5V
1	1	1	1	0V

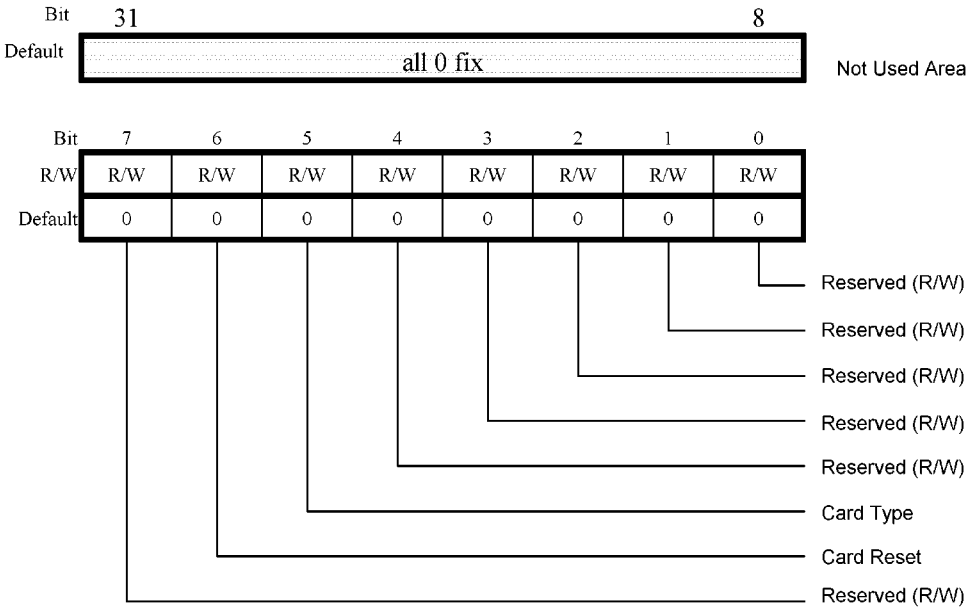
※PCMCIA Function Control Register(Offset 0F8h[UR3EH]) D0 (Power Control Enable) In case of being "0", it becomes Vc3=0, Vc5=0 and becoming Vcc=0V with this case.

D1-D0(Vpp Control bit)

Vcc power control

02H Power Control Register		Terminal output		Power supply
1	0	PPG	PVC	Vpp
0	0	0	0	0 V
0	1	0	1	Vcc
1	0	1	0	0 V
1	1	1	1	Hi-Z

(3) Interrupt and General Control Register (Offset 00Ch、 [UR03H])



D7(Reserved)

Doing R/W can.

D6(Card Reset)

The reverse of the signal to have set to this bit is output from the CRESET terminal.

It becomes a reset condition when setting "0".

0 : Reset

1 : Normal(The condition which is not Reset)

D5(Card Type)

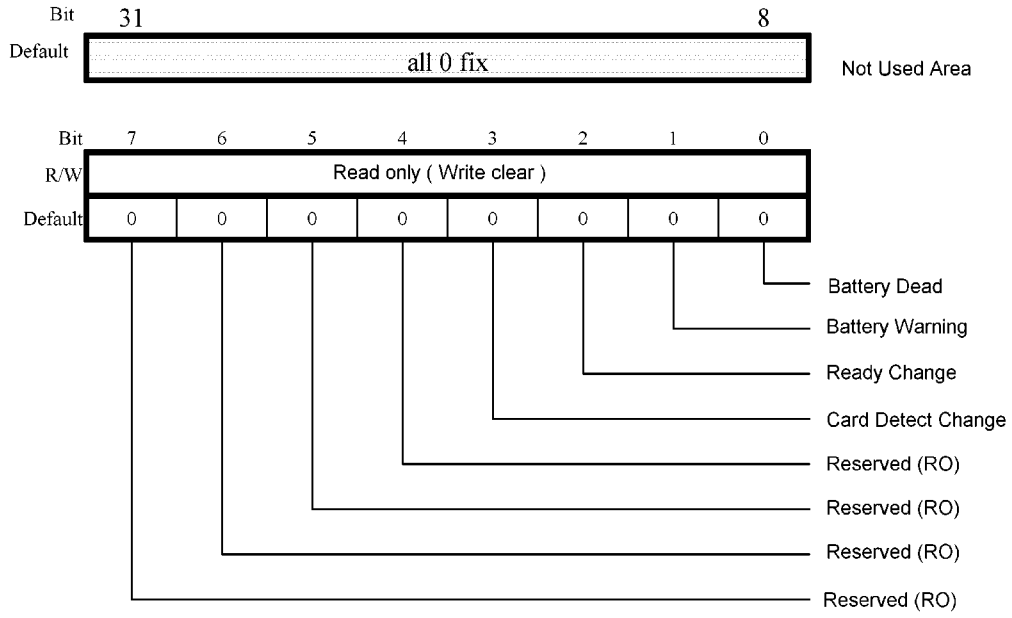
0 : Memory Card

1 : I/O Card

D4 to D0(Reserved)

Doing R/W can.

(4)Card Status Change Register (Offset 010h、 [UR04H])



The description which can depend with the brackets is the terminal name when setting Interrupt and General Control Register (Offset 00Ch、 [UR03H]) D5 to 1.

At this register, it is a read only register and it maintains the condition of the change of the card status signal. But, the write operation sometimes has a meaning, too.

(The following reference to the way of clearing a register)

When there is a change in Enable and the set card status signal according to Card Status Change Control Register (Offset 014h[UR05H]) "1" is set in the bit which this register corresponds to. Also, the squeeze occurs from the IRQ line at the same time.

When there is a change in Disable and the set card status signal according to Card Status Change Control Register (Offset 014h[UR05H]) Even if the corresponding status signal changes, "1" doesn't stand in the bit of this register.

To clear the bit where "1" stood with this register, there are two ways.

If Global Control Register(Offset 078h[UR1EH]) D2 is "0", it heads this register only, all the bit where "1" of D3-D0 stands are cleared and the IRQ line gets for the in to be active.

When Global Control Register D2 is "1".

In the read operation, it isn't cleared and it clears by "1" writing "1" to the drawn bit.

(Write back operation)

When all bits aren't cleared in this Write back mode because it is possible to 1 bit clear, the IRQ line doesn't get for the in to be active.

D7 to D4(Reserved)

It is possible to read "0".

D3(Card Detect Change)

The CD1 terminal, both CD2 terminals are in the condition of "L". (The card exists at the slot).

→ When either becomes "H"(In other words, it detected when a card was pulled out). Or

The CD1 terminal, both CD2 terminals are in the condition of "H". (The card is not in the slot).

→ When both become "L"(In other words, it detected when a card was inserted).

Then , this bit becomes "1".

As for the pulling-out putting-in of a card in suspend, this bit is set after resumption.

But, in suspend (while the PCMCIA clock stops), as for this detection function, because it doesn't work, independently, it isn't possible to do card detection of this function.

In suspend, it gets to detect a lock switch operation squeeze on the side of the system.

Above-mentioned operation is Card Status Change Control Register Effectively only when (Offset 014h[UR05H])D3 is "1", at the time of "0", this bit doesn't change as "0".

(The Software card detect function, too, is invalid).

Also, because it is the bit of the pulling-out putting-in detection, it doesn't depend on the mode of the operation of the card, too.

D2(Ready Change)

When the RDY/#BSY signal transfers to Low to High in Memory card interface, it becomes 1 and Card Status Change Interrupt occurs to this bit.

When once set, even if RDY/#BSY returns to Low from High, the condition which 1 was set in is maintained.

The change of the RDY/BSY# pin in the condition that the card is not in the slot and after card insertion, it prohibits the change of the RDY/BSY# pin for about 1 ms from detecting by this function.(It is possible to read always "0".).

Above-mentioned operation is effectively only when Card Status Change Control Register (Offset 014h[UR05H]) D2 is "1", at the time of "0", this bit doesn't change as "0".

Also, when the operation mode is IO card interface, too, it is possible to read always "0".

D1(Battery Warning)

When changing into the Battery Warning condition (BVD2=Low as BVD1=High) from the Battery Good condition (BVD1=High and moreover BVD2=High) in Memory card interface, this bit becomes "1" and Card Status Change Interrupt occurs.

When once set, even if it returns, the condition which "1" was set in is maintained by the Battery Good condition. Also, it becomes Battery Warning condition and after this bit becomes "1", when changing into the Battery Dead condition (when BVD1 becomes Low), when the bit of Battery Dead is set, this bit has been cleared.(The bit of Battery Dead is had priority over).

The change of the BVD1,BVD2 pin in the condition that the card is not in the slot and after card insertion, it prohibits the change of the BVD1,BVD2 pin for about 1 ms from detecting this function. (0 can be always read.)

Above-mentioned operation is effective only when Card Status Change Control Register (Offset 014h[UR05H]) D1 is "1" and at the time of "0", this bit doesn't change as "0".

Also, when the operation mode is IO Card Interface, too, it is possible to read always "0".

D0(Battery Dead)

In Memory Card Interface, it is in the Battery Good condition (BVD1=High and moreover BVD2=High) and the Battery Warning condition (BVD1=High and moreover BVD2=Low) This bit becomes "1" and Card Status Change Interrupt occurs when transferring to the condition to Battery Dead condition (BVD1=Low).

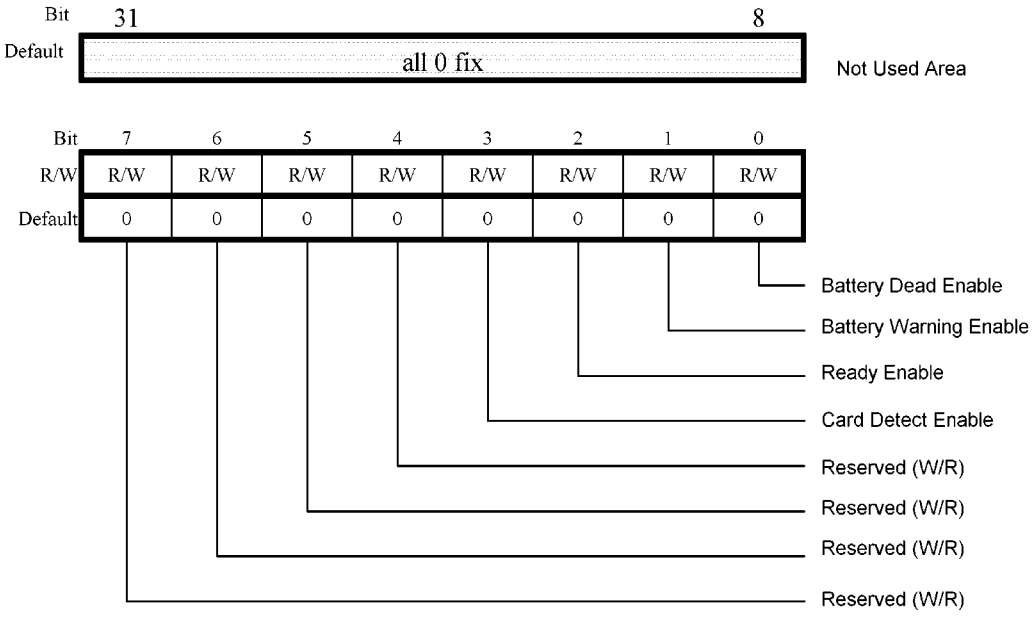
When once set, even if it returns, the condition which 1 was set in is maintained by the Battery Good condition and the Battery Warning condition.

The change of the BVD1,BVD2 pin in the condition that the card is not in the slot and after card pulling-out putting-in, it prohibits the change of the BVD1,BVD2 pin for about 1 ms from detecting this function. (It is possible to read always "0").

In the setting of IO Card Interface, this bit can read "0".

Above-mentioned operation is effective only when Card Status Change Control Register (Offset 014h[UR05H]) D0 is "1" and at the time of "0", this bit doesn't change as "0".

(5) Card Status Change Interrupt Control Register (Offset 014h、[UR05H])



D7 to D4(Reserved)

Doing R/W can.

D3(Card Detect Enable)

1 : Card Detect Change detection function becomes enable.

It becomes possible to make a card status changing squeeze occur by the pulling-out putting-in of a card and the Software card detect function.

0 : Card Detect Change detection function becomes disable.

D2(Ready Enable)

1 : Ready Change detection function becomes enable.

It becomes possible to make a card status changing squeeze occur when the Ready signal changes into Low from High.

0 : Ready Change detection function becomes disable.

This bit has a meaning only by the memory card interface and in the I/O card interface, it is Ready Change As for the detection function, disable is always done.

D1(Battery Warning Enable)

1 : Battery Warning detection function becomes enable.

It becomes possible to make a card status changing squeeze occur when the BVD2 signal changes into Low from High.

0 : Battery Warning detection function becomes disable.

This bit has a meaning only by the memory card interface and as for the I/O card interface, as for the Battery Warning detection function, disable is always done.

D0(Battery Dead Enable)

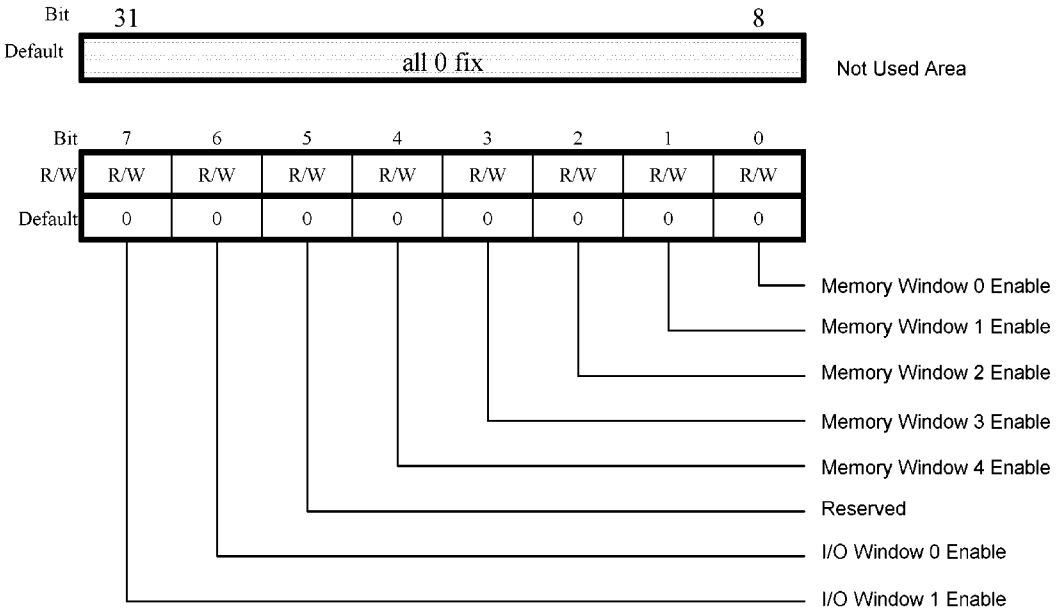
1 : Battery Dead detection function becomes enable.

It becomes possible to make a card status changing squeeze occur when the BVD1 signal changes into Low from High.

0: Battery Dead detection function becomes disable.

This bit has a meaning only by the memory card interface and as for the I/O card interface, disable is always done.

(6) Window Enable Register (Offset 018h、[UR06H])



D7(I/O Window 1 Enable)

1 : Memory access in the range of the address which is specified by Offset 030h to Offset 038h [UR0CH-UR0EH] becomes I/O access to the card.
The access by the memory in the range of the address which is specified by Offset 030h～Offset 038h[UR0CH-UR0EH] becomes I/O access to the card.
As for the address which is output to the card at this time, as for A15-00, the address of the CPU is directly output and as for A25-16, ALL'0' is output.

0 : Even if it is access by the memory in the range of the address which is specified by Offset 030h～Offset 038h[UR0CH-UR0EH], the I/O access cycle to the card doesn't occur.

D6(I/O Window 0 Enable)

1: The access by the memory in the range of the address which is specified by Offset 020h～Offset 028h[UR08H-UR0AH] It becomes I/O access to the card.
As for the address which is output to the card at this time, as for A15-00, the address of the CPU is directly output and as for A25-16, ALL'0' is output.

0 : The access by the memory in the range of the address which is specified by Offset 020h～Offset 028h[UR08H-UR0AH]Even if it meets, the I/O access cycle to the card doesn't occur.

D5(Reserved)

Doing R/W can

D4(Memory Window 4 Enable)

1 : The access by the memory in the range of the address which is specified by Offset 0C0h～Offset 0C4h,Offset 0CCh[UR30H-UR31H,UR33H] becomes access to the card by the memory.
As for the address which is output to the card at this time, as for A11-00, the address of the CPU is directly output, and as for A25-12, the offset value which is specified by the register of Offset 0C8h[UR32H] is added to the CPU address and is output.

0 : Even if it is access by the memory in the range of the address which is specified by Offset 0C0h～Offset 0C4h,Offset 0CCh[UR30H-UR31H,UR33H], the memory access cycle to the card doesn't occur.

D3(Memory Window 3 Enable)

1 : The access by the memory in the range of the address which is specified by Offset 0A0h～Offset 0A4h,Offset 0ACh[UR28H-UR29H,UR2BH] becomes access to the card by the memory.
As for the address which is output to the card at this time, as for A11-00, the address of the CPU is directly output, and as for A25-12, the offset value which is specified by the register of Offset 0A8h[UR2AH] is added to the CPU address and is output.

0 : Even if it is access by the memory in the range of the address which is specified by Offset 0A0h～Offset 0A4h,Offset 0ACh[UR28H-UR29H,UR2BH], the memory access cycle to the card doesn't occur.

D2(Memory Window 2 Enable)

1 : The access by the memory in the range of the address which is specified by Offset 080h～Offset 084h,Offset 08Ch[UR20H-UR21H,UR23H] becomes access to the card by the memory.
As for the address which is output to the card at this time, as for A11-00, the address of the CPU is directly output.
As for A25-12, the offset value which is specified by the register of Off-set 088h[UR22H] is added to the CPU address and is output.

0 : Even if it is access by the memory in the range of the address which is specified by Offset 080h～Offset 084h,Offset 08Ch[UR20H-UR21H,UR23H], the memory access cycle to the card doesn't occur.

D1(Memory Window 1 Enable)

1 : The access by the memory in the range of the address which is specified by Offset 060h～Offset 064h,Offset 06Ch[UR18H-UR19H,UR1BH] becomes access to the card by the memory.
As for the address which is output to the card at this time, as for A11-00, the address of the CPU is directly output. As for A25-12, it is Off-set The offset value which is specified by the register of 068h[UR1AH] is added to the CPU address and is output.

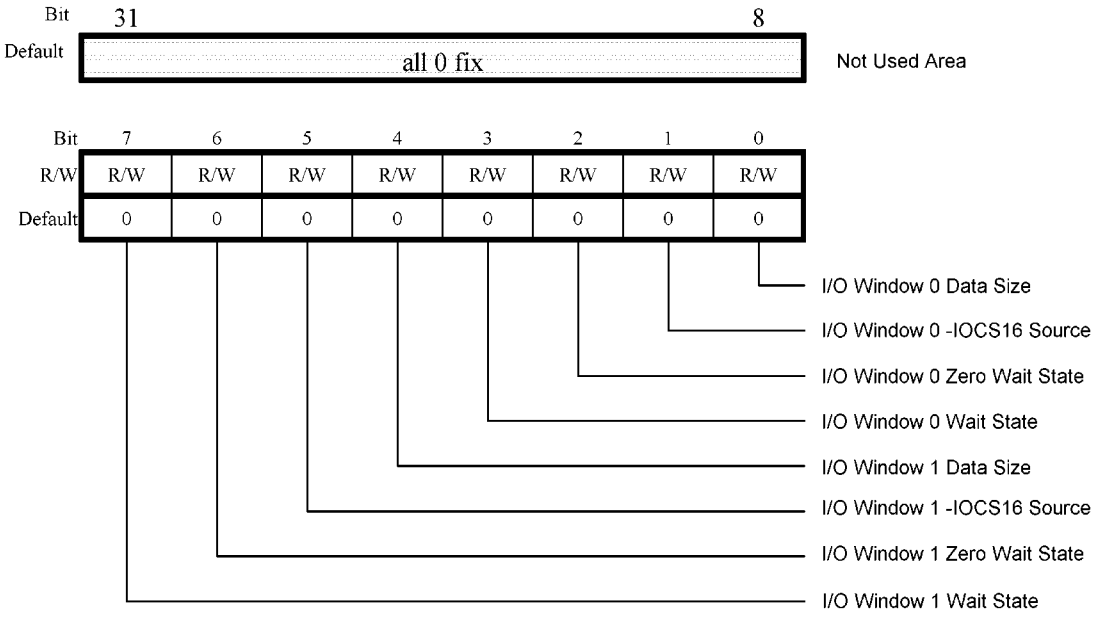
0 : Even if it is access by the memory in the range of the address which is specified by Offset 060h～Offset 064h,Offset 06Ch[UR1AH], the memory access cycle to the card doesn't occur.

D0(Memory Window 0 Enable)

1 : The access by the memory in the range of the address which is specified by Offset 040h～Offset 044h,Offset 04Ch[UR10H-UR11H,UR13H] becomes access to the card by the memory.
As for the address which is output to the card at this time, as for A11-00, the address of the CPU is directly output.
As for A25-12, it is Off-set The offset value which is specified by the register of 068h[UR1AH] is added to the CPU address and is output.

0 : Even if it is access by the memory in the range of the address which is specified by Offset 040h～Offset 044h,Offset 048h[UR10H-UR11H,UR13H], the memory access cycle to the card doesn't occur.

(7) I/O Window Control Register (Offset 01Ch、[UR07H])



D7(I/O Window 1 Wait State)

0 : The 16 bit I/O access into the range of I/O Window1 becomes 3ISACLK mode.
(Standard bus cycle of 16 bits)

1 : The 16 bit I/O access into the range of I/O Window1 becomes 4ISACLK mode.
(1WAIT mode)

Moreover, in the WAIT signal from the card, among the activists, Wait cycle is inserted and a Bus cycle is prolonged. (WAIT priority from the card)

D6(I/O Window 1 Zero Wait State)

0 : The 8bitI/O access to I/O Window 1 becomes an average bus cycle. (6ISACLK mode)

1 : The 8bitI/O access to I/O Window 1 becomes the bus cycle (the 4ISACLK mode) of 0 wait. Also, when the WAIT signal from the card is an activist (the time of "L"), too, ZERO Wait cycle doesn't occur. (WA IT signal from the card is had priority over).

D5(I/O Window 1 -IOCS16 Source)

0 : When accessing I/O Window 1, access to the card is fixed by D4.

1 : It is fixed by the 16 bit IO access signal to the system.

D4(I/O Window 1 Data Size)

When 0 and moreover D5 (I/O Window 1 -IOCS16 Source) are 0 in this bit, the access by I/O Window1 becomes 8 bit access by the bus. (- The IOCS16 signal doesn't become active)

When 1 and moreover D5 (I/O Window 1 -IOCS16 Source) are 0 in this bit, the access by I/O Window1 becomes 16 bit access by the bus. (- The IOCS16 signal becomes active)

But, when D5 is “1”, this bit doesn't have a meaning.

D3(I/O Window 0 Wait State)

0 : The 16 bit I/O access into the range of I/O Window0 becomes 3ISACLK mode.
(Standard bus cycle of 16 bits)

1 : The 16 bit I/O access into the range of I/O Window0 becomes 4ISACLK mode. (1WAIT mode)
Moreover, in the WAIT signal from the card, among the activists, Wait cycle is inserted and a Bus cycle is prolonged. (WAIT priority from the card)

D2(I/O Window 0 Zero Wait State)

0 : The 8bitI/O access to I/O Window0 becomes an average bus cycle. (6ISACLK mode)

1 : The 8bitI/O access to I/O Window0 is the bus cycle of 0 wait. It becomes. (4ISACLK mode)
Also, when the WAIT signal from the card is an activist (the time of "L"), too,
ZERO wait cycle doesn't occur. (WAIT from the card is had priority over).

D1(I/O Window 0 -IOCS16 Source)

0 : When accessing I/O Window0, access to the card is fixed by D0.

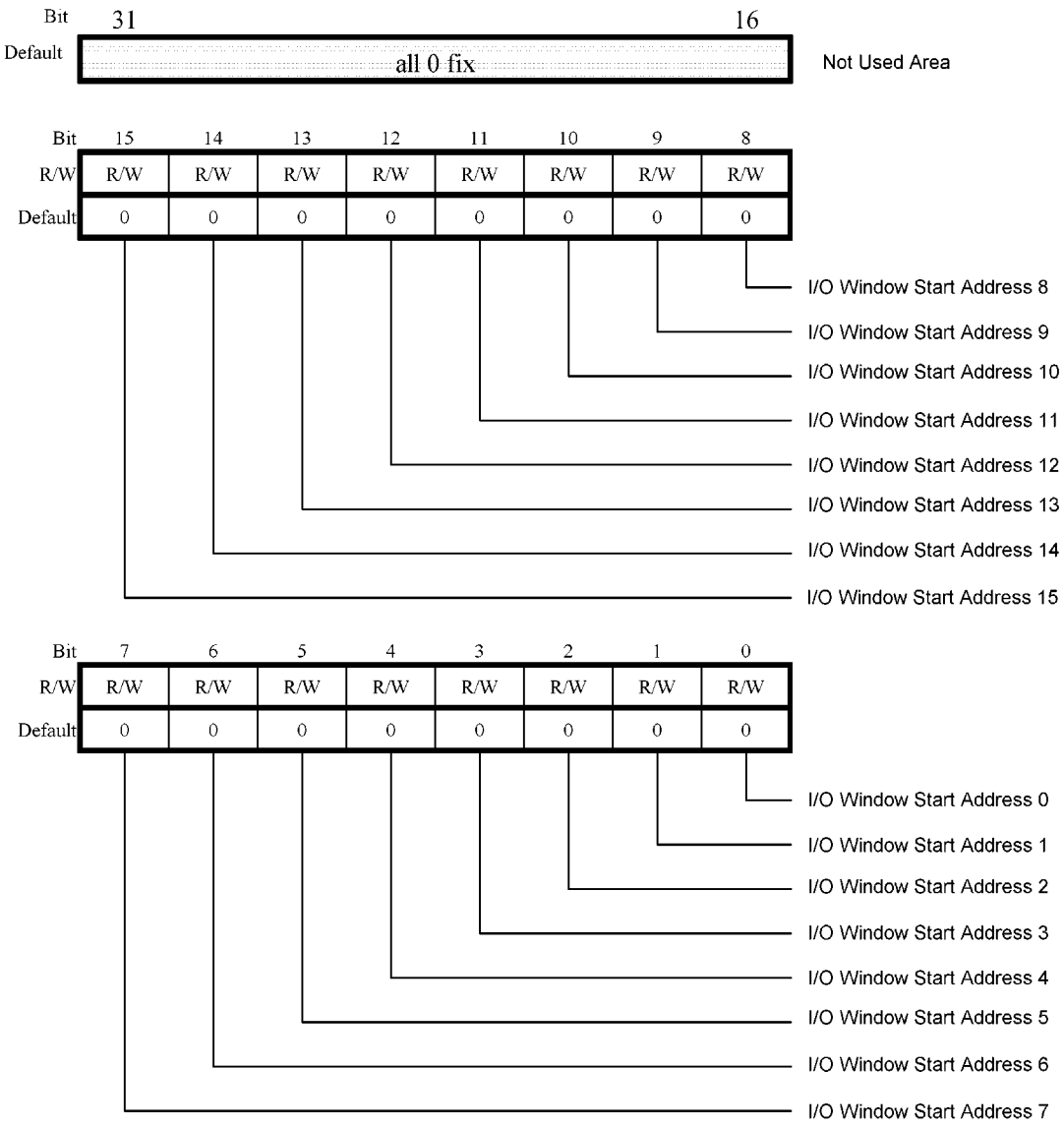
1 : It is fixed by the 16 bit IO access signal to the system.

D0(I/O Window 0 Data Size)

When “0” and moreover D1(I/O Window 0 -IOCS16 Source) are “0” in this bit, the access by I/O Window0 becomes 8 bit access by the bus. (- The IOCS16 signal doesn't become active).
When “1” and moreover D1 (I/O Window 0 -IOCS16 Source) are “0” in this bit, the access by I/O Window0 becomes 16 bit access by the bus.(- The IOCS16 signal becomes active).
But, when D1 are “1”, this bit doesn't have a meaning.

(8) I/O Window n Start Address Register **Offset 020h(n=0) [UR08H]**

Offset 030h(n=1) [UR0CH]

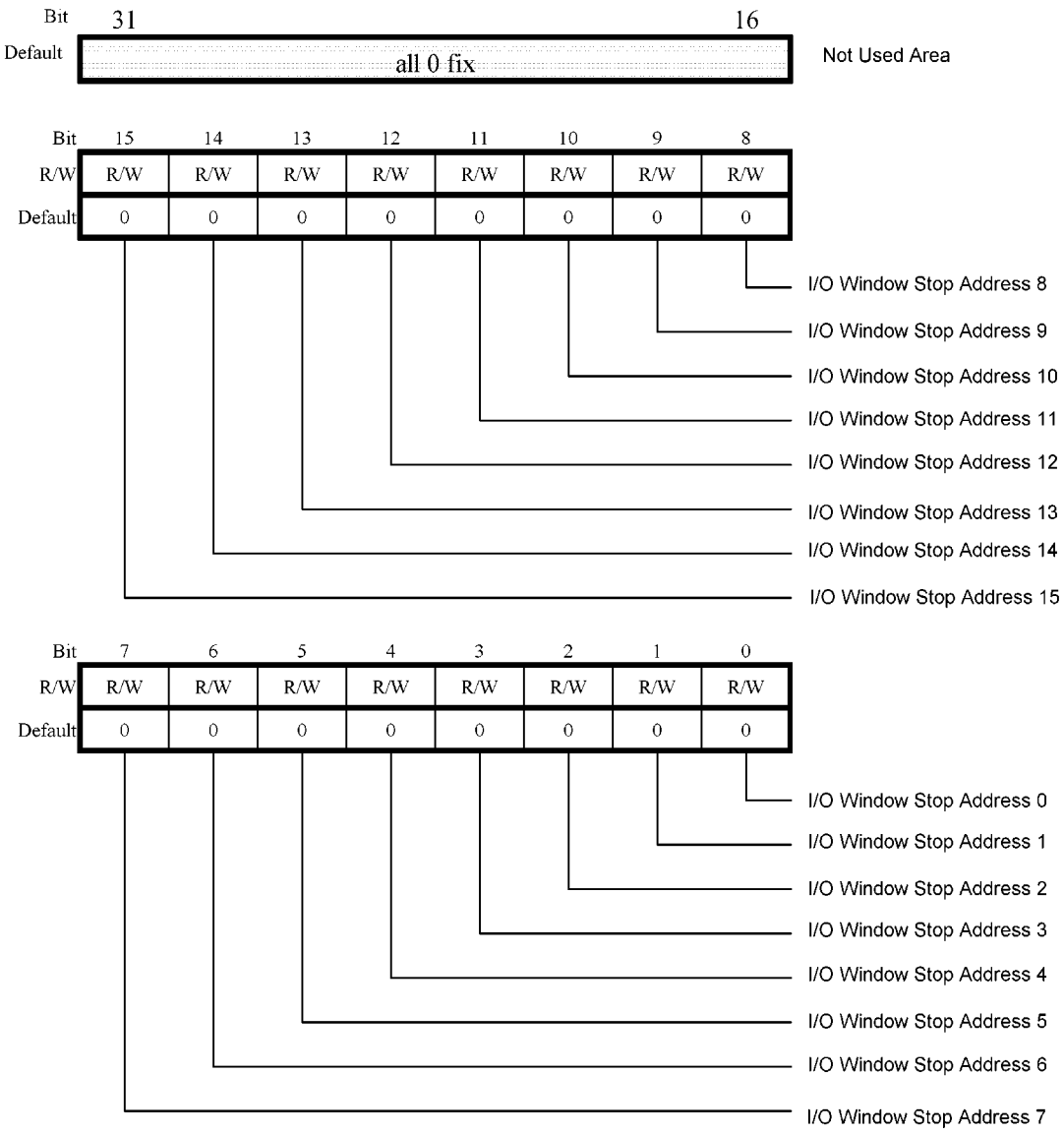


This register is the register to set the start address of I/O window n(n=0,1).

D15 to D0(Address 15-0)

The start address of I/O window n(n=0,1)

(9) I/O Window n Stop Address Register Offset 024h(n=0) [UR09H]
Offset 034h(n=1) [UR0DH]

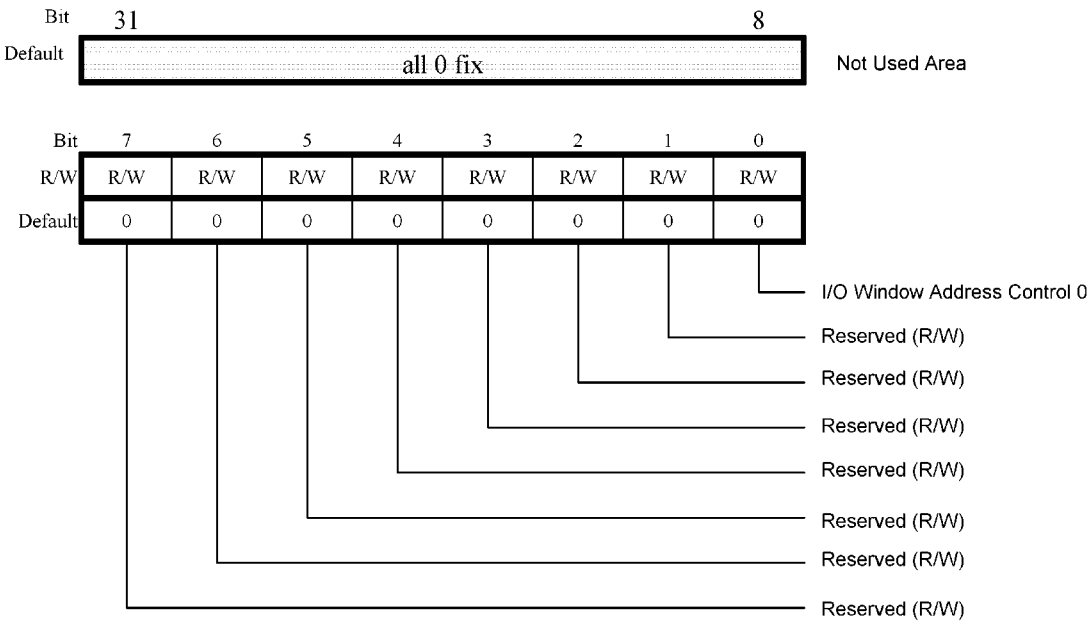


This register is the register to set the stop address of I/O window n(n=0,1).

D15-D0(Address 15-0)

The stop address of I/O window n(n=0,1)

(10) I/O Window n Address Control Register **Offset 028h(n=0) [UR0AH]**
Offset 038h(n=1) [UR0EH]



This register is the register to set the address of I/O window n(n=0,1).

D7 to D1(Reserved)

Doing R/W can

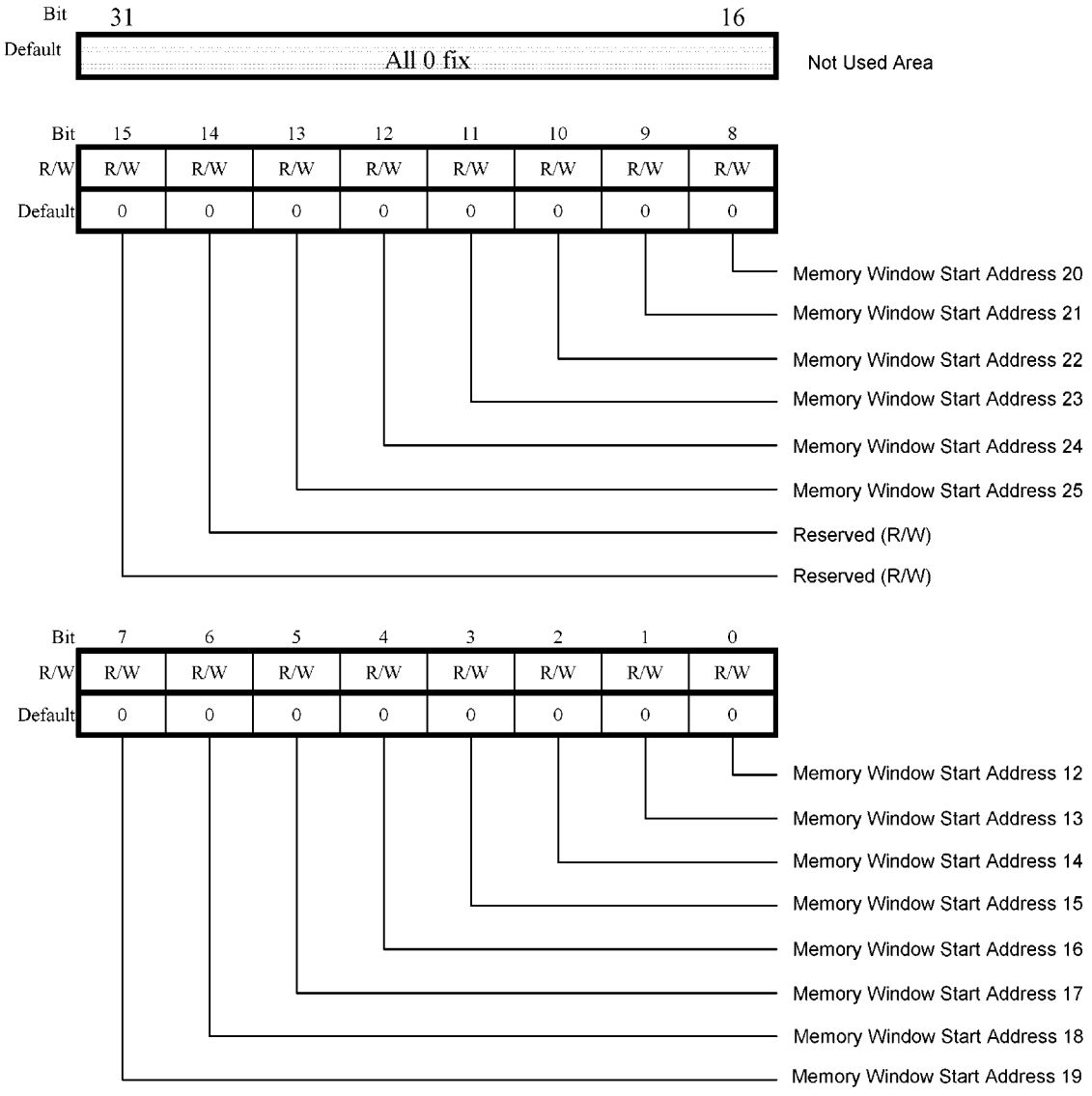
D0(I/O Window n Address Control)

It makes the I/O window n(n=0,1) which was specified by the start address - the stop address PCMCIA I/O area in the system space in the mapping.

Two PCMCIA I/O areas do a mapping like the following table when there are they and they do respectively in I/O area 1, I/O area 2. (on the system address I/O area 1 the relation of < I/O area 2)

D0	The area of PCMCIA I/O
0	The area1 of I/O
1	The area2 of I/O

(11) Memory Window n Start Address Register **Offset 040h(n=0) [UR10H]**
Offset 060h(n=1) [UR18H]
Offset 080h(n=2) [UR20H]
Offset 0A0h(n=3) [UR28H]
Offset 0C0h(n=4) [UR30H]



This register is the register to set the start address of memory window n(n=0,1,2,3,4).

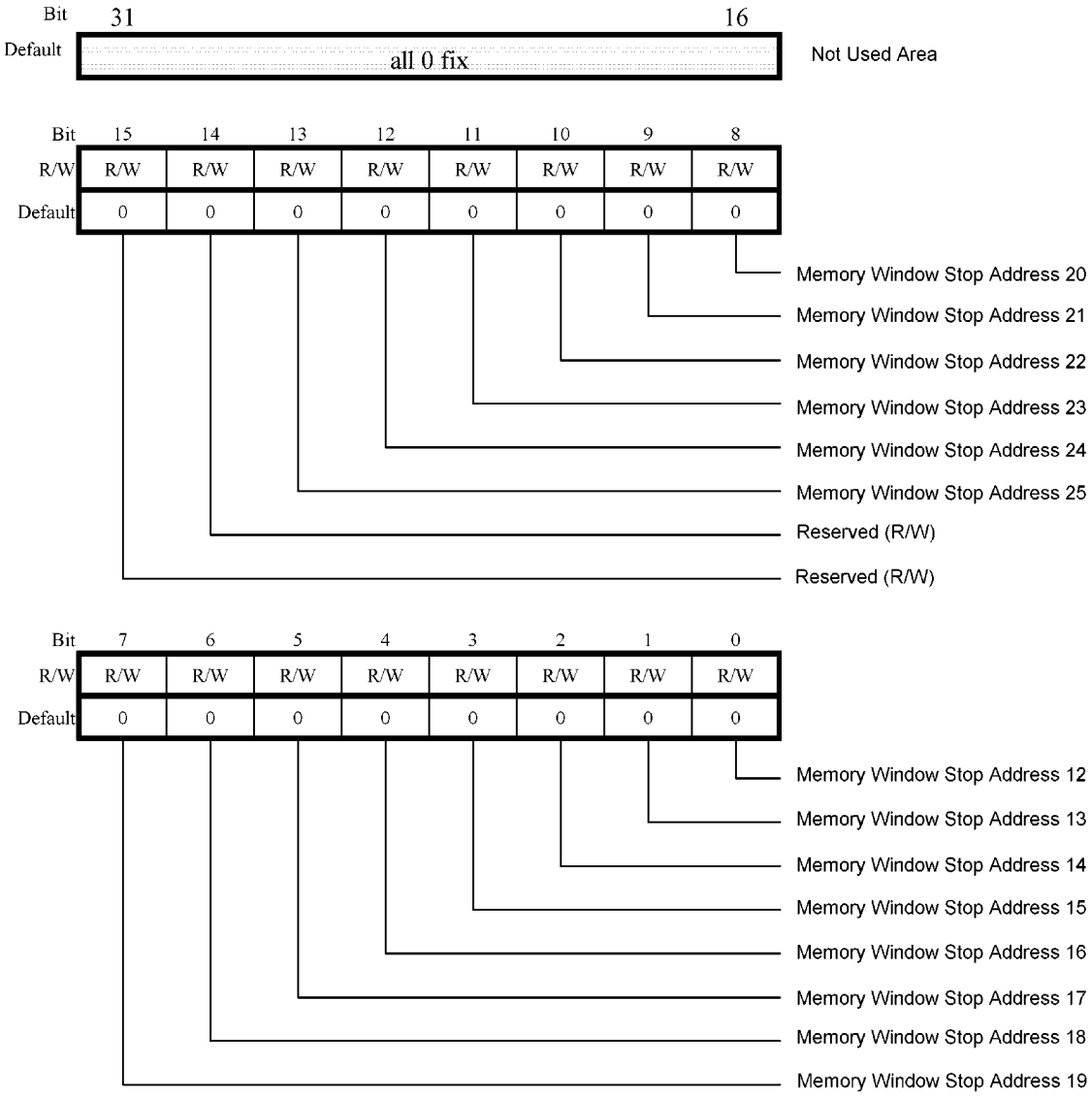
D15 to D14(Reserved)

Doing R/W can

D13 to D0(Address 25-12)

The start address of memory window n(n=0,1,2,3,4)

(12) Memory Window n Stop Address Register **Offset 044h(n=0) [UR11H]**
Offset 064h(n=1) [UR19H]
Offset 084h(n=2) [UR21H]
Offset 0A4h(n=3) [UR29H]
Offset 0C4h(n=4) [UR31H]



This register is the register to set the stop address of memory window n(n=0,1,2,3,4) .

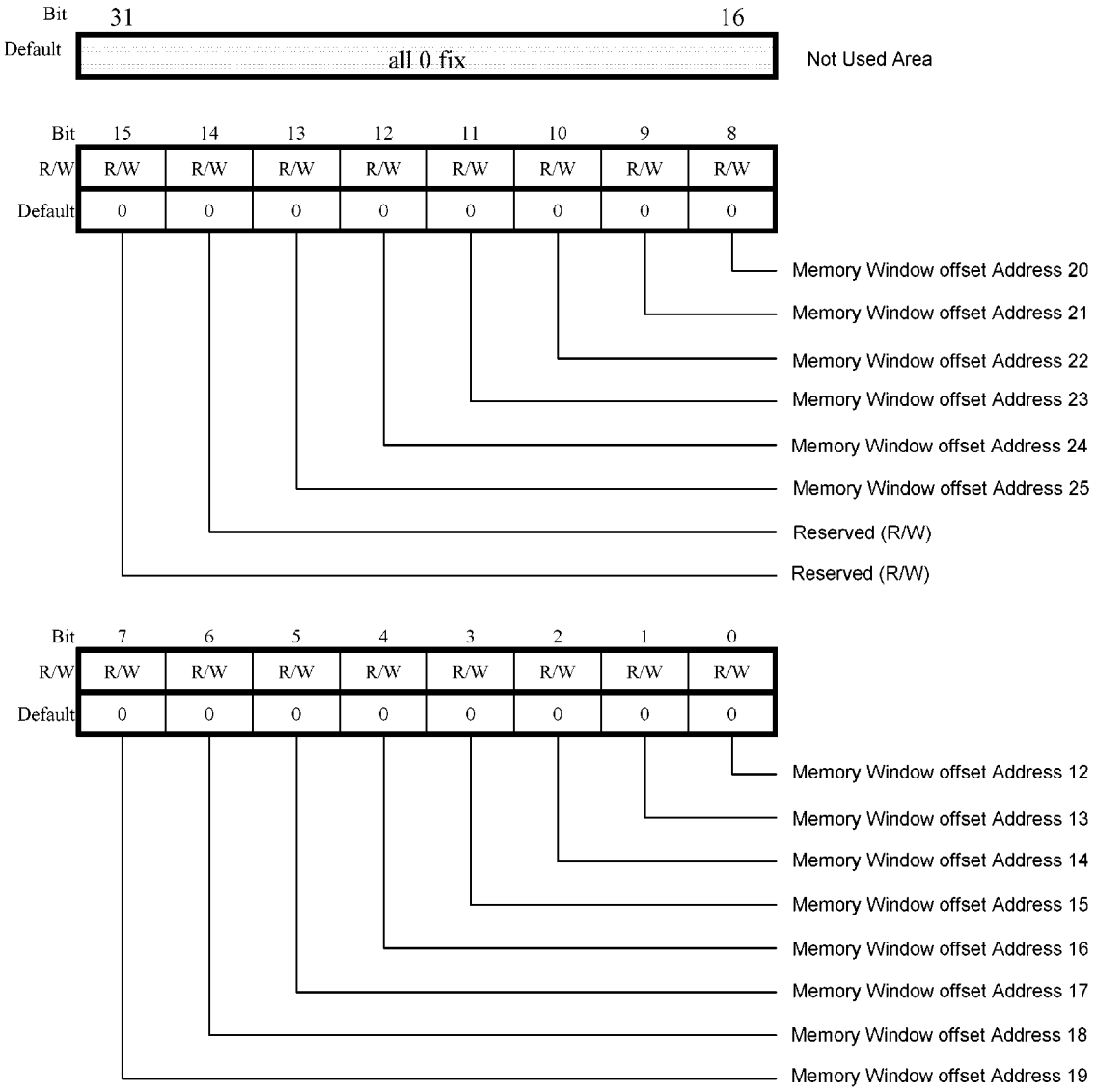
D15 to D14(Reserved)

Doing R/W can

D13 to D0(Address 25-12)

The stop address of memory window n(n=0,1,2,3,4)

(13) Memory Window n Offset Address Register **O7ffset 048h(n=0) [UR12H]**
Offset 068h(n=1) [UR1AH]
Offset 088h(n=2) [UR22H]
Offset 0A8h(n=3) [UR2AH]
Offset 0C8h(n=4) [UR32H]



This register is the register to set the offset address of memory window n(n=0,1,2,3,4) .

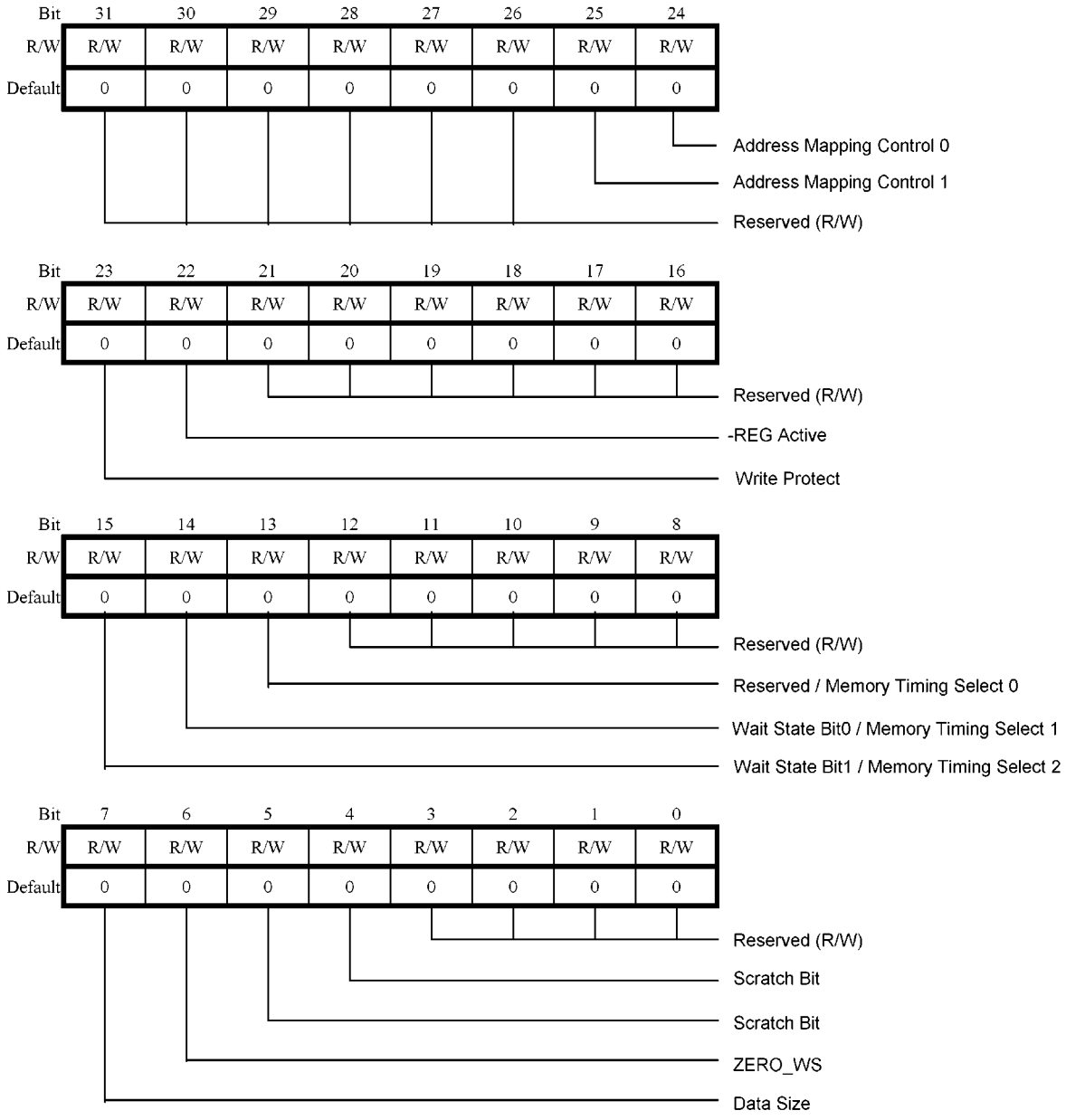
D15 to D14(Reserved)

Doing R/W can

D13 to D0(Address 25-12)

The offset address of memory window n(n=0,1,2,3,4)

(14) Memory Window n Control Register **Offset 04Ch(n=0) [UR13H]**
Offset 06Ch(n=1) [UR1BH]
Offset 08Ch(n=2) [UR23H]
Offset 0ACh(n=3) [UR2BH]
Offset 0CCh(n=4) [UR33H]



This register is the register to specify mapping function to the system space, write protect function of the memory window, common / attribute memory, timing setting, data size of the memory window and wait control.

D31 to 26(Reserved)

Doing R/W can

D25 to 24(Address Mapping Control)

It makes Memory Window n(n=0,1,2,3,4) the PCMCIA Memory/Attribute area of the system in the mapping.

Four PCMCIA Memory/Attribute areas do a mapping like the following table when there are they and they make MEM area 1, MEM area 2, MEM area 3, MEM area 4 respectively.

(On the system address There is relation of MEM area 1 < MEM area 2 < MEM area 3 < MEM area 4)

D25	D24	The area of PCMCIA Memory/Attribute
0	0	MEM area1
0	1	MEM area2
1	0	MEM area3
1	1	MEM area4

D23(Write Protect)

0 : Memory write operation via memory window n is permitted.

1 : Memory write operation via memory window n is prohibited.

Memory read operation isn't influenced by the setting of this bit.

D22(-REG Active)

0 : The access via memory window n becomes access to the common memory.
The card - REG signal become "H".

1 : The access via memory window n becomes access to the attribute memory.
The card - REG signal become "L".

D21 to D16(Reserved)

Doing R/W can

D15 to D14(Wait State Bit 1-0 / Memory Timing Select 2-1)

As for the timing, with D15-14 , it specifies Wait cycle of 16bit memory access to Memory window n .

D7	D6	Add Wait Cycle	Mode
0	0	Standard 16Bit Cycle	3 ISACLK Mode
0	1	1－Wait Cycle	4 ISACLK Mode
1	0	2－Wait Cycle	5 ISACLK Mode
1	1	3－Wait Cycle	6 ISACLK Mode

D13 to 8(Reserved)

Doing R/W can

D7(Data Size)

0 : The access to memory window n(n=0-4) becomes 8 bit access.

1 : The access to memory window n(n=0-4) becomes 16 bit access.

D6(Zero_WS)

0 : The 8 bit access to memory window n(n=0-4) by the memory becomes an average bus cycle.
(6SYSCLK mode)
Also, the 16 bit access by the memory becomes the bus cycle which is specified by D15, D14.
(3 - 6SYSCLK mode)

1 : As for 8/16 bit access to Memory window n(n=0-4), ZERO wait bus cycle becomes.
(8 bit access : 4SYSCLK mode, 16 bit access : 2SYSCLK mode)

Also, when WAIT signal is inputted from the card, even if this bit meets in "1", ZERO wait cycle doesn't occur. (WAIT signal from the card is had priority over).

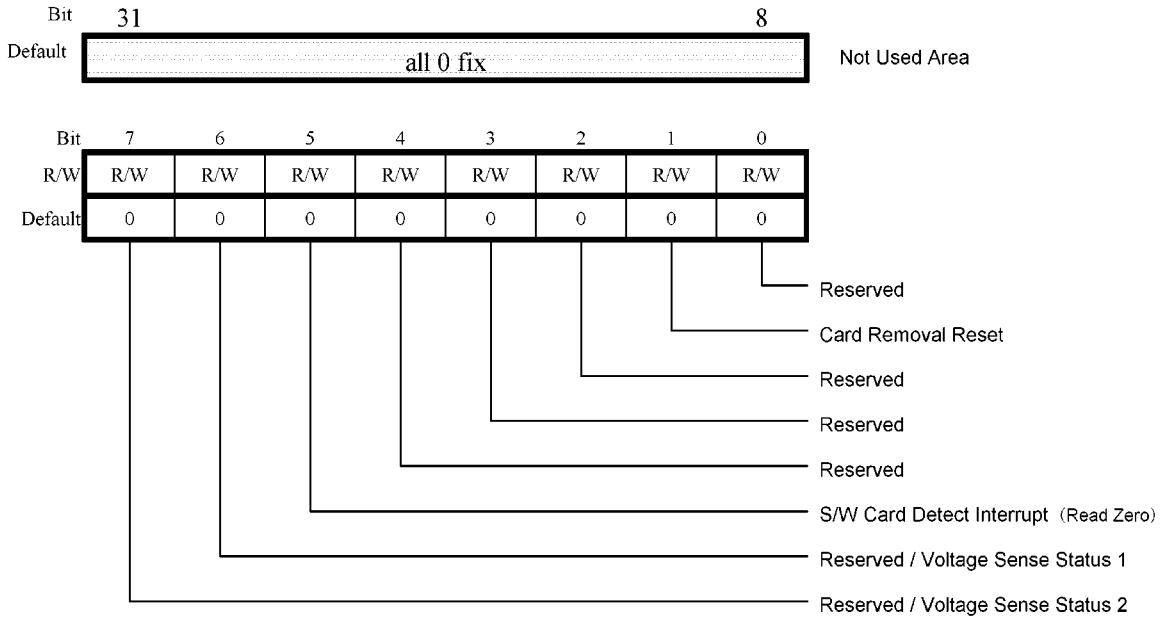
D5-D4(Reserved)

Doing R/W can.

D3-D0(Reserved)

Doing R/W can.

(15) Additional General Control Register (Offset 058h、[UR16H])



This register is the register which was added in ExCA B-STEP of Intel and does a various function control.

D7 to D6(Reserved / Voltage Sense Status)

The time of the bit 1="0" of PCMCIA Function Select Register (0F8h [UR3EH])

This bit doesn't influence operation even if it becomes the bit of Reserved and sets "1", "0". H/W, it exists as the bit which can do R/W.

The time of the bit 1="1" of PCMCIA Function Select Register (0F8h [UR3EH])

CVSx The value of the pin can be read.

The write is not in the meaning.

D5(S/W Card Detect Interrupt) - Read Zero

The time of the D3 (Card Detect Enable) ="1" (Pulling-out putting-in detection permission condition of the card) of Offset 014h[UR05H]∅ Card Status Change Interrupt Control Register

Card Status Change Interrupt occurs and is Offset when doing "1" in the write to this bit 010 h Card Status Change Register D3(Card Detect Change) becomes "1".

It is the function which pretends to have called this Software Card Detect and for there to have been pulling-out putting-in of a card according to the software.

Software Card Detect Interrupt by this bit depends on Pulling-out putting-in of the hard card Card Detect Change Interrupt Equivalent completely.

Software Card Detect Interrupt by this bit is due to the pulling-out putting-in of a hard card Card Detect Change Interrupt Equivalent completely.

This function is Offset Card Status Change Interrupt Control Register D3 of 014h[UR05H] is " At the time of 0", it isn't possible to use.(It does meaning nothing even if there is write).

Incidentally, the register bits for this bit don't exist H/W.

It writes "1" and being popular, too

It is possible to read always "0" at the time of the read.

D4 to D2(Reserved)

Doing R/W can

D1(Card Removal Reset)

1 : When a card is pulled out, all register sets by the PCMCIA card except the register which was shown in the following are Reset(Clear) by H/W Default .

This function becomes effective only in case of " that the card pulled out " from the condition, " which a card is inserted in at ". (Depending on the insertion, it doesn't happen).

Even if a card is pulled out in Suspend(While the PCMCIA clock stops), in the moment, the reset doesn't happen.

It is when the card returns from Suspend in the pulled condition that, actually, it is reset.

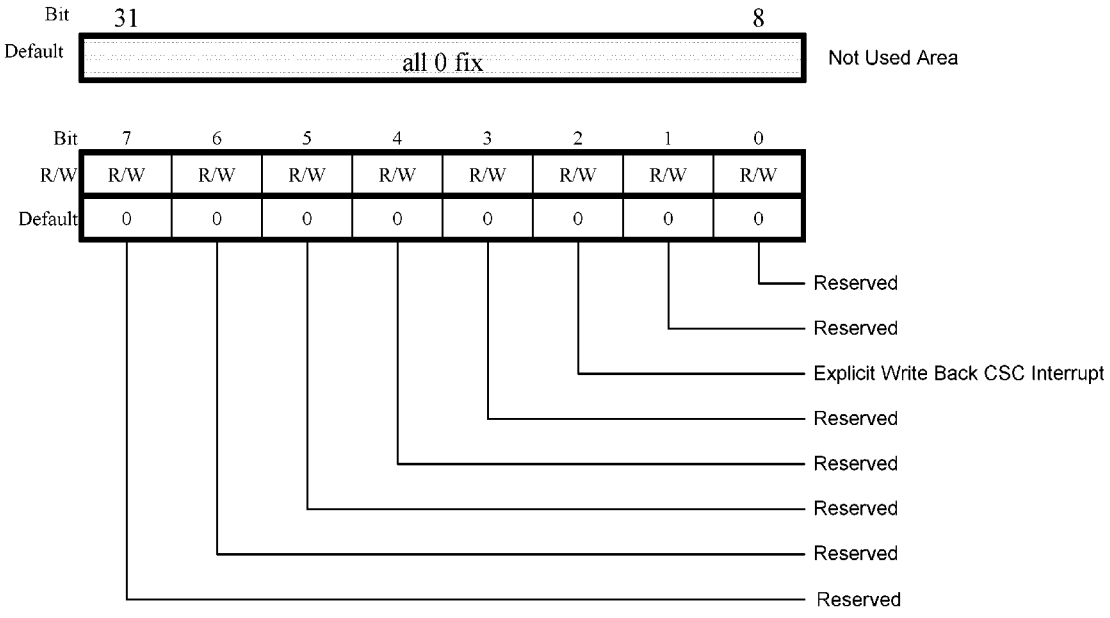
0 : As for the reset function which depends on pulling out a card, a Disable is done.

Offset 000h (Identification and Revision Register [UR00H]) ··· All bit
Offset 004h (Interface Status Register [UR01H]) ··· All bit
Offset 008h (Power Control Register [UR02H]) ··· All bit
Offset 00Ch (Interrupt and General Control Register [UR03H]) ··· D4 bit
Offset 010h (Card Status Change Register [UR04H]) ··· All bit
Offset 014h (Card Status Change Interrupt Control Register [UR05H]) ··· All bit
Offset 018h (Window Enable Register [UR06H]) ··· D5bit
Offset 058h (Additional Control Register [UR16H]) ··· All bit
Offset 078h (Global Control Register [UR1EH]) ··· All bit
Offset 0ECh (PCMCIA Card Timing Register [UR3BH]) ··· All bit
Offset 0F0h (Reserved Register [UR3CH]) ··· All bit
Offset 0F8h (PCMCIA Function Control Register [UR3EH]) ··· All bit
Offset 0FCh (Special Mode Register [UR3FH]) ··· All bit
All the bits of the equal to or more than Offset 100 h register

D0(Reserved)

Doing R/W can

(16) Global Control Register (Offset 078h、 [UR1EH])



This register, too, is the register which was added in ExcaB-STEP of Intel.
This register doesn't exist every slot and exists every slot group.
The slot group means the pair of the register which is treated as the pair like slot 1 and slot 2 in this PCMCIA Controller specification which supports more than one slot.
Because it is one(For example, it is one with slot 1 and slot 2) to the slot group in this way, even if it accesses Global Control Register of any slot, actually, it becomes access to the identical register.

D7-D3(Reserved)

Doing R/W can

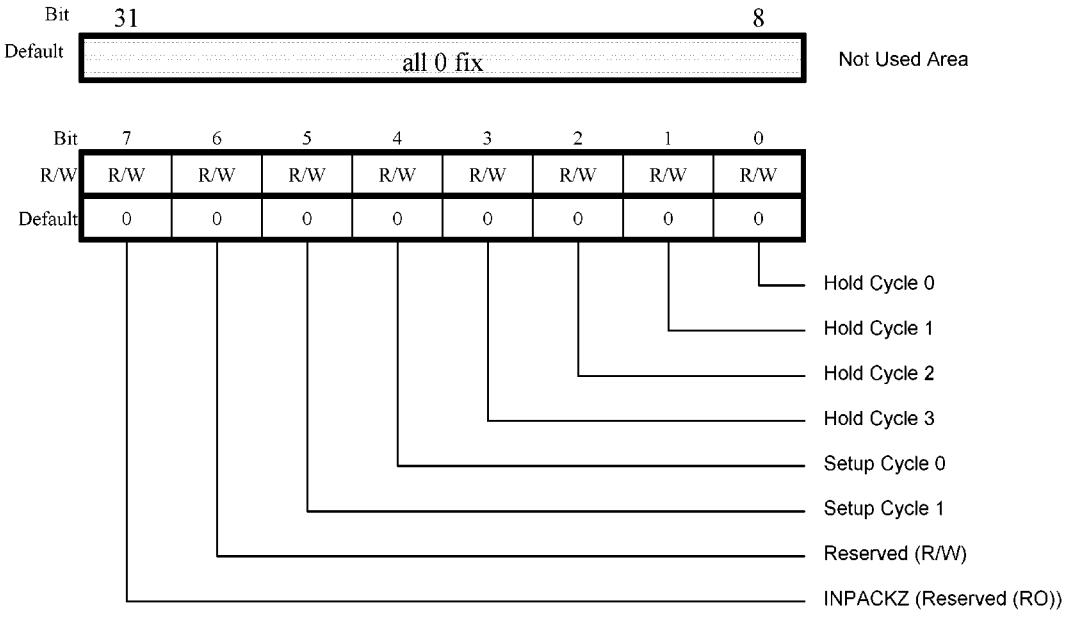
D2(Explicit Write Back CSC Interrupt)

0 : When heading Offset 010h[UR04H]Card Status Change Register , all bits that 1 stands in Card Status Change Register are cleared.
Also, Card Status Change Interrupt is canceled. (IRQn becomes inactive.)
This is for all bits to be cleared with the read in the once.
Also, in this condition, the write operation to Card Status Change Register doesn't have a meaning.

1 : By that 1 of Card Status Change Register makes "1" (It needs only to be 1 bit and more than one bit is good at the same time)a drawn bit in the write, the bit where 1 of Card Status Change Register stands is cleared. (=0)
(It needs only to be 1 bit and more than one bit is good at the same time).
In Card Status Change Register, 0 to the write operation to 0 bits and the bit where 1 stands pieces of write don't have a meaning.
Also, as for Card Status Change Register, a bit is never cleared by the Read.
Card Status Change Interrupt isn't canceled until all the bits of Card Status Change Register are cleared by the Write. (IRQn keeps an active condition)

D1-D0(Reserved) Doing R/W can

(17) PCMCIA Card Timing Register (Offset 0ECh、 [UR3BH])



The writing in this register can be written when ID_LOCK of the slot control register is "0".
At the time of "1", it isn't possible to write.
PCMCIA Function Select Register (0F8h [UR3EH]) D3 Card Timing Enable = 1
If being, the value of the register can be read.
PCMCIA Function Select Register (0F8h [UR3EH]) D3 Card Timing Enable = 0
If being, it is possible to read zero even if a value is set in the register.

D7(Reserved)

It is possible to read "1" at the time of the read. Card Timing Enable=0, it is possible to read "0".

D6(Reserved)

Doing R/W can.

D5-D4(Setup Cycle)

PCMCIA Function Select Register (0F8h [UR3EH]) D3 Card Timing Enable = "1"

If being, Wait with the value which is shown by this register is inserted during the setup cycle of the access by the card.

At the time of "0", Wait cycle isn't inserted.

Setup-Cycle="00"、"01"、"10"、"11"

Each when being Wait of 0 CLK、1 CLK、2 CLK and 3 CLK is inserted.

PCMCIA Function Select Register (0F8h [UR3EH]) D3 Card Timing Enable = "0"

When being, Wait cycle isn't inserted.

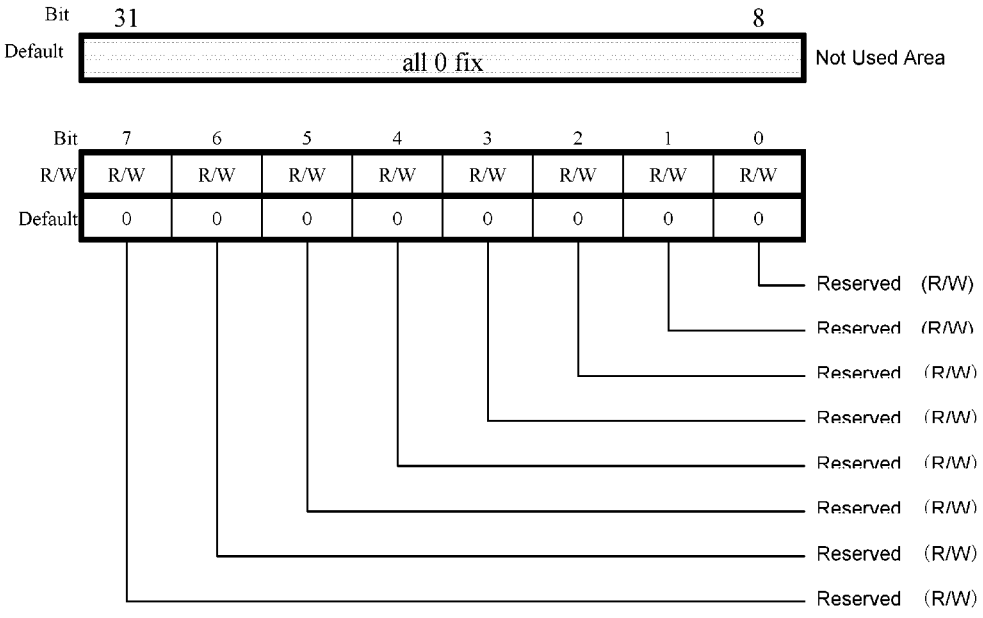
D3-D0(Hold Cycle)

If being PCMCIA Function Select Register (0F8h [UR3EH]) D3 Card Timing Enable = "1", Wait with the value which is shown by this register is inserted during the fold cycle of the access by the card. At the time of "0", Wait cycle isn't inserted.

At the time of "0001", Wait of 1CLK is inserted. At the time of "1111", Wait of 15CLK is inserted.

At the time of PCMCIA Function Select Register (0F8h [UR3EH]) D3 Card Timing Enable = 0 , Wait cycle isn't inserted.

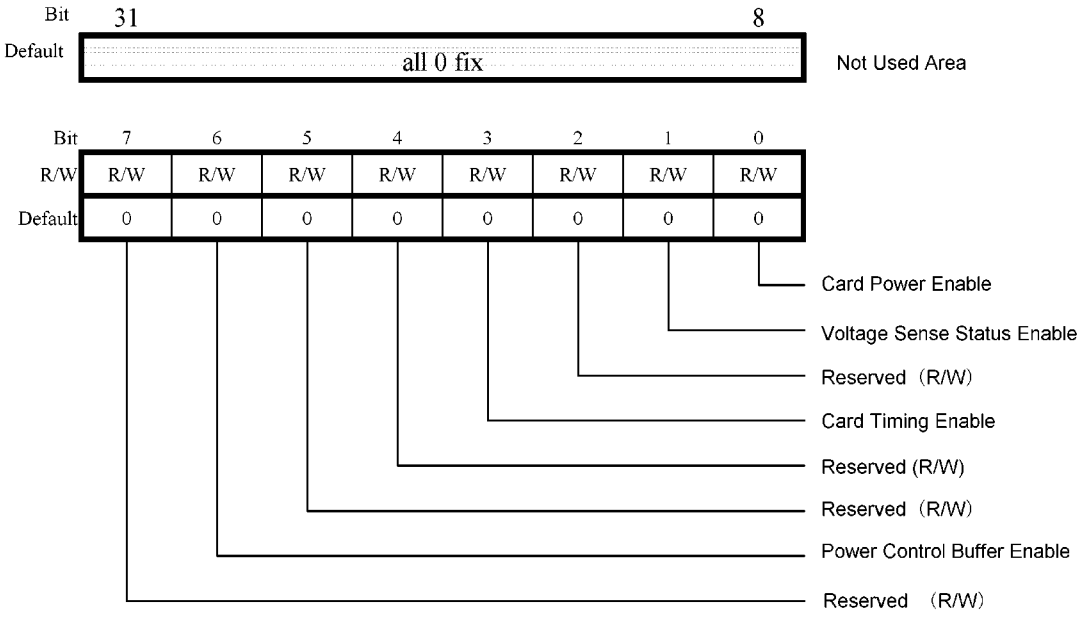
(18) Reserved Register (Offset 0F0h、[UR3CH])



D7-D0(Reserved)

Doing R/W can.

(19) PCMCIA Function Control Register (Offset 0F8h、 [UR3EH])



Slot control register (Offset 100h [HR00H]) ID_LOCK At the time of "0", the write can be done.
At the time of "1", it is not, coming in the write.
The read to this register can head zero even if a value is set in the register when ID_LOCK is "1".
When ID_LOCK is "0", the value of the register can be headed.

D7(Reserved)

Doing R/W can.

D6(Power Control Buffer Enable)

1 : When Buffer off register (Offset 104h [HR01H] 0 bit) is "1"
The RIOUT Interrupt Signal becomes "0" (Disable condition).

0 : It is not in what.

D5-D4(Reserved)

Doing R/W can.

D3(Card Timing Enable)

1 : The access timing of the card is controlled according to the setting of PCMCIA Card Timing Register. (Offset 0ECh [UR3BH])

0 : Access timing to the card isn't controlled.

D2(Reserved)

Doing R/W can.

D1(Voltage Sense Status Enable)

1 : The VSx pin condition of the card is set in D7-6 when reading Additional General Control Register (Offset 058h [UR16H]).

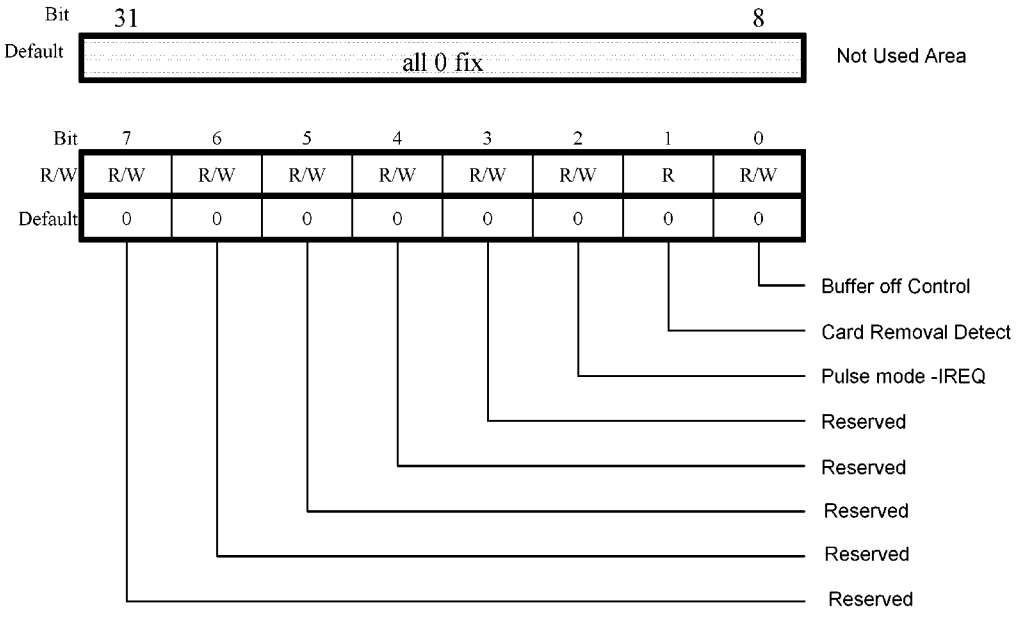
0 : Even if it reads Additional General Control Register (Offset 058h [UR16H]), it is possible to read the value of the register only.

D0(Card Power Enable)

1 : Power Control Register (Offset 008h [UR02H]) D3 is extended and can support the power of 3v.

0 : Offset 008 h support only "Vcc=5 V" .

(20) Special Mode Register (Offset 0FCh、[UR3FH])



D7-D3(Reserved)

Doing R/W can.

D2(Pulse Mode -IREQ)

It is the bit to be output - to choose the polarity of the IREQ signal from the card by the I/O Card Interface.

1: It was output from the card - it outputs IREQ signal just as it is in IRQn of the system. This means a Pulse mode Interrupt .

0: It was output from the card, - it reverses IREQ signal in the polarity and it outputs it in IRQn of the system. This means a Level mode Interrupt.

These setting has a meaning only when a - IREQ signal from the card is assigned to IRQn of the system by the I/O card interface and moreover Interrupt and General Control Register D3-D0 .

Also, it doesn't influence the fall of the Card status changing. PLUM sets '0'.

D1(Card Removal Detect)

Only this bit is the bit of the read only. This bit is set for "1" when it pulls out a card.

There are not Card Status Change Register D3 and a difference about depending and pulling out by the card about the time of usual operation.

But, in this bit, it isn't possible to do the detection of the insertion.

(It isn't possible to do processing in Suspend).

D0(Buffer off Control)

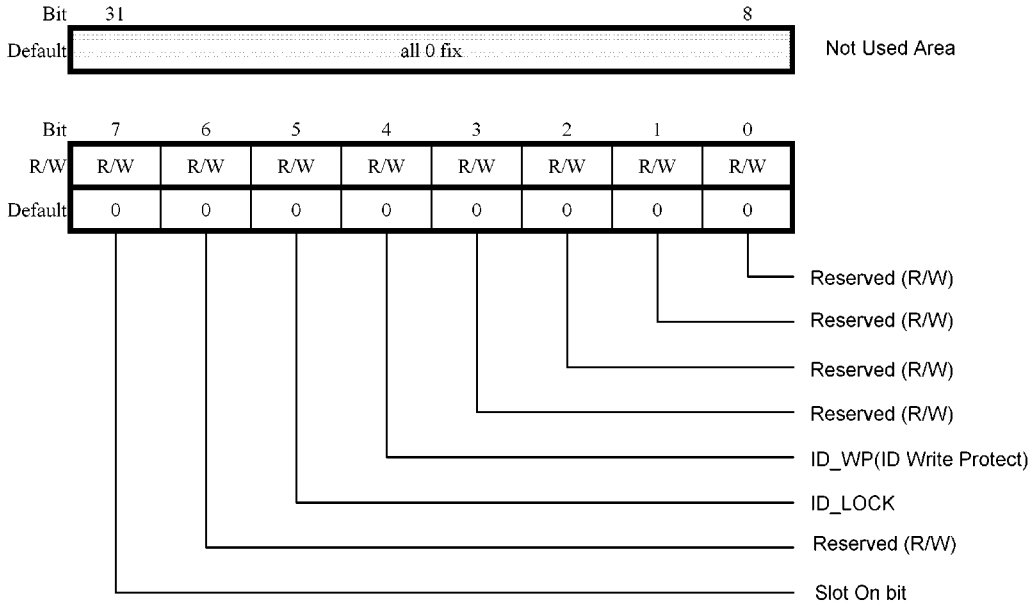
It uses this bit for the changing of an off buffer control by the BUFFOFF(Offset 104h [HR01H]).

1: An off buffer control by the BUFFOFFN signal isn't done.

0: It does an off buffer control by the BUFFOFFN signal.

(It does about the interface of the PCMCIA slot).

(21) Slot Control Register (Offset 100h、[HR00H])



D7(Slot On bit)

This bit is the enable bit of the SLOT hierarchy of PCMCIA. In reset, it becomes "0".

(PCMCIA function hierarchy)

1 : enable (Generally, it is an operation mode.)

0 : disable

It is Offset of the PCMCIA register set when making disable It doesn't reply to the access to 000h-0FCh. Also, it doesn't service a card.

HW, at the time of disable, it is Offset It is resetting the register of 000h-0FCh.

(A setting value and so on are cleared).

D6(Reserved)

Doing R/W can.

D5(ID_LOCK)

This bit is a write enable bit to Special Mode Register(Offset 0FCh). In reset, it becomes "0".

1 : LOCK(The prohibition)

0 : UNLOCK(The permission)

At the time of LOCK, PCMCIA Controller replies to the access to Special Mode Register by the write but write isn't worked to the register by it. But, at the read, it is possible regardless of this bit.

D4(ID_WP)

This bit is a writing enable bit to Indentification and Revision Register(Offset 000h) of the PCMCIA register set. In reset, it becomes "0".

1 : Write Protect

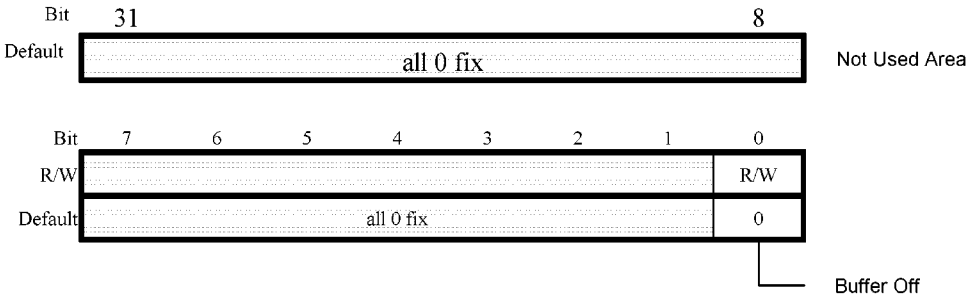
0 : Write Enable

At the time of Write Protect, writing in Indentification and Revision Register(Offset 000h) of the PCMCIA register is prohibited. But, as for PCMCIA Controller, there is to reply to the access. Also, the read, too, is possible.

D3-0(Reserved)

Doing R/W can.

(22) Buffer Off Register (Offset 104h、[HR01H])

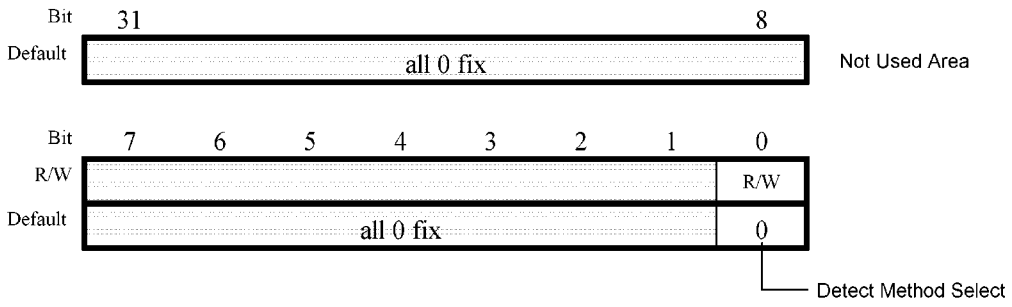


D0(Buffer Off)

1 : All the signals of the Card Interface are Buffer Off and become a Hi-Z condition.
(Offset 0FCh [UR3FH] D0 reference)

0 : Generally, it is in the condition.

(23) Card Detect Mode Register (Offset 108h、[HR02H])



D0(Detect Method Select bit)

A way of detecting a card is fixed by this bit. In reset, it is "0".

1 : The detection of the card by Software

0 : The detection of the card by Hardware

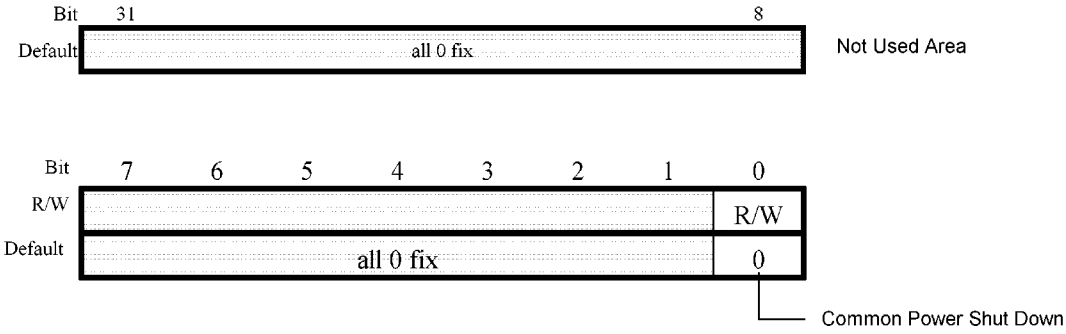
< Reference > About Detect Method Select bit

The card is inserted and when setting "1" in this bit at the time, it can realize the condition which a card was inserted (the detection) in.

But, as for the Voltage Sense signal, it doesn't have an influence.

Generally, it uses card detection by Hardware.

(24) Card Power Control Register (Slot Common) (Offset 10Ch、)



This only one register exists in PCMCIA Controller and controls both Slot in Power Shut Down.
When of Offset 10Ch accessing with each slot of PCMCIA, it becomes access to this register.

D0(Common Power Shut Down)

This bit Shut down a power, being simultaneous with 2SLOT of PCMCIA with.

1 : Power Shut down (making Vcc, Vpp of PCMCIA Card Hi-Z)

0 : Generally, it is a power.

(For the details, it refers to Offset 008.)

(25) The register of other PCMCIA Controller

00 h are headed when heading the area where the register doesn't exist.
But, 05Ch[UR17H] can always head 0fh.

5.8. SmartMedia controller

5.8.1. Features

The control function of smart media

It has a odd parity generation circuit.

5.8.2. Address mapping

The base address of the smart media

The space of MCS0 6C418000H

5.8.3. Way of accessing

(1) Access from TX3922

It uses the MCS0 space of TX3922 for the access of this SmartMedia controller.

(2) Setting of access timing

It sets the number of wait when accessing a SmartMedia wait control register.

(3) Access by the SmartMedia

It sets a power and the condition of the I/O buffer to the ON condition of the power at the power control register.

It sets an access mode at the mode setting register and it sets a SmartMedia controller to the access mode. Next, when accessing a data transfer register, the forwarding of data is done. After use of the SmartMedia controller, return to the non- access mode beforehand.

When not accessing SmartMedia, because it does the low consumption becoming of the electric power, it makes a power control register the condition of power OFF beforehand.

5.8.4. SmartMedia controller Register

(1)SSFDC data transfer register (6C418000H)

It does the transmission of the command to the SmartMedia and the sending and receiving of the address, the data.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC DATA	R/W	—	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

DATA7-0 : When accessing this register, the following forwarding is done by the mode setting.

Command mode Command (write-only)
Address mode Address
Data mode Data
Non- access mode Access Impossible

It becomes 0 with the powering reset.

(2)SSFDC mode setting register (6C418004H)

It sets a mode of the access to the SmartMedia.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC MODE	R/W	—	MODE 7	MODE 6	MODE 5	MODE 4	MODE 3	MODE 2	MODE 1	MODE 0

MODE7-0 : An access mode is set as follows.

00H non- access mode
10H data mode
11H command mode
12H address mode

It prohibits setting except the above.

After access ending to the SmartMedia, set to the non- access mode.

It becomes 00H with the power on reset.

For the details of the command mode, refer to the specification of the SmartMedia.

(3)SSFDC status register (6C418008H)

It sets a write protect to the SmartMedia. Also, the status information of the SSFDC controller is shown.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC STATUS	R/W	—	0	SMHW WP	SMSW WP	SM VT	SM RDY	0	SM CN	SM CD

SMCD : The electrical put in/pull out condition of SSFDC is shown. Read-only.
It is in the insertion condition at 0.

SMCN : The form put in/pull out condition of SSFDC is shown. Read-only.
It is in the insertion condition at 0.

SMRDY : The inner operation condition of SSFDC is shown. Read-only.
1:Ready 0:Busy

SMVT : It distinguishes between the operation voltage of inserted SSFDC. Read-only.
1:3.3V 0:5V

SMSWWP : It sets a write protect.
It becomes a write protect at 1.
It becomes 1 with the powering reset.

SMHWWP : The existence or non-existence of SSFDC's sealing up the write protect is shown. Read-only.
0:Doing seal being

For the details of the electric put in/pull out condition, the form put in/pull out condition having to do with a shape, refer to the SmartMedia and the specification of the SmartMedia slot.

(4)The SSFDC interrupt status register (6C41800CH)

It begins to read the interrupt status of SSFDC and the interrupt factor can be distinguished between. Also, the interrupt factor condition can be cleared in writing 1 in the corresponding bit.

	R/W	D31-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDCINT STATUS1	R/W	—	—	—	—	—	SMNB IN1	0	SMCN IN1	SMCD IN1

SMCDIN1 : Status change Interrupt by electric put in/pull out of SSFDC.
It becomes 1 when detecting the change of the electric put in/pull out condition of SSFDC.
The request condition can be cleared in writing 1 in this bit.

SMCNIN1 : Status change Interrupt by form put in/pull out of SSFDC.
It becomes 1 when detecting the change of the form put in/pull out condition of SSFDC.
The request condition can be cleared in writing 1 in this bit.

SMNBIN1 : The BUSY cancellation interrupt of SSFDC.
It becomes 1 when the inner operation condition of SSFDC changes into READY from BUSY.
The request condition can be cleared in writing 1 in this bit.

It becomes 0 with the power on reset.

(5)The SSFDC interrupt status register (After the mask) (6C418010H)

The interrupt status of SSFDC after the mask can be read. This status is AND of interrupt status of (5) and interrupt enable of (6).

	R/W	D31-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDCINT STATUS2	RD	—	—	—	—	—	SMNB IN2	0	SMCN IN2	SMCD IN2

SMCDIN2 : The status change Interrupt of electric put in/pull out of SSFDC.
It is in the request condition at 1.

SMCNIN2 : The status change Interrupt of form put in/pull out of SSFDC.
It is in the request condition at 1.

SMNBIN2 : The BUSY cancellation interrupt of SSFDC.
It is in the request condition at 1.

(6)SSFDC interrupt enable register (6C418014H)

It sets interrupt enable of SSFDC.

	R/W	D31-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDCINT ENABLE	R/W	—	—	—	—	—	SMNB MASK	—	SMCN MASK	SMCD MASK

SMCDMASK : It masks the status change interrupt of electric put in/pull out of SSFDC.
It permits a interrupt at 1 and it prohibits a interrupt at 0.

SMCNMASK : It masks the status change interrupt of form put in/pull out of SSFDC.
It permits a interrupt at 1 and it prohibits a interrupt at 0.

SMNBMASK : It masks the BUSY cancellation interrupt of SmartMedia.
It permits a interrupt at 1 and it prohibits a interrupt at 0.

It becomes 0 with the power on reset.

(7)The SSFDC power control register (6C418018H)

It sets a power control by SmartMedia.

	R/W	D31-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC POWER	R/W	—	SM STDN	0	0	SM BOF1	SM BOF0	SM OEEN	SM PWR2	SM PWR1

SMPWR2-1 : It sets a power control of SmartMedia.
00 : power off
01 : 5 V power on
10 : 3.3V power on
It prohibits setting except the above.

SMOEEN : It enables output to SmartMedia.
"1":enable.
"0":The output control signal to SmartMedia becomes Hi-Z.
When cutting the power off the SmartMedia, make 0.

SMBOF1-0 : It sets SmartMedia interface.
11:Generally, it is in the use condition.
It doesn't use SmartMedia interface in "X0".In this setting, all input from SmartMedia becomes piercing electric current prevention and the output to SmartMedia becomes high impedance.
It doesn't make two of SMCDZ, SMCINZ piercing electric current prevention at 01. It uses this setting when detecting put in/pull out of the card.
When cutting the power of the SmartMedia, set to 00.

SMSTDN : The shutdown setting of SmartMedia power
It is a power generally at 0.
It is power shutdown at 1.It makes the power of the SmartMedia high Impedance.

It becomes 0 with the power on reset.

(8)The SSFDC ECC control register (6C41801CH)

It sets the ECC generation circuit of SSFDC.

	R/W	D31-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC ECC CONTROL	R/W	—	—	—	—	—	—	—	ECC EN	ECC CLR

ECCCLR : It clears an ECC generation circuit.
0:clear

When using this ECC generation circuit, it makes this bit 1 immediately before data transfer beginning and transfer data. The data transfer complete and after doing a odd parity reading, until the following data transfer beginning, clear an ECC circuit beforehand.

ECCEN : This bit enables ECC generation circuit.
1:enable. 0:not use ECC generation circuit.

It becomes 0 with the power on reset.

(9)The SSFDC parity data register 1(6C418020H)

It does the reading of the line parity data of SmartMedia.

	R/W	D31-16	D15	D14	D13	D12	D11	D10	D9	D8
SSFDC ECC DATA1	RD	—	LP15	LP14	LP13	LP12	LP11	LP10	LP09	LP08

D7	D6	D5	D4	D3	D2	D1	D0
LP07	LP06	LP05	LP04	LP03	LP02	LP01	LP00

LP15-00 : The line parity data in data part 0-255 (256 bytes)

(10)The SSFDC parity data register 2(6C418024H)

It does the reading of the column parity data of SSFDC.

	R/W	D31-8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC ECC DATA2	RD	—	CP5	CP4	CP3	CP2	CP1	CP0	1	1

CP5-0 : The column parity data in data part 0-255 (256 bytes)

(11)The SSFDC parity data register 3(6C418028H)

It does the reading of the line parity data of SmartMedia.

	R/W	D31-16	D15	D14	D13	D12	D11	D10	D9	D8
SSFDC ECC DATA3	RD	—	LP15	LP14	LP13	LP12	LP11	LP10	LP09	LP08

D7	D6	D5	D4	D3	D2	D1	D0
LP07	LP06	LP05	LP04	LP03	LP02	LP01	LP00

LP15-00 : The line parity data in data part 256-511 (256 bytes)

(12)The SSFDC parity data register 6(6C41802CH)

It does the reading of the column parity data of SmartMedia.

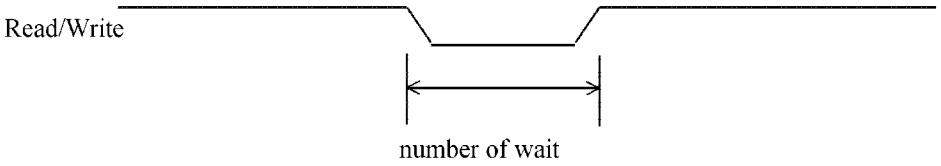
	R/W	D31- 8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC ECC DATA4	RD	—	CP5	CP4	CP3	CP2	CP1	CP0	1	1

CP5-0 : The column parity data in data part 256-511 (256 bytes)

(13)SSFDC wait control register (6C418030H)

	R/W	D31- 8	D7	D6	D5	D4	D3	D2	D1	D0
SSFDC WAIT CONTROL	R/W	—					WAIT 3	WAIT 2	WAIT 1	WAIT 0

WAIT3-0 : It sets the number of wait in access by the SmartMedia.



It becomes the length that the pulse width of Read/Write is of this bit for the setting value +1 clock.
The operation clock is the clock of the 1/2 dividing of CLKBUS.
It outputs read/write signal with length of this register for the setting value +1 clock
when the SmartMedia access.
The operation clock of the SmartMedia is 1/2 of CLKBUS.
Set for the number of wait to satisfy the AC specification of the SmartMedia.
The recommendation value is 3.

5.9. I/O bus interface

5.9.1. Features

The interface function to connect the I/O device of TX3922 and the 5 V power.
It outputs the data bus of 8/16 bits, a 11 bit address, the write signal, the read signal of it and five chip selection signals for each device.
The number of wait in case of I/O access can be set every time it selects a chip.

5.9.2. Address mapping

physical address	capacity	CS
6C415000H-6C415FFFH	4KB	It is not in CS.
6C414000H-6C414FFFH	4KB	IO5CS4
6C413000H-6C413FFFH	4KB	IO5CS3
6C412000H-6C412FFFH	4KB	IO5CS2
6C411000H-6C411FFFH	4KB	IO5CS1
6C410000H-6C410FFFH	4KB	IO5CS0

The bit 10-0 of the physical address is output by the address 10-0 of this bus.

5.9.3. Way of accessing

(1)Setting of the bus width of the I/O bus

By writing bus width in the corresponding bit of the I/O bus width setting register every time it selects a chip, the setting of 16 bits or 8 bits can be done.

(2)Setting of the number of wait

The number of wait in case of access by the I/O bus can be set by writing the number of wait in I/O bus wait control register every time it selects a chip.

(3)Access from TX3922

This I/O bus controller uses MCS0 access by TX3922.This bus is 16 bits or 8 bit access. When bigger than the bus width which the bus latitude of the access which the CPU did set, this I/O controller changes into the I/O access with more than one time.

(4)Example of the device which it is possible to connect

The keyboard controller, IDE, Super I/O, Ether

5.9.4. I/O bus controller Register

(1)I/O bus width setting register (10806000H)

It sets the I/O bus number of the bits.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
BUS SIZE CONTROL	R/W	—			IO5 BE5	IO5 BE4	IO5 BE3	IO5 BE2	IO5 BE1	IO5 BE0

IO5BE0 : It sets the data bus number of the bits in case of IO5CS0 access.
0:16 bit,1:8 bit

IO5BE1 : It sets the data bus number of the bits in case of IO5CS1 access.
0:16 bit,1:8 bit

IO5BE2 : It sets the data bus number of the bits in case of IO5CS2 access.
0:16 bit,1:8 bit

IO5BE3 : It sets the data bus number of the bits in case of IO5CS3 access.
0:16 bit,1:8 bit

IO5BE4 : It sets the data bus number of the bits in case of IO5CS4 access.
0:16 bit,1:8 bit

IO5BE5 : It sets the data bus number of the bits in case of access without CS.
0:16 bit,1:8 bit

It becomes 0 with the power on reset.

(2)I/O wait control register1(10806004H)

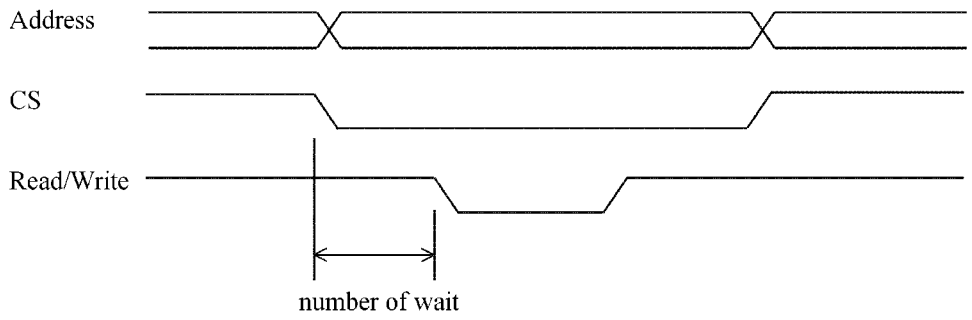
When the I/O bus accesses, the Read / Write signal actively sets the number of wait to become from the access beginning.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
WAIT CONTROL1	R/W	—						WAIT 2	WAIT 1	WAIT 0

WAIT2-0 : The setting of the number of wait that the Read / Write in access by the I/O bus become active

The length of wait is this for the setting value +1 clock.. This controller operation clock is the clock of the 1/2 dividing of CLKBUS.

It becomes 0 with the power on reset.



(3)I/O wait control register2(10806008H)

It sets the I/O access number of wait.

	R/W	D31	D30	D29	D28	D27	D26	D25	D24
WAIT CONTROL2	R/W			WAIT 29	WAIT 28	WAIT 27	WAIT 26	WAIT 25	WAIT 24

D23	D22	D21	D20	D19	D18	D17	D16
WAIT 23	WAIT 22	WAIT 13	WAIT 12	WAIT 11	WAIT 10	WAIT 9	WAIT 8

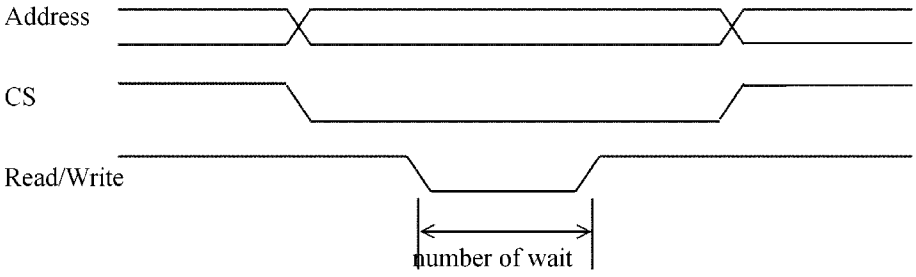
D15	D14	D13	D12	D11	D10	D9	D8
WAIT 15	WAIT 14	WAIT 13	WAIT 12	WAIT 11	WAIT 10	WAIT 9	WAIT 8

D7	D6	D5	D4	D3	D2	D1	D0
WAIT 7	WAIT 6	WAIT 5	WAIT 4	WAIT 3	WAIT 2	WAIT 1	WAIT 0

WAIT4-0 : It sets the IO5CS0 access number of wait.
WAIT9-5 : It sets the IO5CS1 access number of wait.
WAIT14-10 : It sets the IO5CS2 access number of wait.
WAIT19-15 : It sets the IO5CS3 access number of wait.
WAIT24-20 : It sets the IO5CS4 access number of wait.
WAIT29-25 : --

It sets the wait number of the access which doesn't have CS.
The length of wait is length for the setting value +1 clock.

It becomes 0 with the power on reset.



(4)I/O wait control register3(1080600CH)

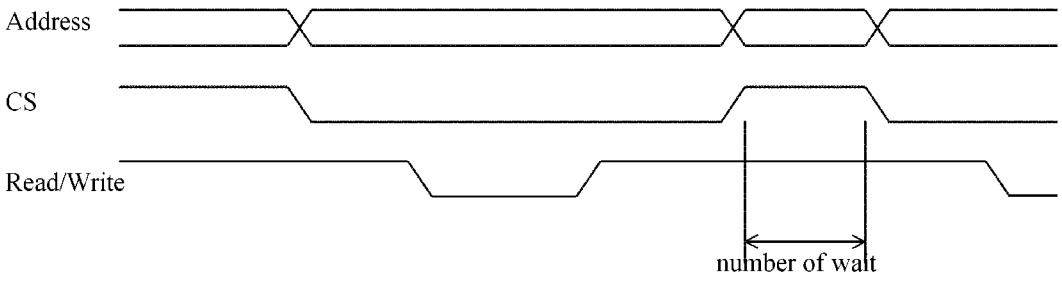
It sets the number of wait during access by the I/O bus.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
WAIT CONTROL3	R/W	—						WAIT 2	WAIT 1	WAIT 0

WAIT2-0 : It sets the number of wait during access by the I/O bus.
The length of wait is length for the setting value +1 clock.

Because the I/O bus is 16 bits or 8 bit access, the I/O bus controller changes into the 16/8 more-than-one time bit access when accessing at 32 bits from the CPU and of the 8 bit bus accessing at 16 bits from the CPU. It sets the number of Wait during access by the case.

It becomes 0 with the power on reset.



(5)IDE mode setting register (10806010H)

It sets IO bus to the IDE mode.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
IDE MODE	R/W	—								IDE MODE

IDEMODE : It makes IO5CS3, 4 IDE mode at 1.
When connecting IDE with the I/O bus, use IO8CS3, 4 and set 1 to this register.

It becomes 0 with the power on reset.

5.10. USB host controller

This section describes the USB Host Controller part for the PLUM2 chip, which is referred to as 'UHOSTC' in this section.

5.10.1. Overview

The UHOSTC supports two USB ports with per-port power switching and overcurrent detection.
It also supports power reduction by stopping its operational clock during USBSUSPEND state.
It conforms to 'Open Host Controller Interface Specification for USB,' which is referred to as 'OHCI,' and 'Universal Serial Bus Specification' Revision 1.0 and 1.1 with a few exceptions.
The exceptions are described below.
These specifications are freely available at the WWW site 'http://www.usb.org/developers/'.

5.10.2. Unique Features

5.10.2.1 Shared RAM

In OHCI, the communications memory between the Host Controller Driver and the Host Controller is defined as 'shared RAM', which resides on the system memory. In case of the PLUM2, however, the UHOSTC uses the VRAM as the shared RAM because the CPU (TX3922) provides no direct access from the UHOSTC to the system memory.

All the data structures for the communication between the driver and the UHOSTC, including Host Controller Communication Area (HCCA), End Point and Transfer Descriptor queues, Done queue, and data buffers, have to be allocated on the VRAM. It may be needed to copy data back and forth between the VRAM and a buffer acquired by a third party driver.

5.10.2.2 Shared RAM Write Buffering

In the PLUM2, the shared RAM write is buffered. After writing to the shared RAM, the software has to access any UHOSTC register before waiting for the UHOSTC interrupt.

Accessing any UHOSTC register guarantees the data buffered is written into the shared RAM.

As long as the software follows this instruction, ordering problems between the shared RAM write and the UHOSTC interrupt never occurs.

In the OHCI sample HCD code, the cases where the software writes into the shared RAM before waiting for interrupt are the functions: RemoveED, PauseED, UnscheduleIsochronousOrInterruptEndpoint. In the code, no additional remedy is needed, because the driver accesses the HcInterruptEnable register each time it waits for the interrupt.

5.10.2.3 Shared RAM Controller Clock

While the UHOSTC is operating, the shared RAM (VRAM) controller clock has to be supplied.

This clock has to be glitch-less and its frequency has to be higher than 12MHz.

If VRAM Control (PORAM) register value in the display controller is changed while the UHOSTC is operating, PLUM2 may function improperly.

To change PORAM after the UHOSTC begins operation, the software has to set USBSUSPEND to HCFS field of the HcControl register and wait for 1.2 ms.

The software also has to avoid accessing the shared RAM until PORAM is set to the operational value.

5.10.2.4 Initialization Period

The UHOSTC requires 4us with active clock input to complete initialization after power-on reset.

Accessing the UHOSTC has to wait for this period after enabling USB clock. This is required only after power-on reset.

5.10.2.5 Interrupt

The UHOSTC issues two interrupt requests.

- USBINT : Interrupt as the communication method for HC-initiated communication with the HCD
- USBWAKE : Interrupt as the request for restarting the clocks

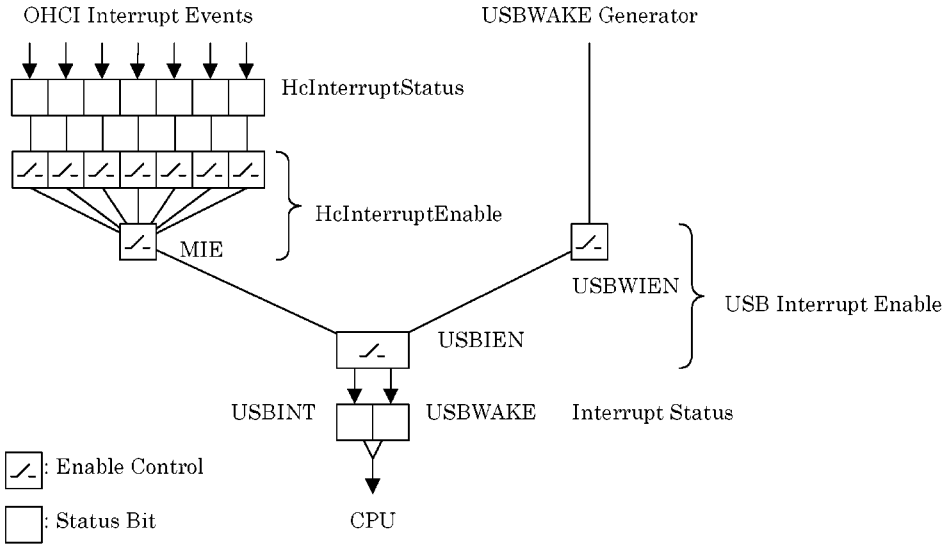
Each of these interrupts has its status bit in the interrupt status register of the PLUM2 and enabled or disabled. through multiple levels of enable controls (Figure 1).

Note that HcInterruptStatus and HcInterruptEnable registers are in the OHCI register space, while USB Interrupt Enable and Interrupt Status registers are in the Interrupt. Controller register space.

Refer to the Controller description for details of the interrupt status and USB interrupt enable registers.

Refer to OHCI specification for details of USBINT. Refer to Sections 5.10.3 and 5.10.5 for details of the USBWAKE usage.

Figure 1 Interrupt Enable Control



5.10.2.6 External Pin Power-Down Mode

When the external power switch IC is powered down, bit 10 of power control register has to be reset to '0'. This makes USBPWR1/2* output signals to ground level. Note that this means 'Port Power On' regardless of overcurrent detection. Therefore the system should guarantee the power switch IC is powered off whenever this bit is '0'.

Resetting this bit to '0' also simulates USB signals inside PLUM2 to be SE0 so that the host controller recognizes as if the ports were disconnected.

5.10.2.7 Reset Operation

UHOSTC reset operation is allowed only when the UHOSTC is not accessing the shared RAM.

To guarantee this condition, the software has to set USBSUSPEND to HCFS field of the HcControl register and wait for 1.2 ms before resetting the UHOSTC.

The reset operations include setting USBRESET to HCFS field of the HcControl register and setting HCR bit in the HcCommandStatus register.

5.10.2.8 Legacy Support

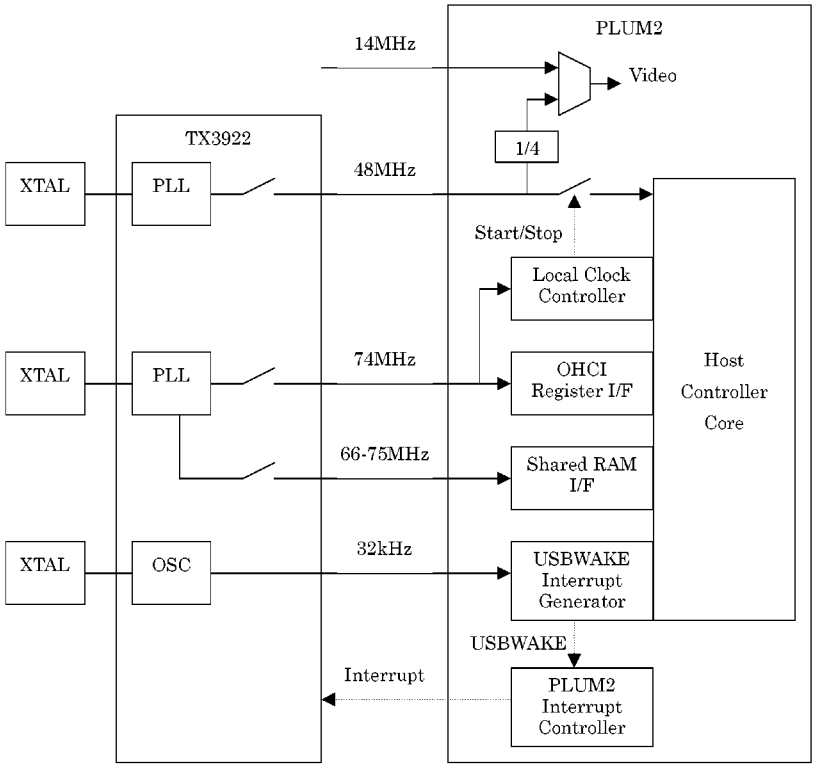
The UHOSTC contains no legacy support circuitry, because legacy support is applicable only to the IBM-PC compatible platform.

5.10.3. Clock Control

5.10.3.1 Overview

The USB core clock (48MHz)origins from a crystal and a PLL in the CPU (TX3922) and flows through clock gates in both the CPU and the PLUM2. The UHOSTC also utilizes bus clock, memory clock, and RTC clock(32kHz). Figure 2 shows clock usage and control for UHOSTC.

Figure 2 Clock usage and control



The UHOSTC's USBWAKE interrupt generator supports interrupt-based, fully software-controlled clock-stopping/restarting .

The UHOSTC's local clock controller supports fully hardware-controlled inside-PLUM2-only clock-stopping/restarting .

These functions enable users to reduce power consumption while the Host Controller Core is in USBSUSPEND state.

Note that USBOPERATIONAL and USBSUSPEND do not necessarily correspond to Windows CE's active and idle state. For example, if no USB device is connected, the UHOSTC may be in USBSUSPEND while Windows CE is in active state.

5.10.3.2 Clock Control by USBWAKE Interrupt

In case of stopping/restarting the 48MHz clocks in the CPU, clock control must be done through USBWAKE interrupt. In this scheme, the clock condition must be under full control of the software.
To obtain proper USB operation, the software must follow the instructions below. Refer to the TX3922's manual for details of controlling the CPU's 48MHz clock outputs.

5.10.3.2.1 Clock Stop

After the software moved the UHOSTC into USBSUSPEND state, the software has to wait for 5ms or longer before stopping the 48MHz clock output from the CPU.
If the software does not follow this, the UHOSTC will not respond properly to events on its ports.

While the 48MHz clock is stopped, accessing UHOSTC's registers causes the system to hang up, so the software has to guarantee the clock is provided to the UHOSTC when the UHOSTC is accessed.

To handle the wakeup event properly, the software has to enable the USBWAKE interrupt by setting USBWIEN bit no later than 28us after disabling the OHCI interrupt (USBINT) or stopping the 48MHz clock.

5.10.3.2.2 Clock Restart

While the 48MHz clock output from the CPU is stopped during USBSUSPEND state, the USBWAKE interrupt generator can detect a wakeup event on the root hub's ports. The interrupt generator responds to the event, if necessary, and requests the CPU to restart the clock by USBWAKE interrupt, if it is enabled. When the software receives the USBWAKE interrupt, the software has to restart the clock, wait at least 2us, and disable the USBWAKE interrupt before the software moves the UHOSTC into USBOPERATIONAL. If the USBWAKE is disabled too early, the UHOSTC may function improperly. If USBWAKE interrupt remains enabled in USBOPERATIONAL state, the UHOSTC will drive improper signaling to its USB ports.

In case the software stopped the oscillator or PLL in the CPU during USBSUSPEND, the software has to first restart the oscillator and PLL and wait for sufficient time for the clock to become stable before enabling the clock outputs and accessing the UHOSTC.

5.10.3.3 Local Clock Control

In case of stopping/restarting the host controller core clock inside PLUM2, clock control can be automatically done by hardware. The hardware behaves as if the clock were not stopped or restarted. Note that in this case the external 48MHz clock or the internal system and memory clocks can not be stopped. Refer to the PLUM2's manual for details of controlling PLUM2's internal clocks.

5.10.3.3.1 Clock Stop

When the UHOSTC remains in USBSUSPEND state for 5ms, the local clock controller automatically stops the host controller core clock.

5.10.3.3.2 Clock Restart

While the host controller core clock is stopped, accessing UHOSTC's registers causes the local clock controller to restart the clock, so the software does not need to be aware of the clock condition when it accesses the UHOSTC.

While the host controller core clock is stopped during USBSUSPEND state, the local clock controller can detect a wakeup event on the root hub's ports and restart the clock automatically.
The host controller core responds the event, if necessary.

5.10.4. Functions and Registers

The UHOSTC fully supports the OHCI functions and registers as defined in OHCI. This section describes how the implementation-specific portions of OHCI are implemented in the UHOSTC. This section also clarifies register bit reset status.

Changed or added descriptions are underlined so you can easily notice them. Register bits not mentioned in this section are implemented in accordance with OHCI.

5.10.4.1 HcControl Register

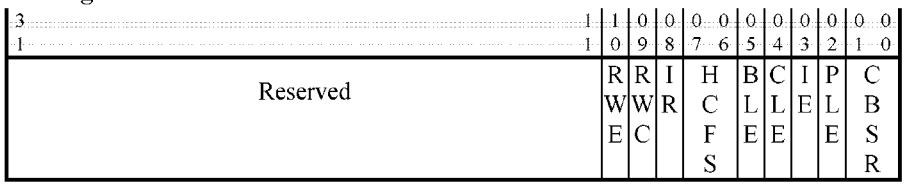


Figure 3: HcControl Register

Key	Reset	Read/Write		Description
		HCD	HC	
HCFS	00b	R/W	R/W	**HostControllerFunctionalState for USB** 00b: USBRESET 01b: USBRESUME 10b: USBOPERATIONAL 11b: USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of *HcInterruptStatus*. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports. After setting HCFS into UsbSuspend, HCD must wait for at least 5ms before stopping USB clock..
IR	0b	R/W	R	**InterruptRouting** This bit determines the routing of interrupts generated by events registered in *HcInterruptStatus*. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC. The UHOSTC does not utilize System Management Interrupt, so do not set this bit.

5.10.4.2 HcRhDescriporA Register

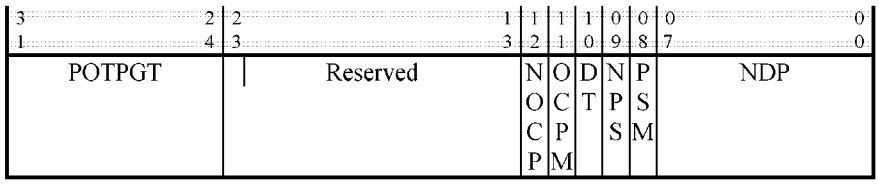


Figure 4 : *HcRhDescriptorA* Register

Field	Power On Reset	Read/Write		Description
		HCD	HC	
NDP	2	R	R	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15.
NPS	0	R/W	R	**NoPowerSwitching** These bits are used to specify whether power switching is supported or port are always powered. It is implementation- specific. When this bit is cleared, the **PowerSwitchingMode** specifies global or per-port switching. 0: Ports are power switched 1: Ports are always powered on when the HC is powered on
PSM	1	R/W	R	**PowerSwitchingMode** This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the **NoPowerSwitching** field is cleared. 0: all ports are powered at the same time. 1: each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the **PortPowerControlMask** bit is set, the port responds only to port power commands (**Set/ClearPortPower**). If the port mask is cleared, then the port is controlled only by the global power switch (**Set/ClearGlobalPower**).
OCPM	1	R/W	R	**OverCurrentProtectionMode** This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, this fields should reflect the same mode as **PowerSwitchingMode**. This field is valid only if the **NoOverCurrentProtection** field is cleared. 0: over-current status is reported collectively for all downstream ports 1: over-current status is reported on a per-port basis
NOCP	0	R/W	R	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the **OverCurrentProtectionMode** field specifies global or per-port reporting. 0: Over-current status is reported collectively for all downstream ports 1: No overcurrent protection supported
POTPGT	8	R/W	R	**PowerOnToPowerGoodTime** This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as **POTPGT** * 2 ms.

5.10.4.3 HcRhDescriporB Register

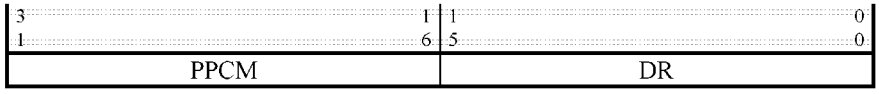


Figure 5 : *HcRhDescriptorB* Register

Field	Power-On Reset	Read/Write		Description
		HCD	HC	
DR	0	R/W	R	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit15: Device attached to Port #15
PPCM	bit1:1 bit2:1	R/W	R	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when **PowerSwitchingMode** is set. When set, the port's power state is only affected by per-port power control (**Set/ClearPortPower**). When cleared, the port is controlled by the global power switch (**Set/ClearGlobalPower**). If the device is configured to global switching mode (**PowerSwitchingMode**=0), this field is not valid. Bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit15: Ganged-power mask on Port #15

5.10.5. USBWAKE Interrupt Implementation

5.10.5.1 USBWAKE Interrupt Generator

This module detects USB events which must be responded by the UHOSTC: remote wakeup, connect, disconnect, and overcurrent.

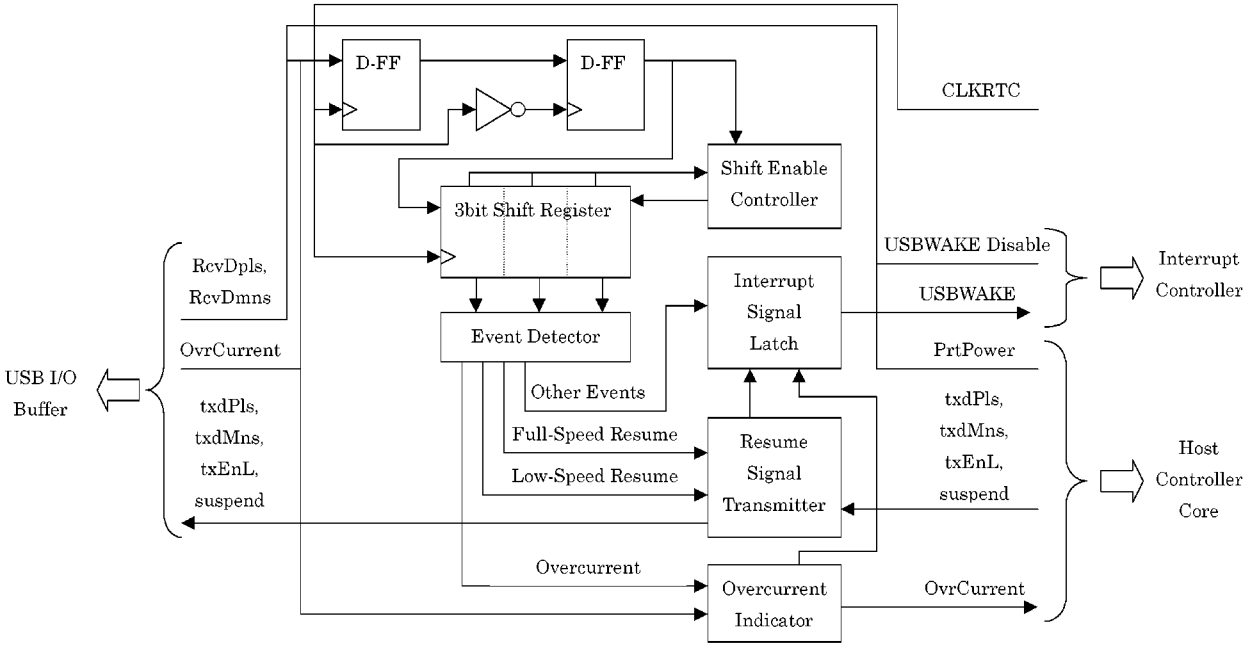
Functions of this module are:

- Driven by CLKRTC (32kHz)
- Watches single-ended Dplus, single-ended Dminus, and overcurrent signals from the USB I/O buffer
- Detects overcurrent, full- and low-speed resume, full- and low-speed device connect, and device disconnect
- Issues interrupt signal by latching the detection flag while the interrupt is enabled
- Sends resume signaling, if the event is remote wakeup, to the originating device while USBWAKE interrupt is active
- Latches overcurrent signal while USBWAKE interrupt is active

This module consists of the elements below (Figure 6).

- Input-synchronizing flip-flops
- Three bit shift register(signal state memory)
- Shift enable control
- Event detector logic
- Interrupt signal latch
- Resume signal transmitter
- Overcurrent indicator

Figure 6 Block Diagram of USBWAKE Interrupt Generator



5.10.5.2 Sample Sequence

This section describes a sample of USB clock stop/restart sequence. The software is not required to implement this sequence but it must satisfy the requirements described in section 5.10.3

5.10.5.2.1 Clock Stop Sequence

A routine called `USBClockStop' stops the USB clock.

Software Module	*Action*
USBD and HCD	Write USBSUSPEND into HCFS bits in RhControl. Set RD bit in RhInterruptEnable. Schedule the invocation of USBClockStop after 5ms.
(other)	(5ms)
USBClockStop	Disable CPU interrupt. Check if HCFS bits still remain in USBSUSPEND. If not, enable CPU interrupt and exit. Write `1' into MIE bit in RhInterruptDisable to disable the UHOSTC interrupt. Stop the USB clock. Enable USBWAKE. Enable CPU interrupt.

5.10.5.2.2 Clock Restart Sequence

USBWAKE interrupt handler restarts the USB clock. In case of remote wakeup, after the clock restarts, the UHOSTC will issue `Resume Detected' interrupt, which enables the software to move the UHOSTC into USBOPERATIONAL.

The USB driver must execute itself the same sequence if it wants to access the UHOSTC while the USB clock is stopped.

Software Module	*Action*
USBWAKE handler Or USBD and HCD	Restart the USB clock. (wait until the clock become stable, if necessary.) Wait for 2us. Disable USBWAKE (by USBWAKE handler only). Write `1' into MIE bit in RhInterruptEnable to enable the UHOSTC interrupt.

5.10.5.2.3 Operation in the Critical Case

If a remote wakeup event happens just a little before the clock is stopped, the host controller core may or may not detect and respond to the event, because the core requires about 2us to do this. In either case, the event will be properly detected and the clock will be restarted properly, as long as the software follows the restriction.

In case the core could detect and respond before the clock stops, the core sets `Resume Detected' interrupt status, which is masked by MIE. The event detector will detect the event and issue USBWAKE interrupt after 2.5 CLKRTC clocks or later, at which time USBWAKE will have been enabled by the USBClockStop routine. The USBWAKE interrupt invokes the handler, which restarts the clock, and enables MIE. This enables the pending `Resume Detected' USBINT.

In case the core could not detect and respond the remote wakeup before the clock stops, the event detector will detect the event, reflect resume signaling, and issue USBWAKE interrupt after 2.5 CLKRTC clocks or later, at which time USBWAKE will have been enabled by the USBClockStop routine. The USBWAKE interrupt invokes the handler, which restarts the clock. The host controller core will detect the resume signaling driven by the event detector and reflect the signal by itself within 2us, which is before the USBWAKE is disabled by the software.

5.10.5.3 Difference from USB Specification

The event detector reflects resume signaling only to the signaled port within 92us after the remote wakeup. The other enabled ports will be resume-signaled when the interrupt handler restarts the UHOSTC core clock; perhaps after dozens of milliseconds. This does not conform to the USB Specification Revision 1.0, which requires a suspended hub to reflect resume signaling to the signaled port and the other enabled ports less than 50us after the wakeup. In the USB Specification Revision 1.1, however, maximum allowed delay is 100us.

5.11. Power controller

5.11.1. Features

The oscillation, the stop control of the clock

The output of the ON/OFF control signal of the power of various I/O

5.11.2. Power management signal

(1)Power of various I/O

In the power control part of Plum2, it outputs the power of the LCD panel, the power of the I/O bus, power control signals for the other external device.

The value or the turning-over signal to have set to the corresponding bit of the power control register is output outside.

The software control so as not for electric power to be wastefully consumed by cutting an unnecessary power.

5.11.3. Power controller Register

(1)Power control register (10807000H)

It sets the condition of the power control signal of each I/O.

	R/W	D32-16	D15	D14	D13	D12	D11	D10	D9	D8
POWER CONTROL	R/W	—	—	—	—	—	—	USB EN	IO5 OE	LCD OE

D7	D6	D5	D4	D3	D2	D1	D0
D7	EXT PW2	EXT PW1	EXT PW0	IO5 PWR	BKL IGHT	LCD PWR	LCD DSP

LCDDSP : The ON/OFF control of the display of LCD. It is display ON at 1.
A setting value is output by LCDDSP.

LCDPWR : The ON/OFF control of the power of LCD. It is power ON at 1.
The reverse of the setting value is output by LCDOFFZ.

BKLIGHT : The ON/OFF control of the back light of LCD. It is back light ON at 1.
The reverse of the setting value is output by BKLOFFZ.

IO5PWR : The ON/OFF control of the power of the module which is connected with the I/O bus.
A setting value is output by IO5PWR.

EXTPW2-0 : The various power for I/O or the control signal for clock enable.
A setting value is output by PWRCNT2-0.
As for the use of this control signal, refer to the board specification.

D7 : Reserved. It is possible to read a written value.

LCDEN : The enable control of the output signal to the LCD panel
It makes output to the LCD panel enable at 1.The output to the LCD panel becomes L at 0.

IO5OE : Enable control of the I/O bus
It makes I/O bus enable at 1.The output to the I/O bus becomes L at 0 and the input from the I/O bus becomes piercing electric current prevention.

USBEN : The output enable signal of the USB controller.
1 : Enable
0 : The output signal(USBPWR) of the USB controller becomes "0".
It becomes 0 with the power on reset.

When cutting the power of I/O which is connected with Plum2, it accesses this register and make IO5OE “0” and make IO5PWR “0”.When switching over to suspend mode, the software access this register before the mode switches over and OFF an unnecessary power beforehand. Incidentally, it controls a power with the power control register which is had by each controller about the PCMCIA controller, the SmartMedia controller.

(2)Clock control register (10807004H)

It sets the supply / stop of the clock of each module.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
CLOCK CONTROL	R/W	—			USB CLK2	USB CLK1	IO5 CLK	SM CLK	PCC CLK2	PCC CLK1

PCCCLK1 : It controls the supply / stop of the clock to PCMCIA controller 1.
1:Supply,0:Stop

PCCCLK2 : It controls the supply / stop of the clock to PCMCIA controller 2.
1:Supply,0:Stop

SMCLK : It controls the supply / stop of the clock to SmartMedia controller.
1:Supply,0:Stop

IO5CLK : It controls with the hardware in the clock supply to the I/O bus controller at 0.
It doesn't control in the clock supply to I/O bus controller at 1.
It always supplies a clock to the I/O bus controller at 1.

USBCLK1 : Controls the supply / stop of the clock to the USB host controller.
1:USBCLK2 is effective
0:Stop

USBCLK2 : Forces clock supply to the USB host controller.
1: Clock is always supplied while USBCLK1=1.
0: Clock supply is adaptively controlled by hardware while USBCLK1=1.

When using USB, set USBCLK1 to 1 and optionally set USBCLK2 to 1 to disable adaptive control. Setting USBCLK1=1 and USBCLK2=0 is recommended.

It becomes 0 with the power on reset.

(3)Mask ROM control register (10807008H)

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
MROM_ADD CONTROL	R/W	—						MRPM SL1	MROM SL0	MRMA EN

MRMAEN : Control signal of the address output by the mask ROM

At 0, only as for the access to the mask ROM, it outputs an address in the mask ROM interface. As for the access except the mask ROM, it makes the address of the mask ROM interface oar 0.

It outputs an address in the mask ROM interface to all access at 1.

It sets this bit to "1" when using the debugging board which connects with the mask ROM interface. By this, as for the access except the mask ROM, too, an address is output by the mask ROM interface and the debugging board becomes able to be used. Because it doesn't use a debugging board at the fruit machine, because it does the low consumption becoming of the electric power, so as not for the address to change, set this bit to 0 except the access by the mask ROM.

MROMSL1 - 0 : It sets the capacity of the 1 chip selection by the mask ROM.

0 0 : 8MB

0 1 : 4MB

1 X : 16MB

It becomes 0 with the power on reset.

(4)Input signal enable register (1080700CH)

It sets each input signal to enable.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
INPUT_SIG ENABLE	R/W	—								RMCS EN

RMCSEN : It makes the input signal of the MCS interface from TX3922 enable.

1:enable

It becomes 0 with the power on reset.

PLUM2 is using MCS area in case of address mapping by TX3922 for the I/O access from TX3922.In to set "1" to the corresponding bit of this register, it becomes accessible from the MCS area After setting the MCS interface of TX3922, write "1" in this bit and make the MCS interface of PLUM enable.

(5)Reset control register (10807010H)

It sets the condition of the reset signal of each I/O.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
RESET CONTROL	R/W	—							IO5 CL1	IO5 CL0

IO5CL1-0 : Clear signal for the device which connects with the I/O bus
0:clear
The setting value of IO5CL0 is output to IO5CLRL.
The turning-over value of IO5CL1 is output to IO5CLRH.

It becomes 0 with the power on reset.

5.12. Interrupt controller

5.12.1. Features

The Interrupt output to the distinction function and TX3922 of the Interrupt factor signal From each function block in Plum2.

The latch and the Interrupt mask function of the Interrupt factor signal from the outside input.

5.12.2. Interrupt factor distinction

The interrupt factor which the book interrupt controller handles is shown next.

(1) **Display controller interrupt**

The interrupt from LCD / the CRT Controller.

(2) **PC card controller interrupt**

The interrupt from the PCMCIA controller.

(3) **SmartMedia controller interrupt**

The interrupt from the SmartMedia controller.

(4) **USB host controller interrupt**

The interrupt from the USB host controller.

(5) **Outside input interrupt**

The interrupt which is inputted to Plum2 from outside.

It inputs the interrupt of the device which is connected with the I/O bus, and so on.

The interrupt controller has a interrupt from which block it is or a distinction function. Moreover, to distinguish between the details of the interrupt, read interrupt status in the corresponding block. As for the for each interrupt detailed specification of the display controller, the PC card controller, the SmartMedia controller, refer to the explanation in each block. An outline about the outside input interrupt is shown in the following clause and a register specification is shown in 14.5.

5.12.3. Interrupt from the outside input

A interrupt from the outside that Plum2 handles is shown next.

- I/O bus interrupt

  Four interrupts from the device which is connected with the I/O bus (5 V input)
- Spare is Two (3 V input)

As for above-mentioned interrupt factor, it has the latch and the clear function and the interrupt mask function of the factor. It outputs to the interrupt factor distinction circuit which was shown in 5.11.2 as one outside input interrupt signal by gathering these interrupts.

5.12.4. Interrupt controller Register

（1） interrupt status register (10808000H)

It reads interrupt status in each block and then the block which the interrupt occurred to can be distinguished between.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
INT STATUS	RD	—	EXT INT	SM INT	USB WAKE	USB INT	DISP INT	C2SC INT	C1SC INT	PCC INT

PCCINT : I/O or RI Interrupt from the PCMCIA controller.
1:request condition
For the details of this interrupt, refer to the register and the PCMCIA Controller for Plum2 register specification which is shown in the (6)(7)(8)(9) clause.

C1SCINT : Status changing interrupt from PCMCIA controller 1.
1:request condition
For the details of this interrupt, refer to the PCMCIA Controller for Plum2 register specification.

C2SCINT : Status changing interrupt from PCMCIA controller 2
1:request condition
For the details of this interrupt, refer to the PCMCIA Controller for Plum2 register specification.

DISPINT : Interrupt from LCD / the CRT Controller.
1:request condition
For the details of this interrupt, refer to the Display Controller for Plum Specification.

USBINT : interrupt from the USB host controller
1:request condition
For the details of this interrupt, refer to the USB Host Controller Specification

USBWAKE : USB controller clock resumption request interrupt.
1:request condition
For the details of this interrupt, refer to the USB Host Controller Specification.

SMINT : interrupt from the SmartMedia controller
1:request condition
For the details of this interrupt, refer to the 14.6.

EXTINT : interrupt from the outside input
1:request condition
For the details of this interrupt, refer to the (3),(4),(5)

(2) Interrupt enable register (10808010H)

It makes a interrupt into TX3922 enable.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
INTEN	R/W	—								INT IEN

INTIEN : It sets interrupt enable to TX3922.
It permits a interrupt at 1. It prohibits a interrupt at 0.
It uses this bit when masking a interrupt temporarily in case of interrupt processing of TX3922.It masks temporarily beforehand in interrupt processing and it makes enable again after interrupt processing. By being so, when there is an other interrupt factor, it is possible to make a interrupt occur to TX3922 again.

It becomes 1 with the power on reset

(3) Outside input interrupt status register (10808100H)

It reads the interrupt status of the outside input and the interrupt factor can be distinguished between.

Also, it interrupts in writing 1 in the corresponding bit and the request condition can be cleared.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
EXTINT STATUS	R/W	—			IO3 INT1	IO3 INT0	IO5 INT3	IO5 INT2	IO5 INT1	IO5 INT0

IO5INT3-0 : interrupt from the device which is connected with the I/O bus (5 V input)

1:request condition

The request condition can be cleared in writing `1' in this bit.

IO3INT1-0 : interrupt from the outside input (3.3 V input)

1:request condition

The request condition can be cleared in writing `1' in this bit.

It becomes 0 with the power on reset.

(4) Outside input interrupt status register (After the mask) (10808104H)

The interrupt status behind the mask can be read. This status is AND of the interrupt status of (3) and interrupt enable of (5).

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
EXTINT STATUSM	RD	—			IO3M INT1	IO3M INT0	IO5M INT3	IO5M INT2	IO5M INT1	IO5M INT0

IO5MINT3-0 : The interrupt from the device which is connected with the I/O bus.

1:request condition

IO3MINT1-0 : interrupt from the outside input

1:request condition

（５）Interrupt enable register from the outside input (10808110H)

It sets input enable and interrupt enable to the status register of the interrupt factor input every factor.

	R/W	D32-16	D15	D14	D13	D12	D11	D10	D9	D8
EXTINT ENABLE	R/W	—			IO3 SEN1	IO3 SEN0	IO5 SEN3	IO5 SEN2	IO5 SEN1	IO5 SEN0

D7	D6	D5	D4	D3	D2	D1	D0
		IO3 IEN1	IO3 IEN0	IO5 IEN3	IO5 IEN2	IO5 IEN1	IO5 IEN0

IO5IEN3-0 : It makes a interrupt from the device which is connected with the I/O bus enable.
It permits a interrupt at 1 and it prohibits a interrupt at 0.

IO3IEN1-0 : It makes a interrupt from the input outside enable.
It permits a interrupt at 1 and it prohibits a interrupt at 0.

IO5SEN3-0 : It makes the input of the interrupt from the device which is connected with the I/O bus enable.
It permits a interrupt at 1 and it prohibits a interrupt at 0.

IO3SEN1-0 : It makes the input of the interrupt from the spare input enable.
It permits a interrupt at 1 and it prohibits a interrupt at 0.

When off the power of the device which is connected with the I/O bus, make IO5SEN "0" and make the input of the interrupt prohibition.

It becomes 0 with the power on reset.

（6）PC card interrupt status register (10808200H)

It reads interrupt status from the PC card and the interrupt factor can be distinguished between. Also, in to write "1" in the corresponding bit, the interrupt request condition can be cleared.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
PCCINT STATUS	R/W	—					C2RI INT	C2IO INT	C1RI INT	C1IO INT

C1IOINT : I/O Interrupt from PC card 1.
1:request condition. In to write "1" in this bit, the request condition can be cleared.

C1RIINT : RI Interrupt from PC card 1.
1:request condition. In to write "1" in this bit, the request condition can be cleared.

C2IOINT : I/O Interrupt from PC card 2.
1:request condition. In to write "1" in this bit, the request condition can be cleared.

C2RIINT : RI Interrupt from PC card 2.
1:request condition. In to write "1" in this bit, the request condition can be cleared.

It becomes 0 with the power on reset.

（7）PC card interrupt status register (10808204H)

The status of the interrupt from the PC card after the mask can be read. This status is and of the interrupt status of (6) and interrupt enable of (8).

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
PCCINT STATUSM	RD	—					C2RI INTM	C2IO INTM	C1RI INTM	C1IO INTM

C1IOINTM : I/O Interrupt from PC card 1.
1:request condition.

C1RIINTM : RI Interrupt from PC card 1.
1:request condition.

C2IOINTM : I/O Interrupt from PC card 2.
1:request condition.

C2RIINTM : RI Interrupt from PC card 2.
1:request condition.

(8) PC card interrupt enable register (10808210H)

It sets status enable and interrupt enable of the interrupt factor every factor.

	R/W	D32-16	D15	D14	D13	D12	D11	D10	D9	D8
PCCINT ENABLE	R/W	—					C2RI SEN	C2IO SEN	C1RI SEN	C1IO SEN

D7	D6	D5	D4	D3	D2	D1	D0
				C2RI IEN	C2IO IEN	C1RI IEN	C1IO IEN

C1IOIEN : It enables I/O interrupt from PC card 1.
It permits a interrupt at 1.It prohibits a interrupt at 0.

C1RIIEN : It enables RI interrupt from PC card 1.
It permits a interrupt at 1.It prohibits a interrupt at 0.

C2IOIEN : It enables I/O interrupt from PC card 2.
It permits a interrupt at 1.It prohibits a interrupt at 0.

C2RIIEN : It enables RI interrupt from PC card 2.
It permits a interrupt at 1.It prohibits a interrupt at 0.

C1IOSEN : It enables the input of the I/O interrupt Input from PC card 1.
It permits a interrupt Input at 1.It prohibits a interrupt output at 0.

C1RISEN : It enables the input of the I/O interrupt Input from PC card 1.
It permits a interrupt Input at 1.It prohibits a interrupt output at 0.

C2IOSEN : It enables the input of the I/O interrupt Input from PC card 2.
It permits a interrupt Input at 1.It prohibits a interrupt output at 0.

C2RISEN : It enables the input of the I/O interrupt Input from PC card 2.
It permits a interrupt Input at 1.It prohibits a interrupt output at 0.

It becomes 0 with the power on reset.

(9) PC card interrupt detection register (10808220H)

It chooses a clock for the I/O interrupt of the PC card .

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
PCCINT CLOCK	R/W	—								PCC CLK

PCCCLK : It chooses a clock for the I/O interrupt of the PC card .
It shows the operation clock of the controller in "0".
It shows RTC clock in "1".
It becomes 0 with the power on reset.

It uses this register by the I/O interrupt from the PC card at the time of "suspend mode" when making "Wake up".
Because the system clock stops at suspend, when
" Wake up " is necessary, set interrupt detection to the clock of RTC.
Generally, when working, set to the system clock. When setting to the RTC clock, it begins detection for equal to or more than 30 μ s.

(10) USB interrupt enable register (10808310H)

It sets enable of the clock resumption request interrupt from the USB host controller.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
USB INTEN	R/W	—							USB IEN	USBW IEN

USBWIEN : It enables the clock restart request interrupt from the USB host controller.
It permits the interrupt in "1". It prohibits the interrupt in "0"

USBIEN : It master-enables the USB interrupts (USBINT and USBWAKE).
It permits the interrupts in "1". It prohibits the interrupts in "0"

This register is reset to "0" by the power-on reset.

(11) SmartMedia interrupt enable register (10808410H)

It sets enable of the clock resumption request interrupt from the SmartMedia controller.

	R/W	D32-8	D7	D6	D5	D4	D3	D2	D1	D0
SM INTEN	R/W	—								SM IEN

SMIEN : It makes a interrupt from the SmartMedia controller(SMINT) enable.

1 : interrupt enable.

0 : interrupt disable.

When this bit is 0, it doesn't output a interrupt signal in TX3922.

It isn't possible to see the status of squeeze status register (10808000H),too.

It becomes **0** with the powering reset.

It uses this bit to mask a s interrupt temporarily in interrupt processing.

There is a control bit of interrupt enable in the SmartMedia controller, too.

Refer to the specification, too.

5.13. Debugging support

5.13.1. About the interface with the debugging board which Plum2 handles

It debugs a system using the substrate for the debugging which connects with the MROM connector.
Plum2 handles chip selection, Wait, a interrupt signal as the signal for the debugging board.

Allocation of address

It allocates the address of the debugging board for the address in the MCS0 space of TX3922 as follows.

Debugging support physical address

MCS0 6C4190000H-6C419FFFH

5.14. ID register (108B0000H)

	R/W	D32-16	D15	D14	D13	D12	D11	D10	D9	D8
ID	RD	—	REV 15	REV 14	REV 13	REV 12	REV 11	REV 10	REV 9	REV 8

D7	D6	D5	D4	D3	D2	D1	D0
REV 7	REV 6	REV 5	REV 4	REV 3	REV 2	REV 1	REV 0

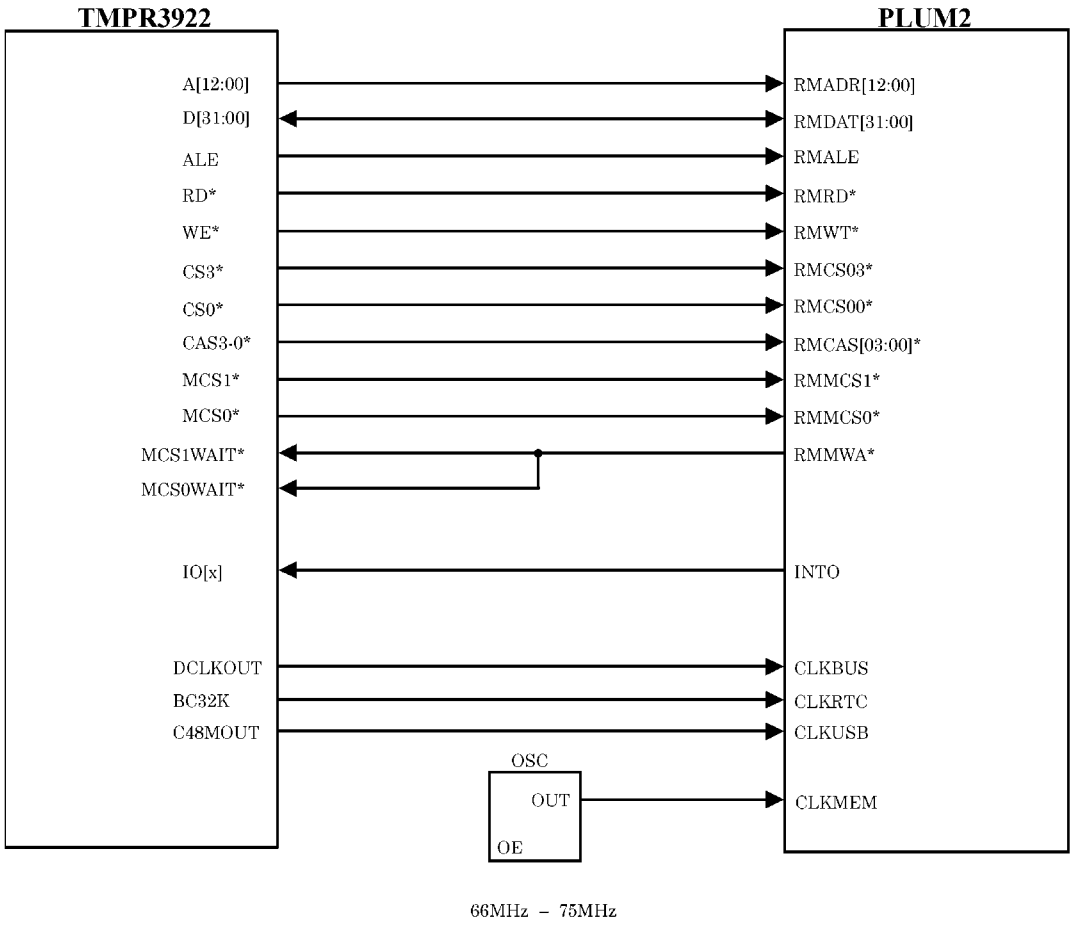
REV15-0 : PLUM2 Revision.

PLUM2 #1 : 0002

PLUM2 #2 : 0102

5.15. Signal connection guidance

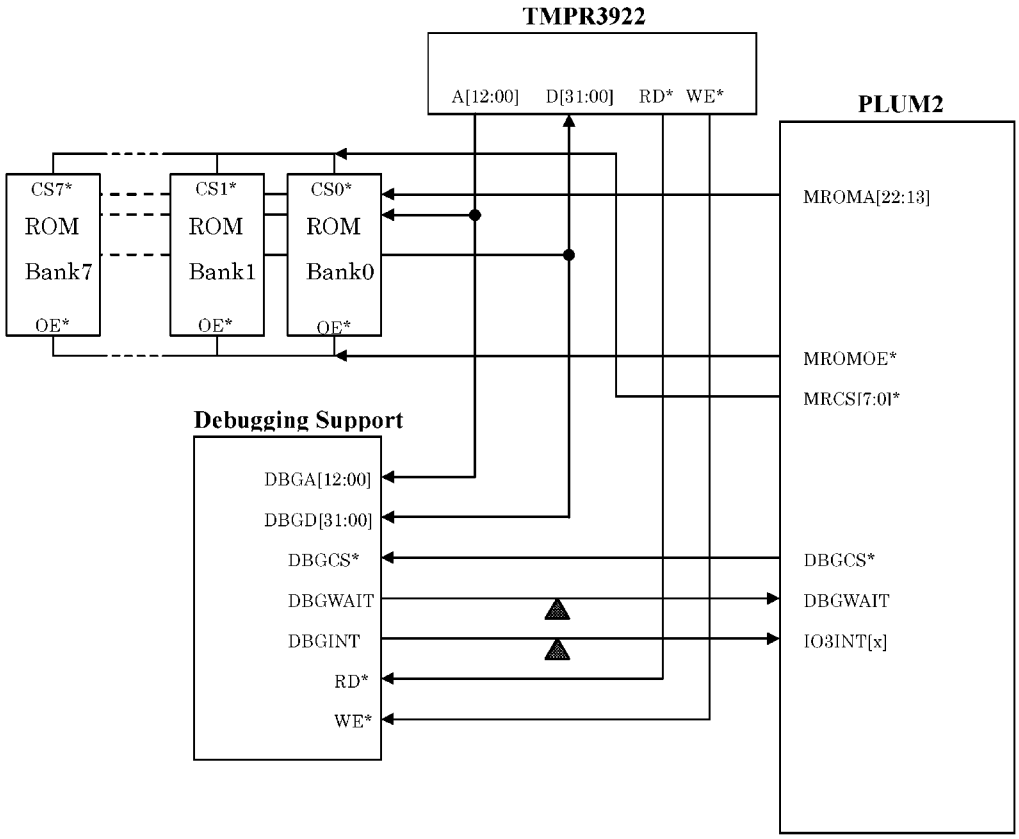
5.15.1. Connection between TMPR3922 and PLUM2



* Active-low signal

Note 1: TMPR3922 must **be Little Endian** Mode.

5.15.2. Mask ROM and Debug Board Connection



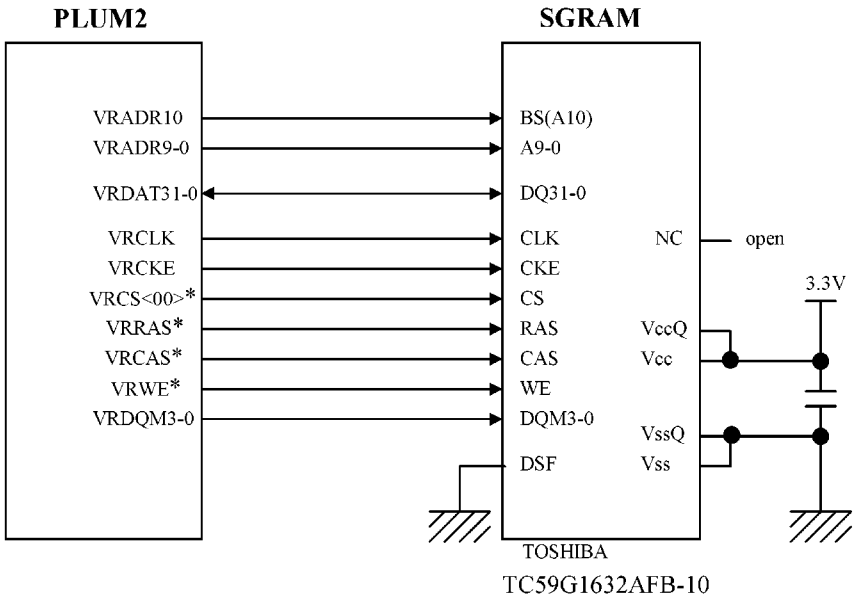
* Active-low signal

▲ : Pull Down

Note1: It is recommended to pull down **DBGWAIT** and **DBGCS*** so that any input line may not be floating even if debug board is not connected.

5.15.3. Video RAM Connection

PLUM2 supports **SGRAM (Synchronous Graphic RAM)** as VIDEO RAM.



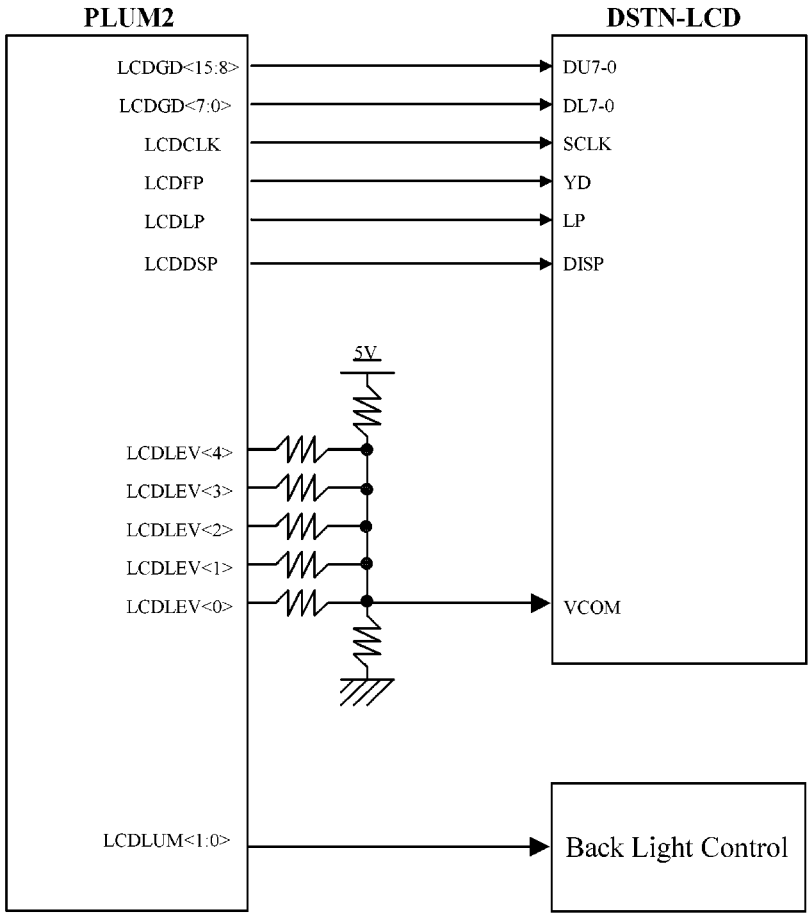
* Active-low signal

Note that: This figure shows a case of **2Mbyte** VIDEO RAM constructed by **One Memory Bank**.

5.15.4. LCD panel connection

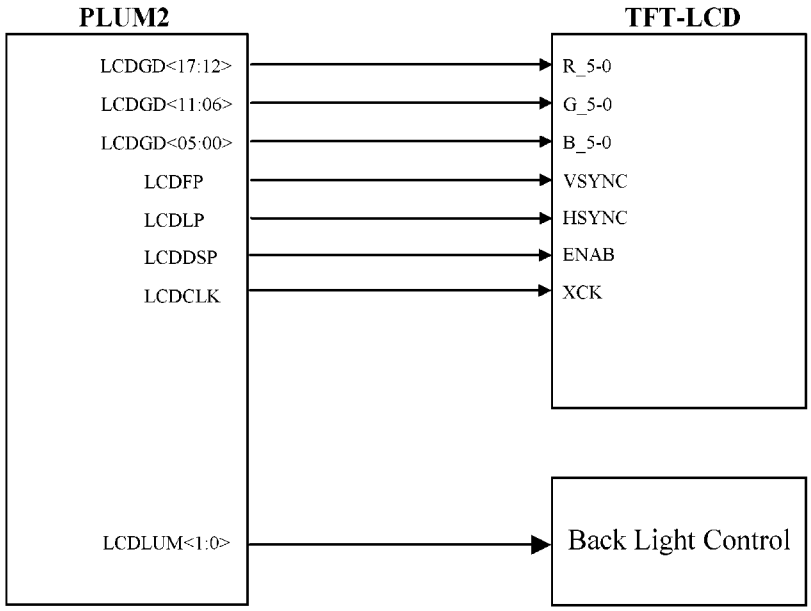
PLUM2 supports **LCD output functions** that is supported both **DSTN-LCD** and **TFT-LCD**.

(1) DSTN-LCD PANEL



Note that: LCDLEV<4:0> signals are Open-Drain signals.

(2) TFT-LCD PANEL

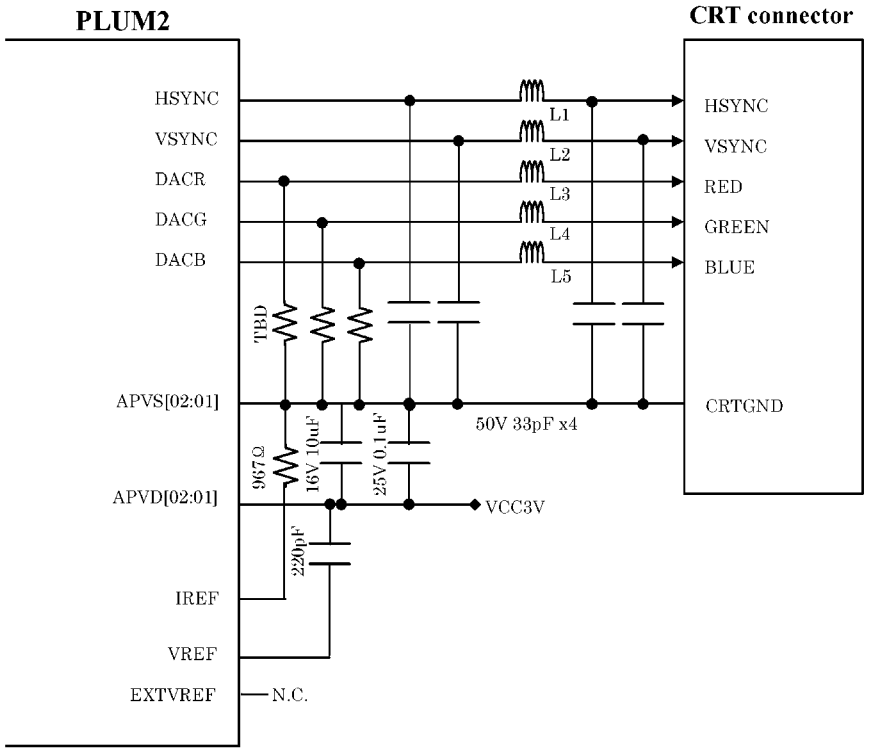


PLUM2 has four control signals to supports many kinds of TFT-LCD panel.

LCD<15:8> : open for STN LCD panel

5.15.5. CRT connection

PLUM2 support CRT output function by using internal RAMDAC.



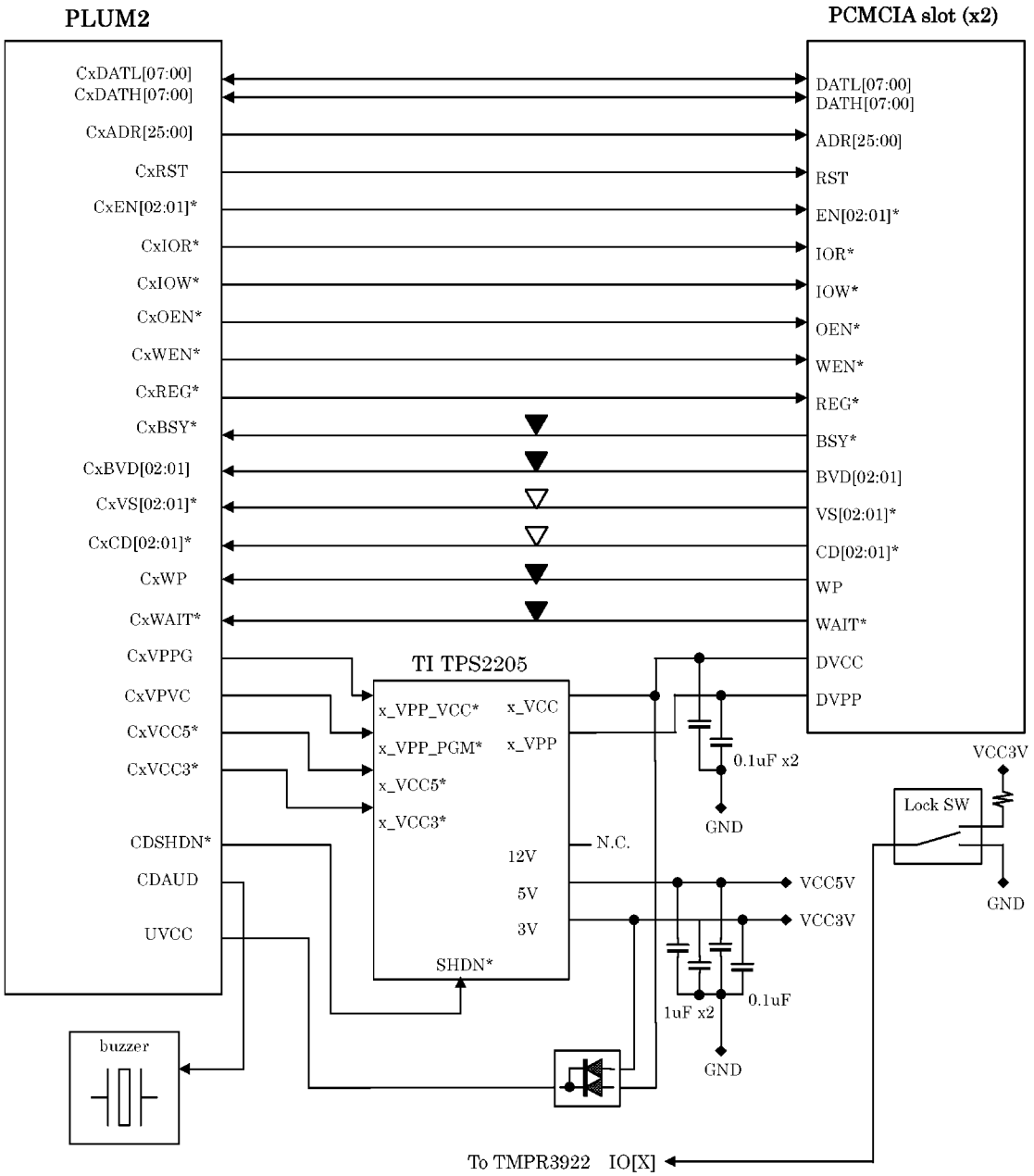
L1,L2 : TAIYOU YUDEN BK2125HS101 etc

L3,L4,L5 : TAIYOU YUDEN BK1608HS471 etc

Note that: All parameters of **R, C** and **L** should be adjusted to each system.

5.15.6. PCMCIA connection

PLUM2 supports two slot of PCMCIA I/F.



▽ : Pull Up to VCC3V

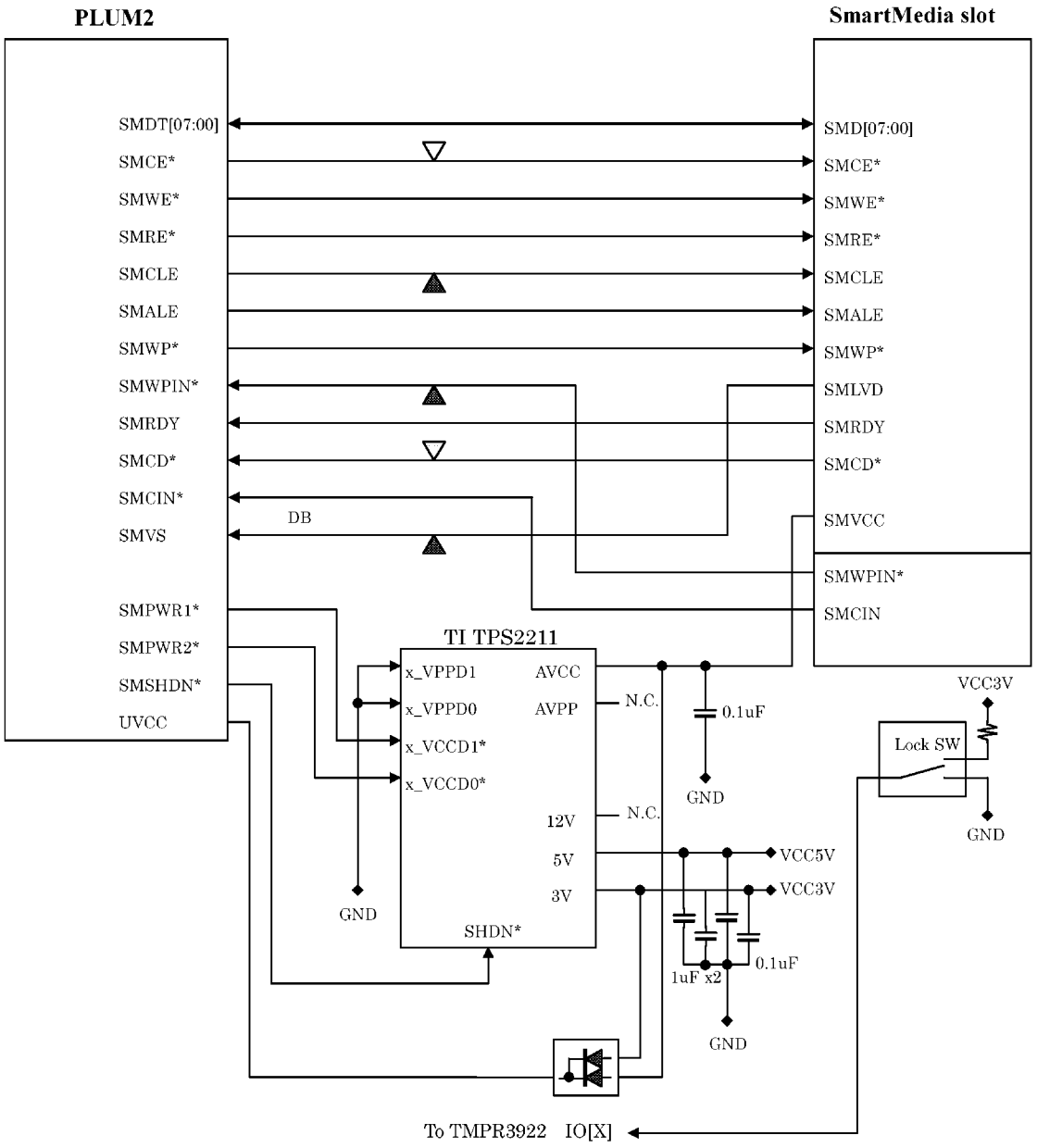
▼ : Pull Up to DVCC

* Active-low signal

Note that: UVCC should NOT be ground (i.e. 0V). This power line MUST keep to **3.3 volts** or **5 volts** whenever system stays in normal state (i.e. not suspend state).

5.15.7. SmartMedia connection

PLUM2 supports one slot of SmartMedia I/F.



▽ : Pull Up to SMVCC

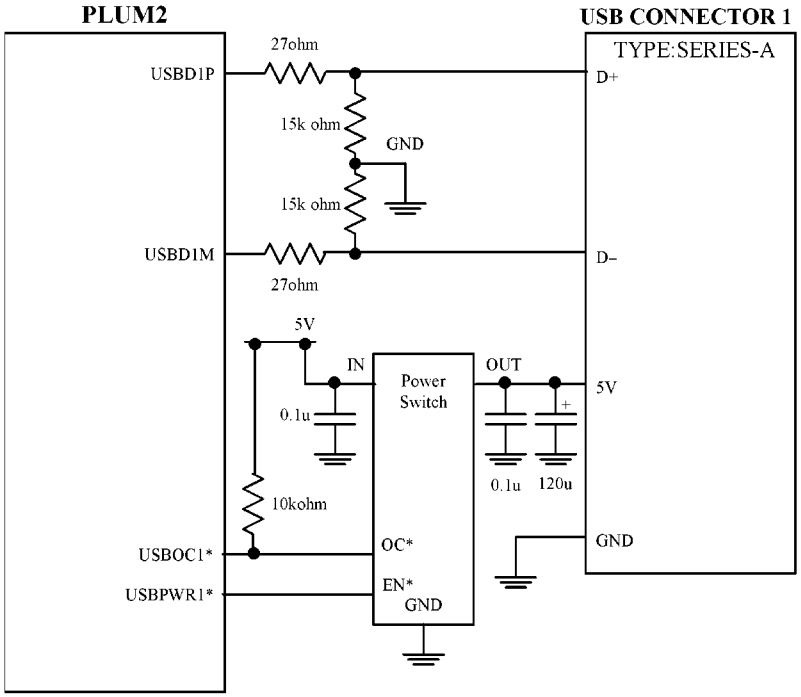
▲ : Pull down to GND

* Active-low signal

Note that: UVCC should NOT be ground (i.e. 0V). This power line MUST keep to **3.3 volts** or **5 volts** whenever system stays in normal state (i.e. not suspend state).

5.15.8. USB connection

PLUM2 supports two ports of **USB-HOST** function.



* Active-low signal

Typical power switch device : Texas Instruments — TPS2014 or TPS2015

This figure shows only one port of USB function of PLUM2. Use similar circuitry for USB CONNECTOR 2(i.e. another USB port of PLUM2).

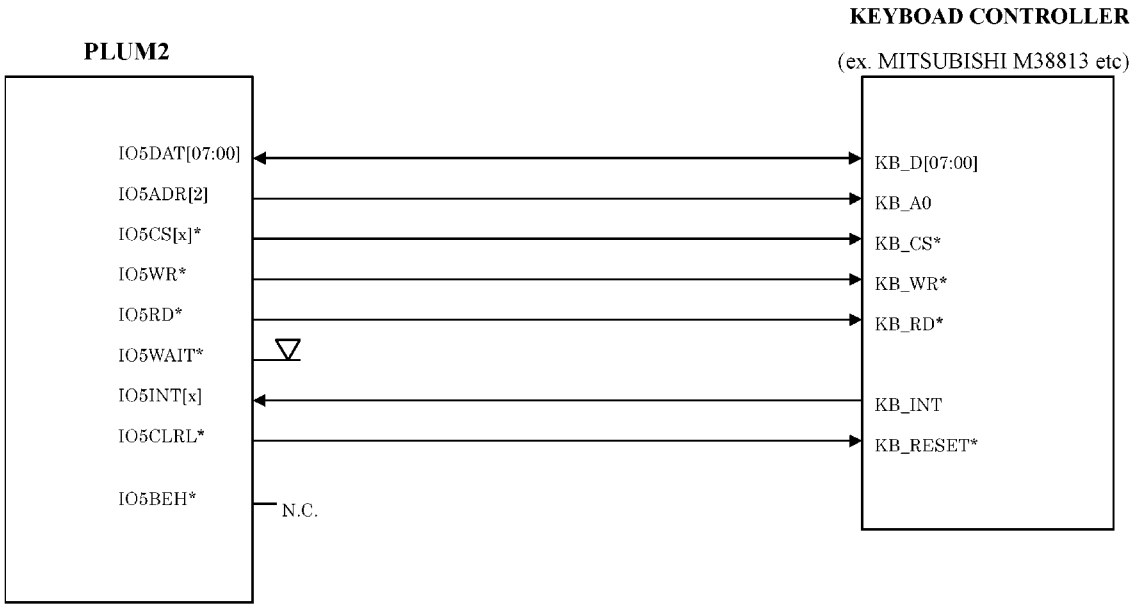
Note that: Component values are to be determined by experiment.

5.15.9. I/O bus connection

PLUM2 supports **16/8 bit I/O bus** that contains similar function/signal to **ISA bus**.

(1)KEYBOAD CONTROLLER

This figure shows sample logic for **16/8 bit I/O Bus** to support **Keyboard** and/or **Mouse** function.

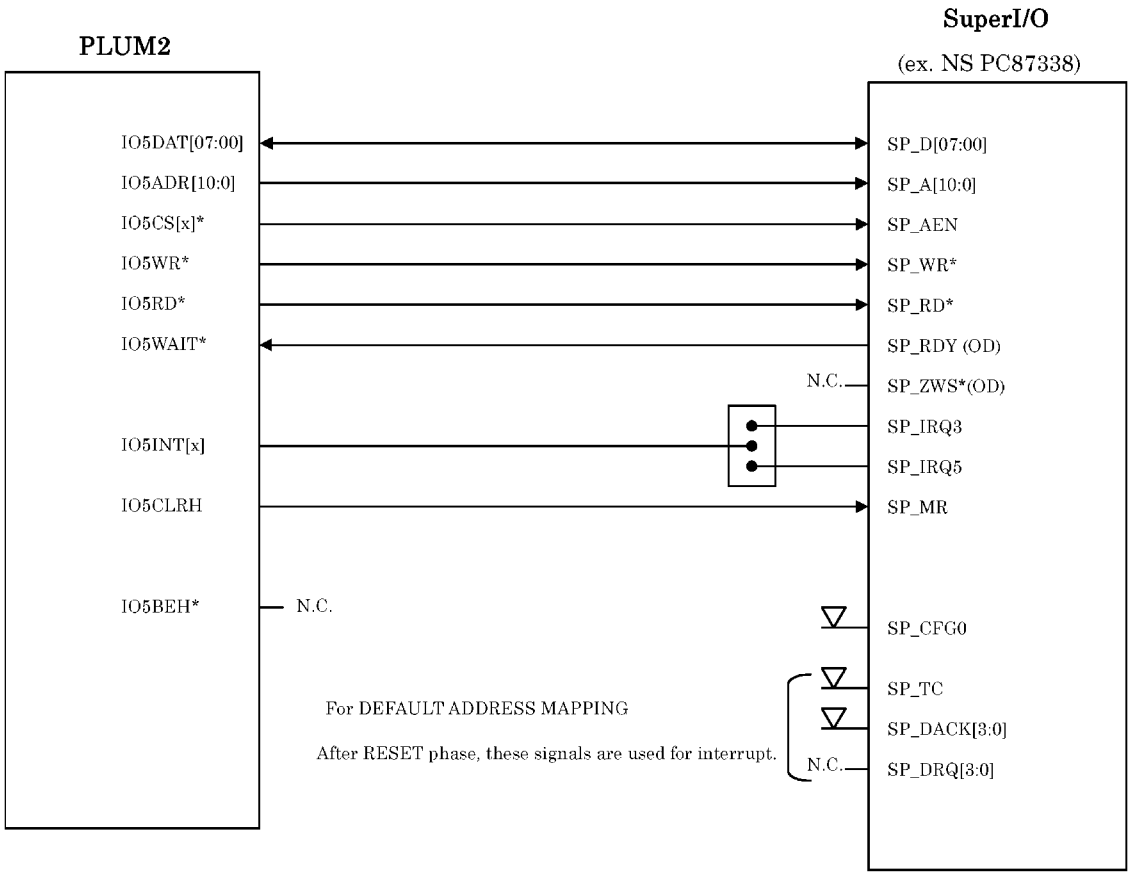


▽ : Pull Up to VCC5V

* Active-low signal

(2) I/O bus connection

This figure shows sample logic for **16/8 bit I/O bus** to support **Parallel, serial port** and **IDE** function.



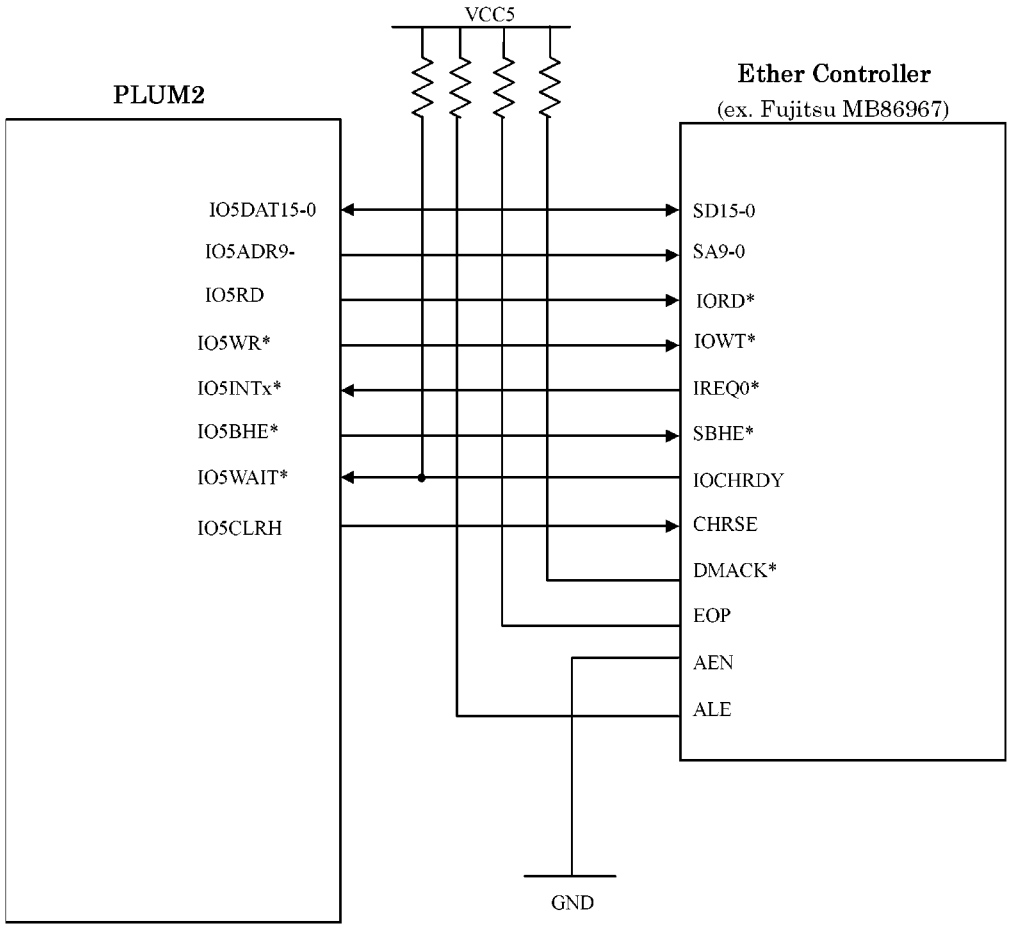
▽ : Pull Up to VCC5V

* Active-low signal

Super I/O supports Parallel port**, additional** Serial port **and** IDE **I/F.**

(3) Ethernet Interface

This figure shows sample logic for **16/8 bit I/O Bus** to support **Ethernet port**.



* Active-low signal

Note: In this sample system, MB86967 is used on **ISA BUS Interface Mode**.

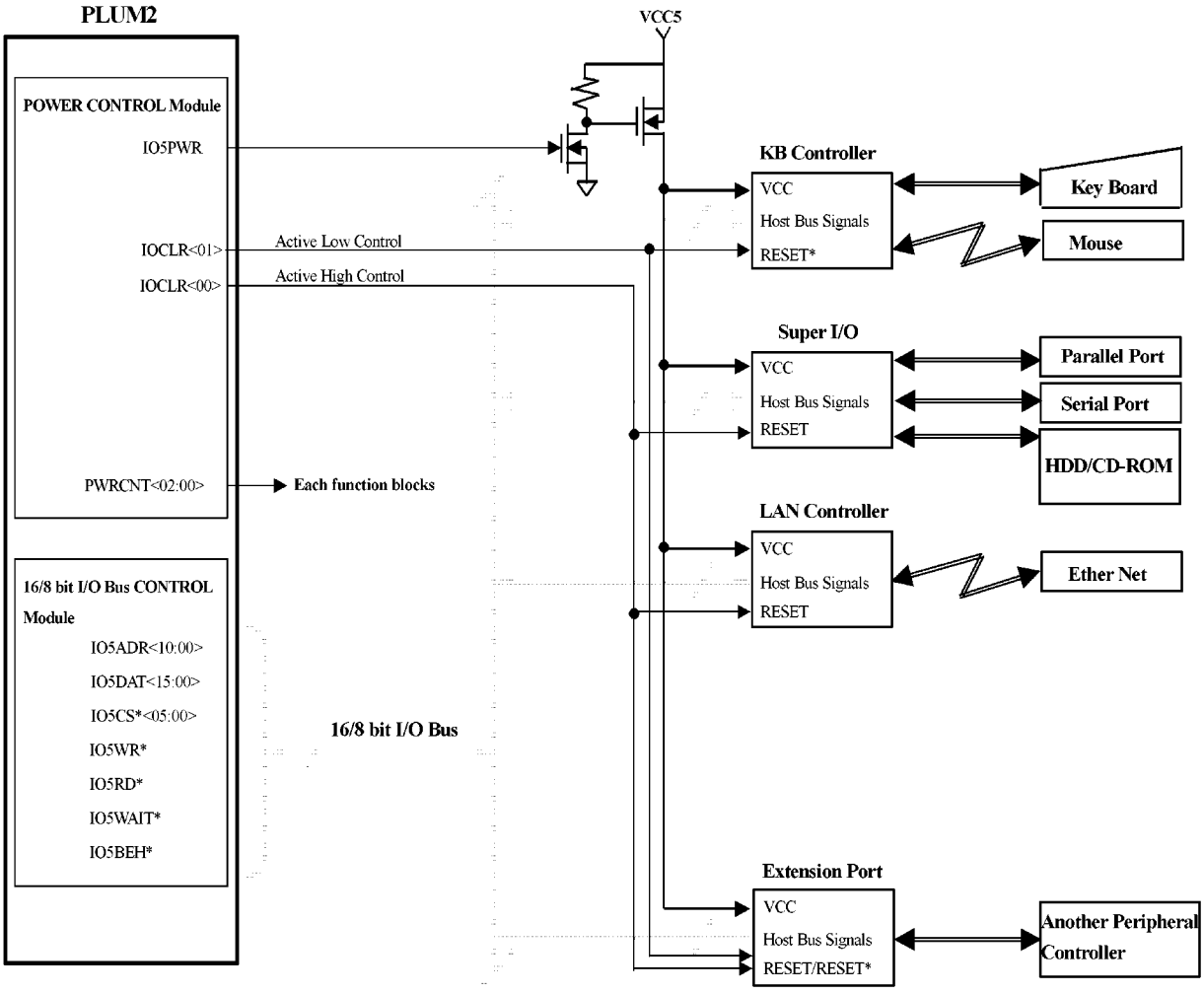
5.15.10. Power management

The PLUM2 has three groups of power management signals.

- **IO5PWR** Power control signal for the **16/8 bit I/O Bus**.
- **IOCLRH/IOCLRL*** Clear signals for the **16/8 bit I/O device** on the **16/8 bit I/O Bus**.
- **PWRCNT<02:00>** Power control signals for **VIDEO functions** of the PLUM2.

(1) For 16/8 bit I/O Bus

IO5PWR signal controls whole 5V power lines of **16/8 bit I/O Bus** and **IOCLRH/IOCLRL*** controls clear signals of each **external ISA controllers** connected on the **16/8 bit I/O Bus** as bellow figure.



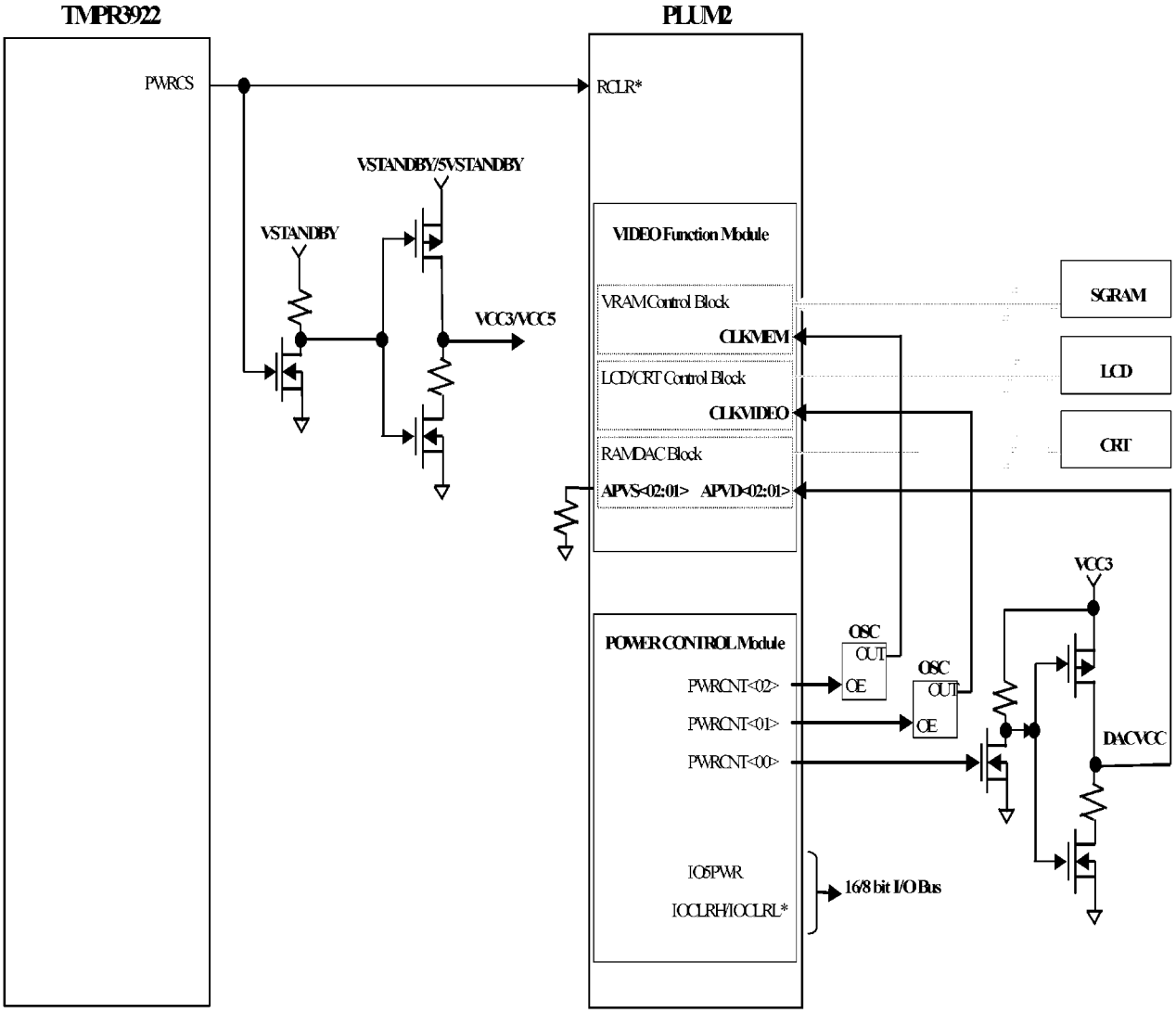
Note 1: All **16/8 bit I/O Bus signals** outputs **Low** level when **IO5PWR** is de-asserted. Due to this fact, **power line for 16/8 bit I/O Bus** is controlled as **5 volts** or **Open** (this power line does **NOT pulled down** to ground level).

Note 2: IOCLR reset only one **5 volts device**. If software wold like to reset each **external ISA controller** individually, control each RESET pin by using MFIO[x] or IO[x] of the TMPR3922U.

(2) For VIDEO functions of the PLUM2

PWRCNT<02:00> controls three kinds of VIDEO function groups of the PLUM2 as shown as bellow.

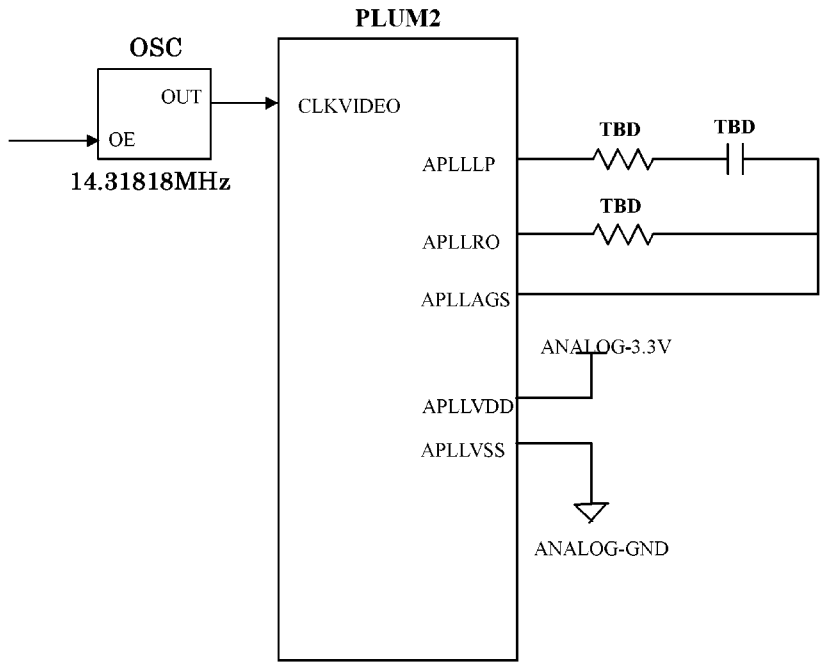
- **PWRCNT<02>** This signal controls Enable signal of the **oscillator** for the **VRAM control**.
- **PWRCNT<01>** This signal controls Enable signal of the **oscillator** for the **LCD module**.
- **PWRCNT<00>** This signal controls **FET Switch** that gates power line for **RAMDAC**.



Note that: Before turn off the power line for **APVD<02:01>**, **PCDAC<01>** that is a internal register of PLUM2 **MUST** set as **ZERO**. **PCDAC<01> is JUST allowed when 3.3 volts power is supplied for APVD<02:01>**

5.15.11. Video clock

PLUM2 includes internal Analog PLL (Phase Locked Loop) logic



Note that: APLLVDD and APLLVSS are ANALOG power supply signals. ANALOG power line/power Plane MUST separate form DIGITAL power line/power plane by using resistance and/or inductor.

Change Record (1/2)

Up Date	REV	total page	contents
13.APR	1.0	26	FIRST EDITION
17.APR	2.0	26	Page 2 BLOCK DIAGRAM VRAM modify A(11) to A(10) LCD modify C(15) to C(14) PCMCIA modify C(22) to C(21) Insert JTAG module Page 4,5 PIN NAMES change Page 6 VRADR<11:00> to VRADR<10:00> Page 7 C1LOK cut Page 8 C2LOK cut SMLOK cut Page 9 JTAG module functions insert Page 18 CRT CONNECTION C1LOK cut and Lock SW connect to TMPR3922 IO[X] Page 19 PCMCIA CONNECTION SMLOK cut and Lock SW connect to TMPR3922 IO[X]
05.JUN	3.0	150	The register specification addition Page140 CRT CONNECTION
10.AUG	3.1	150	Page12 SMPWR1* to SMPWR1 , SMPWR2* to SMPWR2 Page142 SMPWR1* to SMPWR1 , SMPWR2* to SMPWR2 TPS2211 to TPS2205 The change of the connection (VREF and IREF) The register specification deletion.
20.OCT	3.2	156	Page.3 Correct contents items of USB(5.10) Page 9 , 12 Pin name Y04 C1AUD to CDAUD AJ14 C2CFSD* to CDSHDN* C01 IO5BEH to IO5BHE Page13 USB Interface Correct descriptions of USBD2P,USBD2M USBOC1, USBOC2 3.3V -> 5V Page16 MROM Bank 16MB addition Page17 MCS0 I/OBUS Capacity 32KB to 24KB Page18 PLUM register (TESTMOD,SMIEN,PLUMID) Page25 VRAM Memory Size Page32 Note4 addition. Page38 “Sample setting of TOSHIBA SGRAM TC59G1632AFB” addition Page39 POCKL register

Change Record (2/2)

Up Date	REV	total page	contents
20.OCT	3.2	156	Page40 POPLL register Page41 PLCNT register Page37 VRAM Control register D12: **0**:Enable 1:Disable to **0**: Disable 1: Enable Page43 PCDAC register Page44 PLHPX register Page46 PLGMD register Page48 PCHPX register Page51 PCGMD register Page58 Access timing table Page101 An explanation to "SMBOF1-0" was added. Page109 An explanation to "I/O wait control register2"was added. Page111 Delete section title 'Introduction' 5.10.1 Overview Add conformance to USB specification Add reference WWW page addresses Page112 5.10.2.3 Add section 'Shared RAM Controller Clock' Page113 5.10.2.5 Interrupt Move from 5.10.4 Add Figure.1 (interrupt enable control) Page114 5.10.2.6 Move from 5.10.6 5.10.2.7 Add section 'Reset Operation' 5.10.2.8 Move from 5.10.7 Page123 5.10.5.3 Difference from USB Specification Rewrite description Add description about USB specification revision 1.1 Page126 (2) Clock Control Register Correct description of USBCLK1, USBCLK2 Page127 MROM_ADD CONTROL register Page131 An explanation to "Interrupt enable register" was added. Page136 An explanation to "PC card interrupt enable register" was added. (10) USB Interrupt Enable Register Correct description Add USBWIEN Page137 USBINTEN register Page139 ID register addition Page144 An explanation to "TFT-LCD PANEL" was added. Page146 It deletes IOR*,IOW* pull up. Page148 5.15.8 USB Connection Correct pull-up for USBOC1* Page151 Ethernet Interface