



SP8000 SERIES

HIGH SPEED DIVIDERS

SP8650A, B & M 600MHz ÷ 16
SP8651A, B & M 500MHz ÷ 16
SP8652A, B & M 400MHz ÷ 16

The SP8650 series of UHF ÷ 16 counters are fixed ratio synchronous emitter coupled logic counters with, in the case of the SP8650, a maximum operating frequency in excess of 600MHz. All three devices operate up to their maximum specified operating frequencies over temperature ranges of -55°C to $+125^{\circ}\text{C}$ ('A' grade), 0°C to $+20^{\circ}\text{C}$ ('B' grade) and -40°C to $+85^{\circ}\text{C}$ ('M' grade). The input is normally capacitively coupled to the signal source but the circuits can be DC driven if required. The inputs can be either single driven relative to the on-chip reference voltage or differentially driven.

There are two complementary emitter follower outputs.

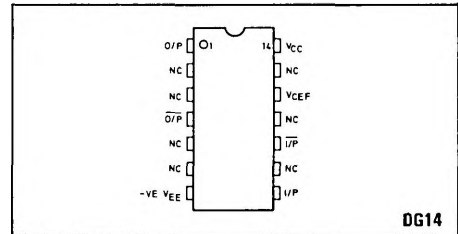


Fig. 1 Pin connections

FEATURES

- Low Power - Typically 250mW
- ECL II & ECL III Output Compatibility
- Easy Operation From UHF Signal Source

APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

QUICK REFERENCE DATA

- Power Supplies $V_{CC} = 0\text{V}$
 $V_{EE} = -5.2\text{V} \pm 0.25\text{V}$
- Temperature Range 'A' grade -55°C to $+125^{\circ}\text{C}$
'B' grade 0°C to $+70^{\circ}\text{C}$
'M' grade -40°C to $+85^{\circ}\text{C}$
- Input Amplitude Range 400mV to 800mVp-p
- Output Voltage Swing 800mV typ. p-p

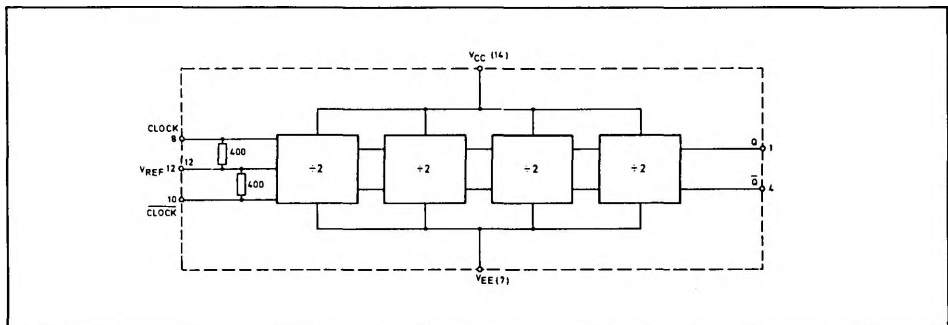


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

$T_{amb} = -55^{\circ}\text{C}$ to -125°C ('A' grade)

0°C to +70°C ('B' grade)

—40°C to —85°C ('M' grade)

Supply Voltage

 $V_{CC} = 0V$
$$V_{EE} = -5.2V + 0.25V$$

Output load = 500Ω in parallel with approx. 3pF

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Toggle frequency	SP8650	600			HMz	Test circuit as in fig. 2
	SP8651	500			MHz	V _{IN} = 400 to 800mV p-p
	SP8652	400			MHz	V _{IN} = 400 to 800mV p-p
Min. toggle frequency for correct operation with a sinewave input	All			40	MHz	V _{IN} = 400 to 800mV p-p
Min. slew rate for square wave input to guarantee correct operation to OHz	All			100	V/μs	
Input reference voltage	All		2.6		V	
Output voltage swing (dynamic)	All	500	800		mV	p-p
Output voltage (static)						
high state	All	—8.95		.615	V	
Low state	All	—1.83		—1.435	V	
Power supply drain current	All		45	60	mA	

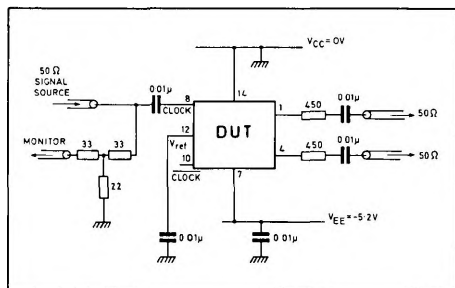


Fig. 3 Toggle frequency test circuit

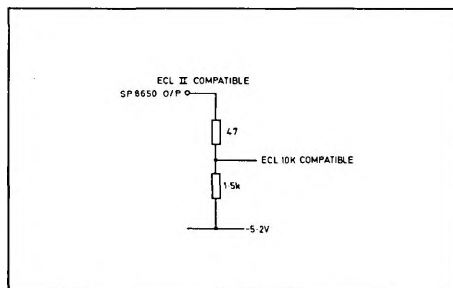


Fig. 4 SP8650 to ECL 10K interface

Toggle Frequency Test Circuit

1. All leads are kept short to minimise stray capacitance and induction.
2. Resistors and capacitors are non-inductive UHF types.
3. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

ABSOLUTE MAXIMUM RATINGS

Power supply voltage / $V_{CC} - V_{EE}$	8 volts
Input voltage V_{INac}	2.5V p-p
Output source curr I_{out}	10mA
Storage temperature range	-55°C to +125°C
Operating junction temperature	150°C max.

OPERATING NOTE

Normal UHF layout techniques should be used if the SP8650 series of dividers are to operate satisfactorily. If the positive supply is used as the earth connection, noise immunity is improved and the risk of damage due to inadvertently shorting the output emitter followers to the negative rail is reduced.

The circuit is normally capacitively coupled to the signal source. In the absence of an input signal the circuit will self-oscillate. This can be prevented by connecting a $10\text{K}\Omega$ resistor between one of the inputs and the negative rail.

The device will also miscount if the input transitions are slow — a slew rate of $100\text{V}/\mu\text{s}$ or greater is necessary for low frequency operation.

The outputs interface directly to ECL II or to ECL 10K with a potential divider (see Fig. 4).

A typical application of the SP8650 series devices would be in the divider chain of a synthesiser operating in the military frequency range 225 MHz to 512 MHz. A binary division rate is optimum where power is at a premium and so the SP8650 series would normally be used in low power applications.

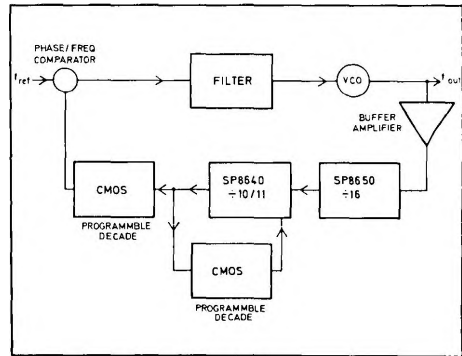


Fig. 5 A low power synthesiser loop