

LP38841-ADJ 0.8A Ultra Low Dropout Adjustable Linear Regulators

Stable with Ceramic Output Capacitors

Check for Samples: [SOLP38841-ADJ](#)

FEATURES

- Ideal for Conversion from 1.8V or 1.5V Inputs
- Designed for Use with Low ESR Ceramic Capacitors
- Ultra Low Dropout Voltage (75mV @ 0.8A typ)
- 0.56V to 1.5V Adjustable Output Range
- Load Regulation of 0.1%/A (typ)
- 30nA Quiescent Current in Shutdown (typ)
- Low Ground Pin Current at all Loads
- Over Temperature/Over Current Protection
- Available in 8 Lead SO nnnn
- -40°C to +125°C Junction Temperature Range
- UVLO Disables Output when $V_{BIAS} < 3.8V$

APPLICATIONS

- ASIC Power Supplies In:
 - Desktops, Notebooks, and Graphics Cards, Servers
 - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulators

DESCRIPTION

The LP38841-ADJ is a high current, fast response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in the SO package.

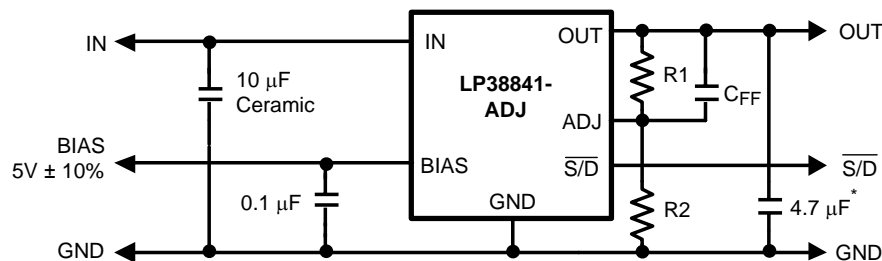
Dropout Voltage: 75 mV (typ) @ 0.8A load current.

Quiescent Current: 30 mA (typ) at full load.

Shutdown Current: 30 nA (typ) when S/D pin is low.

Precision Reference Voltage: 1.5% room temperature accuracy.

Typical Application Circuit



* Minimum value required if Tantalum capacitor is used (see [APPLICATION HINTS](#)).



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Connection Diagram

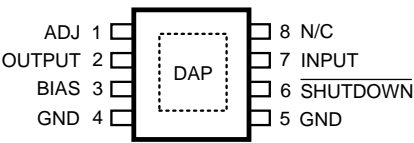
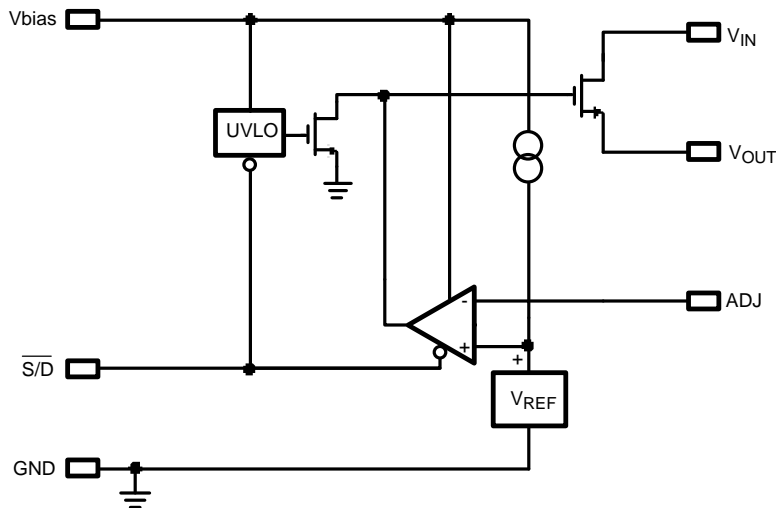


Figure 1. SO-8 – Top View

PIN DESCRIPTION

| Pin Number | Pin Name | Pin Description |
|------------|----------|--|
| 1 | ADJ | The Adjust pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2 (see Typical Application Circuit). |
| 2 | OUTPUT | The regulated output voltage is connected to this pin. |
| 3 | BIAS | The Bias pin is used to provide the low current bias voltage to the chip which operates the internal circuitry and provides drive voltage for the N-FET. |
| 4, 5 | GND | These are the power and analog grounds for the IC. Connect both pins to ground. |
| 6 | SHUTDOWN | This provides a low power shutdown function which turns the regulated output OFF. Tie to V_{BIAS} if this function is not used. |
| 7 | INPUT | The high current input voltage which is regulated down to the nominal output voltage must be connected to this pin. Because the bias voltage to operate the chip is provided separately, the input voltage can be as low as a few hundred millivolts above the output voltage. |
| 8 | N/C | This pin is floating, it has no internal connection. |
| DAP | DAP | The SO DAP is a thermal connection that is physically connected to the backside of the die, and is used as a thermal connection to the PC Board copper. The DAP is not a ground pin connection, but should be connected to ground potential. |

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

| | |
|---|---|
| Storage Temperature Range | –65°C to +150°C |
| Lead Temp. (Soldering, 5 seconds) | 260°C |
| ESD Rating | Human Body Model ⁽³⁾ Machine Model ⁽⁴⁾ |
| | 2 kV 200V |
| Power Dissipation ⁽⁵⁾ | Internally Limited |
| V _{IN} Supply Voltage (Survival) | –0.3V to +6V |
| V _{BIAS} Supply Voltage (Survival) | –0.3V to +7V |
| Shutdown Input Voltage (Survival) | –0.3V to +7V |
| V _{ADJ} | –0.3V to +6V |
| I _{OUT} (Survival) ⁽⁶⁾ | Internally Limited |
| Output Voltage (Survival) | –0.3V to +6V |
| Junction Temperature | –40°C to +150°C |

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see the [ELECTRICAL CHARACTERISTICS](#). Specifications do not apply when operating the device outside of its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.
- (4) The machine model is a 220 pF capacitor discharged directly into each pin.
- (5) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.
- (6) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

OPERATING RATINGS

| | |
|--------------------------------------|---|
| V _{IN} Supply Voltage | (V _{OUT} + V _{DO}) to 5.5V |
| Shutdown Input Voltage | 0 to +5.5V |
| I _{OUT} | 0.8A |
| Operating Junction Temperature Range | –40°C to +125°C |
| V _{BIAS} Supply Voltage | 4.5V to 5.5V |
| V _{OUT} | 0.56V to 1.5V |

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = V_O(NOM) + 1V, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = 10 μF CER, C_{OUT} = 22 μF CER, V_{S/D} = V_{BIAS}. Min/Max limits are specified through testing, statistical correlation, or design.

| Symbol | Parameter | Conditions | MIN | TYP ⁽¹⁾ | MAX | Units |
|-----------------------------------|---|--|-----------------------|--------------------|-----------------------|-------|
| V _{ADJ} | Adjust Pin Voltage | 10 mA < I _L < 0.8A V _O (NOM) + 1V ≤ V _{IN} ≤ 5.5V 4.5V ≤ V _{BIAS} ≤ 5.5V | 0.552 0.543 | 0.56 | 0.568 0.577 | V |
| I _{ADJ} | Adjust Pin Bias Current | 10 mA < I _L < 0.8A V _O (NOM) + 1V ≤ V _{IN} ≤ 5.5V 4.5V ≤ V _{BIAS} ≤ 5.5V | | 1 | | μA |
| ΔV _O /ΔV _{IN} | Output Voltage Line Regulation ⁽²⁾ | V _O (NOM) + 1V ≤ V _{IN} ≤ 5.5V | | 0.01 | | %/V |
| ΔV _O /ΔI _L | Output Voltage Load Regulation ⁽³⁾ | 10 mA < I _L < 0.8A | | 0.1 | 0.4 1.3 | %/A |
| V _{DO} | Dropout Voltage ⁽⁴⁾ | I _L = 0.8A | | 75 | 120 205 | mV |

- (1) Typical numbers represent the most likely parametric norm for 25°C operation.
- (2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
- (3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
- (4) Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $V_{BIAS} = 4.5\text{V}$, $I_L = 10\text{mA}$, $C_{IN} = 10\text{ }\mu\text{F CER}$, $C_{OUT} = 22\text{ }\mu\text{F CER}$, $V_{S/D} = V_{BIAS}$. Min/Max limits are specified through testing, statistical correlation, or design.

| Symbol | Parameter | Conditions | MIN | TYP ⁽¹⁾ | MAX | Units |
|-----------------------|--|--|------------|--------------------|------------------------|------------------------------|
| $I_Q(V_{IN})$ | Quiescent Current Drawn from V_{IN} Supply | $10\text{ mA} < I_L < 0.8\text{A}$ | | 30 | 35 40 | mA |
| | | $\overline{V_{S/D}} \leq 0.3\text{V}$ | | 0.06 | 1 30 | μA |
| $I_Q(V_{BIAS})$ | Quiescent Current Drawn from V_{BIAS} Supply | $10\text{ mA} < I_L < 0.8\text{A}$ | | 2 | 4 6 | mA |
| | | $\overline{V_{S/D}} \leq 0.3\text{V}$ | | 0.03 | 1 30 | μA |
| UVLO | V_{BIAS} Voltage Where Regulator Output Is Enabled | | | 3.8 | | V |
| I_{SC} | Short-Circuit Current | $V_{OUT} = 0\text{V}$ | | 2.6 | | A |
| Shutdown Input | | | | | | |
| V_{SDT} | Output Turn-off Threshold | Output = ON | | 0.7 | 1.3 | V |
| | | Output = OFF | 0.3 | 0.7 | | |
| $T_d(\text{OFF})$ | Turn-OFF Delay | $R_{LOAD} \times C_{OUT} \ll T_d(\text{OFF})$ | | 20 | | μs |
| $T_d(\text{ON})$ | Turn-ON Delay | $R_{LOAD} \times C_{OUT} \ll T_d(\text{ON})$ | | 15 | | |
| $I_{S/D}$ | $\overline{S/D}$ Input Current | $\overline{V_{S/D}} = 1.3\text{V}$ | | 1 | | μA |
| | | $\overline{V_{S/D}} \leq 0.3\text{V}$ | | -1 | | |
| θ_{JA} | Junction to Ambient Thermal Resistance | SO-8 Package ⁽⁵⁾ | | 43 | | $^\circ\text{C/W}$ |
| AC Parameters | | | | | | |
| PSRR (V_{IN}) | Ripple Rejection for V_{IN} Input Voltage | $V_{IN} = V_{OUT} + 1\text{V}$, $f = 120\text{ Hz}$ | | 80 | | dB |
| | | $V_{IN} = V_{OUT} + 1\text{V}$, $f = 1\text{ kHz}$ | | 65 | | |
| PSRR (V_{BIAS}) | Ripple Rejection for V_{BIAS} Voltage | $V_{BIAS} = V_{OUT} + 3\text{V}$, $f = 120\text{ Hz}$ | | 58 | | |
| | | $V_{BIAS} = V_{OUT} + 3\text{V}$, $f = 1\text{ kHz}$ | | 58 | | |
| | Output Noise Density | $f = 120\text{ Hz}$ | | 1 | | $\mu\text{V}/\text{root-Hz}$ |
| e_n | Output Noise Voltage $V_{OUT} = 1.5\text{V}$ | $\text{BW} = 10\text{ Hz} - 100\text{ kHz}$ | | 150 | | $\mu\text{V (rms)}$ |
| | | $\text{BW} = 300\text{ Hz} - 300\text{ kHz}$ | | 90 | | |

(5) For optimum heat dissipation, the exposed DAP on the bottom of the SO package must be soldered to a copper plane or connected using thermal vias to an internal copper plane.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_J = 25^\circ\text{C}$, $C_{IN} = 10\ \mu\text{F CER}$, $C_{OUT} = 22\ \mu\text{F CER}$, $C_{BIAS} = 1\ \mu\text{F CER}$, $\overline{\text{S/D}}$ Pin is tied to V_{BIAS} , $V_{OUT} = 1.2\text{V}$, $I_L = 10\text{mA}$, $V_{BIAS} = 5\text{V}$, $V_{IN} = V_{OUT} + 1\text{V}$.

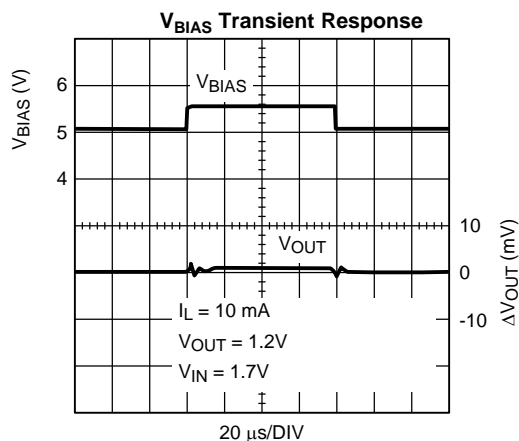


Figure 2.

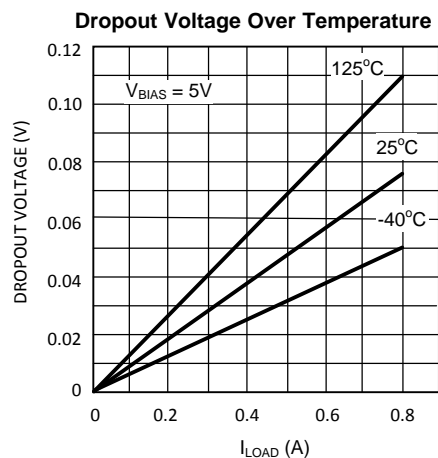


Figure 3.

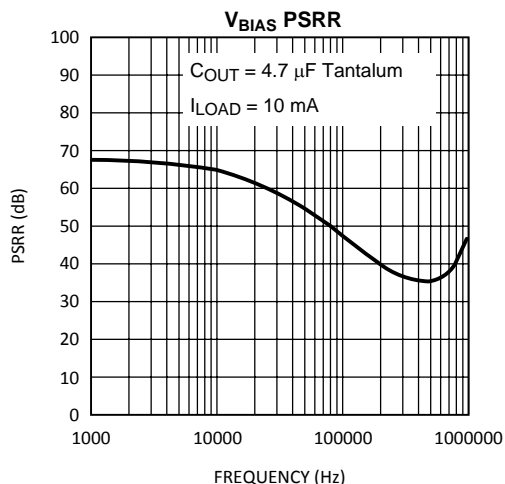


Figure 4.

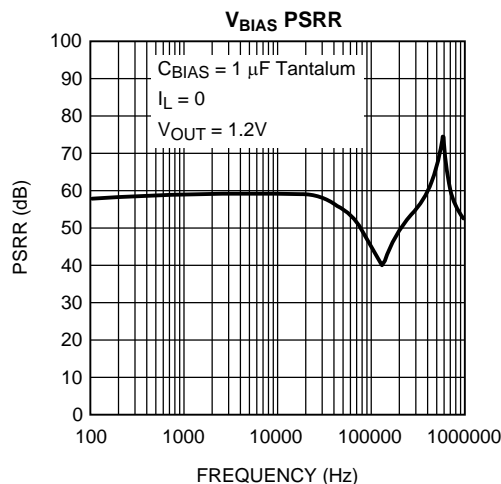


Figure 5.

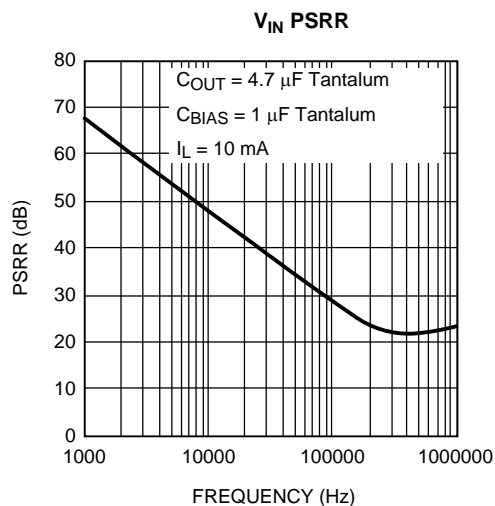


Figure 6.

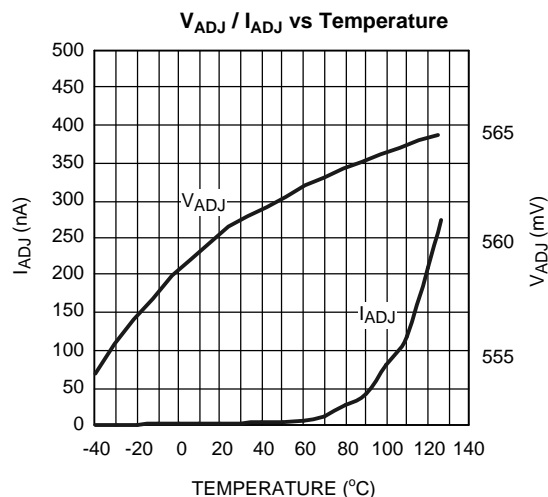


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J = 25^\circ\text{C}$, $C_{IN} = 10\ \mu\text{F CER}$, $C_{OUT} = 22\ \mu\text{F CER}$, $C_{BIAS} = 1\ \mu\text{F CER}$, $\overline{\text{S/D}}$ Pin is tied to V_{BIAS} , $V_{OUT} = 1.2\text{V}$, $I_L = 10\text{mA}$, $V_{BIAS} = 5\text{V}$, $V_{IN} = V_{OUT} + 1\text{V}$.

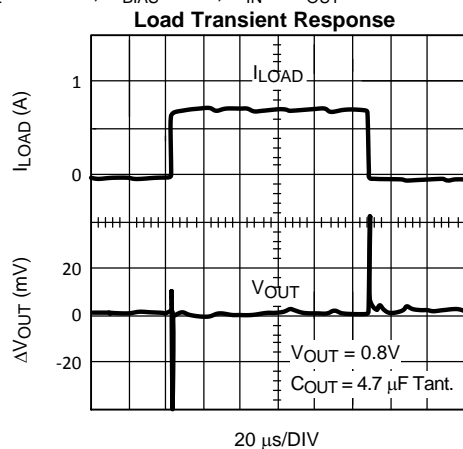


Figure 8.

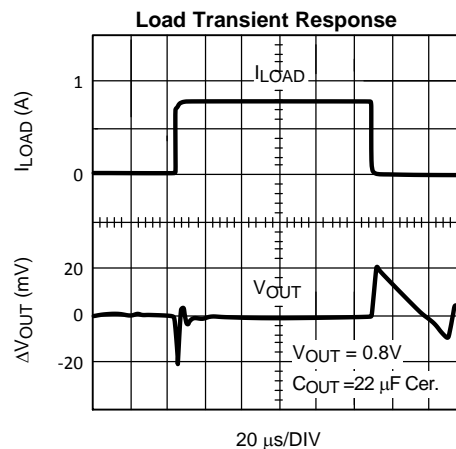


Figure 9.

APPLICATION HINTS

SETTING THE OUTPUT VOLTAGE

(Refer to [Typical Application Circuit](#))

The output voltage is set using the resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + R1 / R2) \quad (1)$$

The value of R2 must be 10k or less for proper operation.

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the [Typical Application Circuit](#).

OUTPUT CAPACITOR

An output capacitor is required on the LP3884X devices for loop stability. The minimum value of capacitance necessary depends on type of capacitor: if a solid Tantalum capacitor is used, the part is stable with capacitor values as low as 4.7µF. If a ceramic capacitor is used, a minimum of 22 µF of capacitance must be used (capacitance may be increased without limit). The reason a larger ceramic capacitor is required is that the output capacitor sets a pole which limits the loop bandwidth. The Tantalum capacitor has a higher ESR than the ceramic which provides more phase margin to the loop, thereby allowing the use of a smaller output capacitor because adequate phase margin can be maintained out to a higher crossover frequency. The tantalum capacitor will typically also provide faster settling time on the output after a fast changing load transient occurs, but the ceramic capacitor is superior for bypassing high frequency noise.

The output capacitor must be located less than one centimeter from the output pin and returned to a clean analog ground. Care must be taken in choosing the output capacitor to ensure that sufficient capacitance is provided over the full operating temperature range. If ceramics are selected, only X7R or X5R types may be used because Z5U and Y5F types suffer severe loss of capacitance with temperature and applied voltage and may only provide 20% of their rated capacitance in operation.

INPUT CAPACITOR

The input capacitor is also critical to loop stability because it provides a low source impedance for the regulator. The minimum required input capacitance is 10 µF ceramic (Tantalum not recommended). The value of C_{IN} may be increased without limit. As stated above, X5R or X7R must be used to ensure sufficient capacitance is provided. The input capacitor must be located less than one centimeter from the input pin and returned to a clean analog ground.

FEED FORWARD CAPACITOR

(Refer to [Typical Application Circuit](#))

A capacitor placed across R1 can provide some additional phase margin and improve transient response. The capacitor C_{FF} and R1 form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (2)$$

For best effect, select C_{FF} so the zero frequency is approximately 70 kHz. The phase lead provided by C_{FF} drops as the output voltage gets closer to 0.56V (and R1 reduces in value). The reason is that C_{FF} also forms a pole whose frequency is given by:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times R1 // R2) \quad (3)$$

As R1 reduces, the two equations come closer to being equal and the pole and zero begin to cancel each other out which removes the beneficial phase lead of the zero.

BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 5.5V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 3.8V.

SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. The $\overline{S/D}$ pin must be actively terminated through a pull-up resistor (10 k Ω to 100 k Ω) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

POWER DISSIPATION/HEATSINKING

Heatsinking for the SO-8 package is accomplished by allowing heat to flow through the exposed DAP on the bottom of the package into the copper on the PC board. The exposed DAP must be soldered down to a copper plane to get good heat transfer. It can also be connected through thermal vias to internal copper planes. Since the DAP is physically connected to the backside of the die, it must be held at ground potential. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LP38841MR-ADJ | ACTIVE | SO PowerPAD | DDA | 8 | 95 | TBD | Call TI | Call TI | -40 to 125 | L38841 MRADJ | Samples |
| LP38841MR-ADJ/NOPB | ACTIVE | SO PowerPAD | DDA | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L38841 MRADJ | Samples |
| LP38841MRX-ADJ | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | TBD | Call TI | Call TI | -40 to 125 | L38841 MRADJ | Samples |
| LP38841MRX-ADJ/NOPB | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L38841 MRADJ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

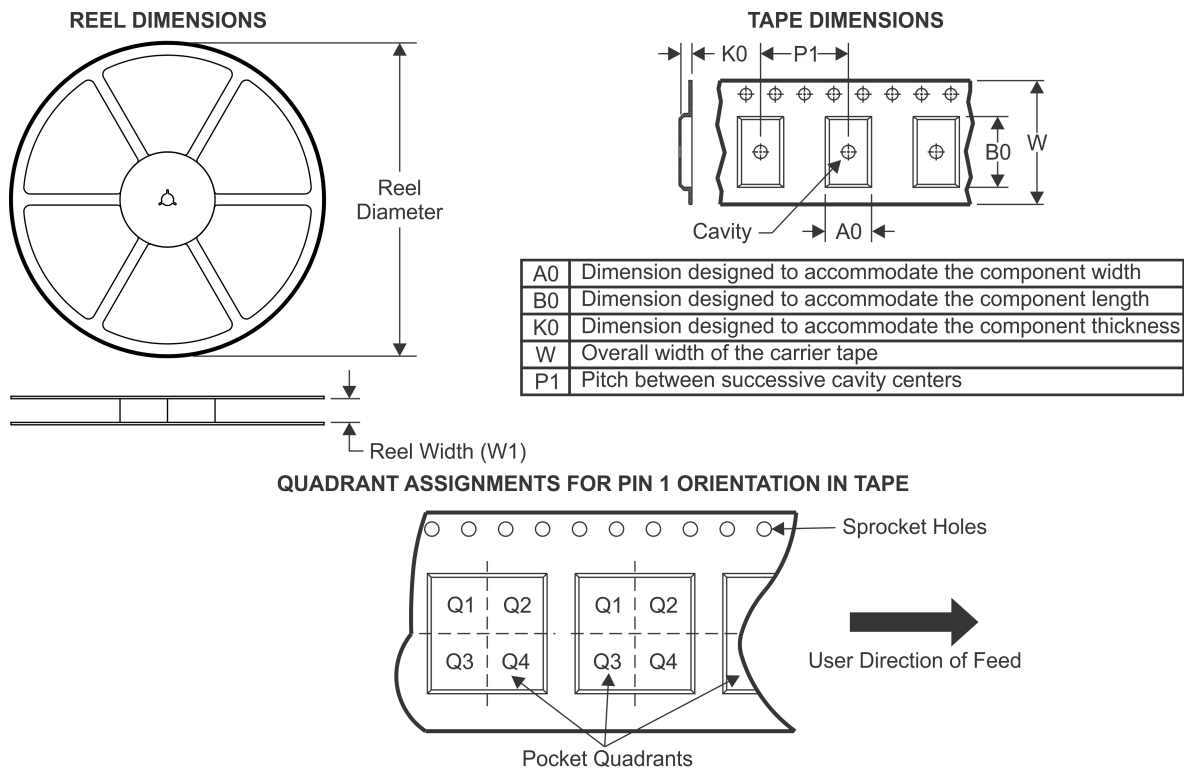
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP38841MRX-ADJ | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP38841MRX-ADJ/NOPB | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

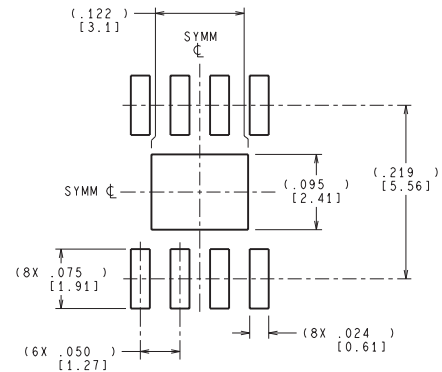
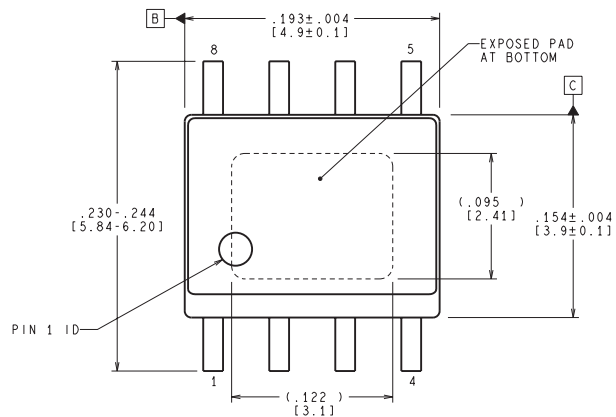
TAPE AND REEL BOX DIMENSIONS



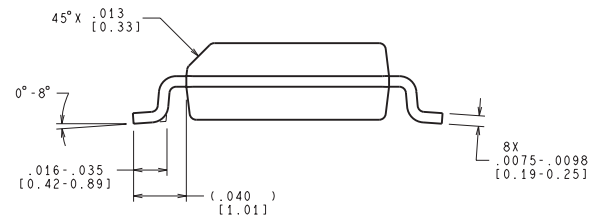
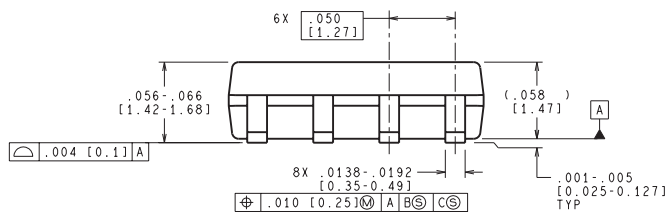
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP38841MRX-ADJ | SO PowerPAD | DDA | 8 | 2500 | 358.0 | 343.0 | 63.0 |
| LP38841MRX-ADJ/NOPB | SO PowerPAD | DDA | 8 | 2500 | 358.0 | 343.0 | 63.0 |

DDA0008B



RECOMMENDED LAND PATTERN



CONTROLLING DIMENSION IS INCH
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MRA08B (Rev B)

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