

# SN54LV4066A, SN74LV4066A QUADRUPLE BILATERAL ANALOG SWITCHES

SCLS4271 – APRIL 1999 – REVISED APRIL 2005

- 2-V to 5.5-V  $V_{CC}$  Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## description/ordering information

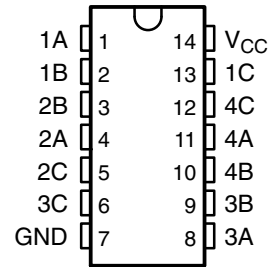
This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V  $V_{CC}$  operation.

These switches are designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

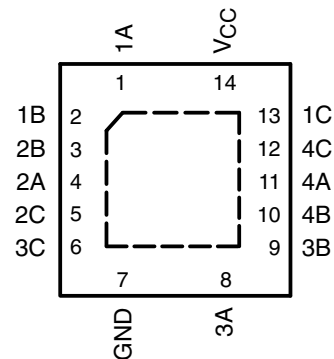
Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

SN54LV4066A . . . J OR W PACKAGE  
SN74LV4066A . . . D, DB, DGV, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN74LV4066A . . . RGY PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| $T_A$          | PACKAGE†    |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------|--------------|-----------------------|------------------|
| –40°C to 85°C  | PDIP – N    | Tube of 25   | SN74LV4066AN          | SN74LV4066AN     |
|                | QFN – RGY   | Reel of 1000 | SN74LV4066ARGYR       | LW066A           |
|                | SOIC – D    | Tube of 50   | SN74LV4066AD          | LV4066A          |
|                |             | Reel of 2500 | SN74LV4066ADR         |                  |
|                | SOP – NS    | Reel of 2000 | SN74LV4066ANSR        | 74LV4066A        |
|                | SSOP – DB   | Reel of 2000 | SN74LV4066ADBR        | LW066A           |
|                | TSSOP – PW  | Tube of 90   | SN74LV4066APW         | LW066A           |
|                |             | Reel of 2000 | SN74LV4066APWR        |                  |
|                |             | Reel of 250  | SN74LV4066APWT        |                  |
|                | TVSOP – DGV | Reel of 2000 | SN74LV4066ADGVR       | LW066A           |
| –55°C to 125°C | CDIP – J    | Tube of 25   | SNJ54LV4066AJ         | SNJ54LV4066AJ    |
|                | CFP – W     | Tube of 150  | SNJ54LV4066AW         | SNJ54LV4066AW    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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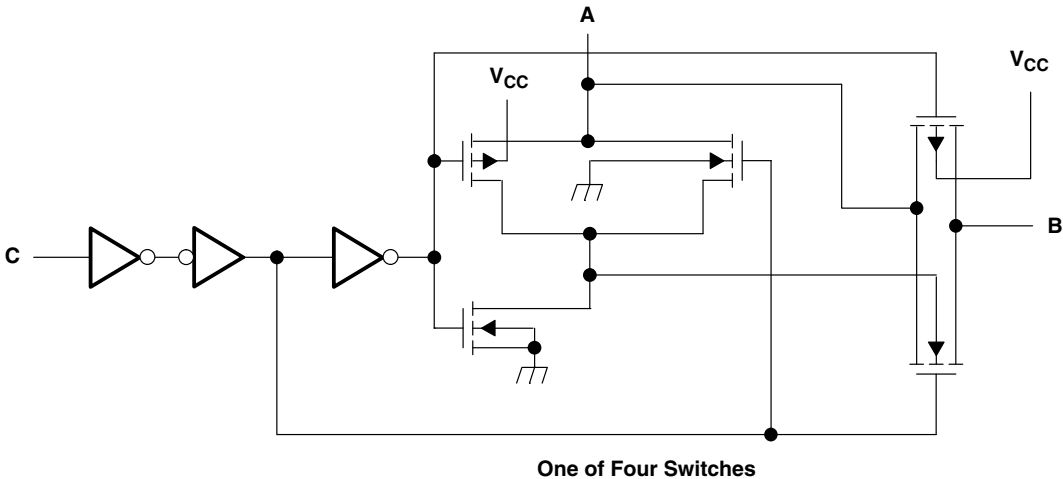
SN54LV4066A, SN74LV4066A  
QUADRUPLE BILATERAL ANALOG SWITCHES

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FUNCTION TABLE  
(each switch)

| INPUT<br>CONTROL<br>(C) | SWITCH |
|-------------------------|--------|
| L                       | OFF    |
| H                       | ON     |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                  |                            |
|------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$ (see Note 1)                      | -0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                          | -0.5 V to 7 V              |
| Switch I/O voltage range, $V_{IO}$ (see Notes 1 and 2)           | -0.5 V to $V_{CC} + 0.5$ V |
| Control-input clamp current, $I_{IK}$ ( $V_I < 0$ )              | -20 mA                     |
| I/O diode current, $I_{IOK}$ ( $V_{IO} < 0$ )                    | -50 mA                     |
| On-state switch current, $I_T$ ( $V_{IO} = 0$ to $V_{CC}$ )      | $\pm 25$ mA                |
| Continuous current through $V_{CC}$ or GND                       | $\pm 50$ mA                |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package | 86°C/W                     |
| (see Note 3): DB package                                         | 96°C/W                     |
| (see Note 3): DGV package                                        | 127°C/W                    |
| (see Note 3): N package                                          | 80°C/W                     |
| (see Note 3): NS package                                         | 76°C/W                     |
| (see Note 3): PW package                                         | 113°C/W                    |
| (see Note 4): RGY package                                        | 47°C/W                     |
| Storage temperature range, $T_{stg}$                             | -65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.  
4. The package thermal impedance is calculated in accordance with JESD 51-5.

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## recommended operating conditions (see Note 5)

|                 |                                          |                                  | SN54LV4066A           |                 | SN74LV4066A           |                 | UNIT |
|-----------------|------------------------------------------|----------------------------------|-----------------------|-----------------|-----------------------|-----------------|------|
|                 |                                          |                                  | MIN                   | MAX             | MIN                   | MAX             |      |
| V <sub>CC</sub> | Supply voltage                           |                                  | 2†                    | 5.5             | 2†                    | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage, control inputs | V <sub>CC</sub> = 2 V            | 1.5                   |                 | 1.5                   |                 | V    |
|                 |                                          | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                 | V <sub>CC</sub> × 0.7 |                 |      |
|                 |                                          | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                 | V <sub>CC</sub> × 0.7 |                 |      |
|                 |                                          | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                 | V <sub>CC</sub> × 0.7 |                 |      |
| V <sub>IL</sub> | Low-level input voltage, control inputs  | V <sub>CC</sub> = 2 V            | 0.5                   |                 | 0.5                   |                 | V    |
|                 |                                          | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.3 |                 | V <sub>CC</sub> × 0.3 |                 |      |
|                 |                                          | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.3 |                 | V <sub>CC</sub> × 0.3 |                 |      |
|                 |                                          | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.3 |                 | V <sub>CC</sub> × 0.3 |                 |      |
| V <sub>I</sub>  | Control input voltage                    |                                  | 0                     | 5.5             | 0                     | 5.5             | V    |
| V <sub>IO</sub> | Input/output voltage                     |                                  | 0                     | V <sub>CC</sub> | 0                     | V <sub>CC</sub> | V    |
| Δt/Δv           | Input transition rise or fall rate       | V <sub>CC</sub> = 2.3 V to 2.7 V | 200                   |                 | 200                   |                 | ns/V |
|                 |                                          | V <sub>CC</sub> = 3 V to 3.6 V   | 100                   |                 | 100                   |                 |      |
|                 |                                          | V <sub>CC</sub> = 4.5 V to 5.5 V | 20                    |                 | 20                    |                 |      |
| T <sub>A</sub>  | Operating free-air temperature           |                                  | −55                   | 125             | −40                   | 85              | °C   |

<sup>†</sup> With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                           | TEST CONDITIONS                                                                                                                                                           | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | SN54LV4066A |     | SN74LV4066A |     | UNIT |
|---------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------------|-----|------|-------------|-----|-------------|-----|------|
|                                                                     |                                                                                                                                                                           |                 | MIN                   | TYP | MAX  | MIN         | MAX | MIN         | MAX |      |
| r <sub>on</sub> On-state switch resistance                          | I <sub>T</sub> = –1 mA,<br>V <sub>I</sub> = V <sub>CC</sub> or GND,<br>V <sub>C</sub> = V <sub>IH</sub><br>(see Figure 1)                                                 | 2.3 V           |                       | 38  | 180  |             | 225 |             | 225 | Ω    |
|                                                                     |                                                                                                                                                                           | 3 V             |                       | 29  | 150  |             | 190 |             | 190 |      |
|                                                                     |                                                                                                                                                                           | 4.5 V           |                       | 21  | 75   |             | 100 |             | 100 |      |
| r <sub>on(p)</sub> Peak on-state resistance                         | I <sub>T</sub> = –1 mA,<br>V <sub>I</sub> = V <sub>CC</sub> to GND,<br>V <sub>C</sub> = V <sub>IH</sub>                                                                   | 2.3 V           |                       | 143 | 500  |             | 600 |             | 600 | Ω    |
|                                                                     |                                                                                                                                                                           | 3 V             |                       | 57  | 180  |             | 225 |             | 225 |      |
|                                                                     |                                                                                                                                                                           | 4.5 V           |                       | 31  | 100  |             | 125 |             | 125 |      |
| Δr <sub>on</sub> Difference in on-state resistance between switches | I <sub>T</sub> = –1 mA,<br>V <sub>I</sub> = V <sub>CC</sub> to GND,<br>V <sub>C</sub> = V <sub>IH</sub>                                                                   | 2.3 V           |                       | 6   | 30   |             | 40  |             | 40  | Ω    |
|                                                                     |                                                                                                                                                                           | 3 V             |                       | 3   | 20   |             | 30  |             | 30  |      |
|                                                                     |                                                                                                                                                                           | 4.5 V           |                       | 2   | 15   |             | 20  |             | 20  |      |
| I <sub>I</sub> Control input current                                | V <sub>I</sub> = 5.5 V or GND                                                                                                                                             | 0 to 5.5 V      |                       |     | ±0.1 |             | ±1  |             | ±1  | μA   |
| I <sub>S(off)</sub> Off-state switch leakage current                | V <sub>I</sub> = V <sub>CC</sub> and V <sub>O</sub> = GND, or V <sub>I</sub> = GND and V <sub>O</sub> = V <sub>CC</sub> , V <sub>C</sub> = V <sub>IL</sub> (see Figure 2) | 5.5 V           |                       |     | ±0.1 |             | ±1  |             | ±1  | μA   |
| I <sub>S(on)</sub> On-state switch leakage current                  | V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>C</sub> = V <sub>IH</sub> (see Figure 3)                                                                                  | 5.5 V           |                       |     | ±0.1 |             | ±1  |             | ±1  | μA   |
| I <sub>CC</sub> Supply current                                      | V <sub>I</sub> = V <sub>CC</sub> or GND                                                                                                                                   | 5.5 V           |                       |     |      |             | 20  |             | 20  | μA   |
| C <sub>ic</sub> Control input capacitance                           |                                                                                                                                                                           |                 |                       | 1.5 |      |             |     |             |     | pF   |
| C <sub>io</sub> Switch input/output capacitance                     |                                                                                                                                                                           |                 |                       | 5.5 |      |             |     |             |     | pF   |
| C <sub>F</sub> Feed-through capacitance                             |                                                                                                                                                                           |                 |                       | 0.5 |      |             |     |             |     | pF   |

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# SN54LV4066A, SN74LV4066A QUADRUPLE BILATERAL ANALOG SWITCHES

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)**

| PARAMETER                                           | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST<br>CONDITIONS                                                   | $T_A = 25^\circ\text{C}$ |     |     | SN54LV4066A |     | SN74LV4066A |     | UNIT |
|-----------------------------------------------------|-----------------|----------------|----------------------------------------------------------------------|--------------------------|-----|-----|-------------|-----|-------------|-----|------|
|                                                     |                 |                |                                                                      | MIN                      | TYP | MAX | MIN         | MAX | MIN         | MAX |      |
| $t_{PLH}$<br>$t_{PHL}$<br>Propagation<br>delay time | A or B          | B or A         | $C_L = 15\text{ pF}$ ,<br>(see Figure 4)                             |                          | 1.2 | 10  |             | 16  |             | 16  | ns   |
| $t_{PZH}$<br>$t_{PZL}$<br>Switch<br>turn-on time    | C               | A or B         | $C_L = 15\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 3.3 | 15  |             | 20  |             | 20  | ns   |
| $t_{PLZ}$<br>$t_{PHZ}$<br>Switch<br>turn-off time   | C               | A or B         | $C_L = 15\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 6   | 15  |             | 23  |             | 23  | ns   |
| $t_{PLH}$<br>$t_{PHL}$<br>Propagation<br>delay time | A or B          | B or A         | $C_L = 50\text{ pF}$ ,<br>(see Figure 4)                             |                          | 2.6 | 12  |             | 18  |             | 18  | ns   |
| $t_{PZH}$<br>$t_{PZL}$<br>Switch<br>turn-on time    | C               | A or B         | $C_L = 50\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 4.2 | 25  |             | 32  |             | 32  | ns   |
| $t_{PLZ}$<br>$t_{PHZ}$<br>Switch<br>turn-off time   | C               | A or B         | $C_L = 50\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 9.6 | 25  |             | 32  |             | 32  | ns   |

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)**

| PARAMETER                                           | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST<br>CONDITIONS                                                   | $T_A = 25^\circ\text{C}$ |     |     | SN54LV4066A |     | SN74LV4066A |     | UNIT |
|-----------------------------------------------------|-----------------|----------------|----------------------------------------------------------------------|--------------------------|-----|-----|-------------|-----|-------------|-----|------|
|                                                     |                 |                |                                                                      | MIN                      | TYP | MAX | MIN         | MAX | MIN         | MAX |      |
| $t_{PLH}$<br>$t_{PHL}$<br>Propagation<br>delay time | A or B          | B or A         | $C_L = 15\text{ pF}$ ,<br>(see Figure 4)                             |                          | 0.8 | 6   |             | 10  |             | 10  | ns   |
| $t_{PZH}$<br>$t_{PZL}$<br>Switch<br>turn-on time    | C               | A or B         | $C_L = 15\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 2.3 | 11  |             | 15  |             | 15  | ns   |
| $t_{PLZ}$<br>$t_{PHZ}$<br>Switch<br>turn-off time   | C               | A or B         | $C_L = 15\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 4.5 | 11  |             | 15  |             | 15  | ns   |
| $t_{PLH}$<br>$t_{PHL}$<br>Propagation<br>delay time | A or B          | B or A         | $C_L = 50\text{ pF}$ ,<br>(see Figure 4)                             |                          | 1.5 | 9   |             | 12  |             | 12  | ns   |
| $t_{PZH}$<br>$t_{PZL}$<br>Switch<br>turn-on time    | C               | A or B         | $C_L = 50\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 3   | 18  |             | 22  |             | 22  | ns   |
| $t_{PLZ}$<br>$t_{PHZ}$<br>Switch<br>turn-off time   | C               | A or B         | $C_L = 50\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 7.2 | 18  |             | 22  |             | 22  | ns   |

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# SN54LV4066A, SN74LV4066A QUADRUPLE BILATERAL ANALOG SWITCHES

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)**

| PARAMETER                                        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST<br>CONDITIONS                                                   | $T_A = 25^\circ\text{C}$ |     |     | SN54LV4066A |     | SN74LV4066A |     | UNIT |
|--------------------------------------------------|-----------------|----------------|----------------------------------------------------------------------|--------------------------|-----|-----|-------------|-----|-------------|-----|------|
|                                                  |                 |                |                                                                      | MIN                      | TYP | MAX | MIN         | MAX | MIN         | MAX |      |
| $t_{PLH}$<br>$t_{PHL}$<br>Propagation delay time | A or B          | B or A         | $C_L = 15\text{ pF}$ ,<br>(see Figure 4)                             |                          | 0.3 | 4   |             | 7   |             | 7   | ns   |
| $t_{PZH}$<br>$t_{PZL}$<br>Switch turn-on time    | C               | A or B         | $C_L = 15\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 1.6 | 7   |             | 10  |             | 10  | ns   |
| $t_{PLZ}$<br>$t_{PHZ}$<br>Switch turn-off time   | C               | A or B         | $C_L = 15\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 3.2 | 7   |             | 10  |             | 10  | ns   |
| $t_{PLH}$<br>$t_{PHL}$<br>Propagation delay time | A or B          | B or A         | $C_L = 50\text{ pF}$ ,<br>(see Figure 4)                             |                          | 0.6 | 6   |             | 8   |             | 8   | ns   |
| $t_{PZH}$<br>$t_{PZL}$<br>Switch turn-on time    | C               | A or B         | $C_L = 50\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 2.1 | 12  |             | 16  |             | 16  | ns   |
| $t_{PLZ}$<br>$t_{PHZ}$<br>Switch turn-off time   | C               | A or B         | $C_L = 50\text{ pF}$ ,<br>$R_L = 1\text{ k}\Omega$<br>(see Figure 5) |                          | 5.1 | 12  |             | 16  |             | 16  | ns   |

**analog switch characteristics over operating free-air temperature range (unless otherwise noted)**

| PARAMETER                                        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST<br>CONDITIONS                                                                                                                                | $V_{CC}$                   | $T_A = 25^\circ\text{C}$ |     |     | UNIT |
|--------------------------------------------------|-----------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|--------------------------|-----|-----|------|
|                                                  |                 |                |                                                                                                                                                   |                            | MIN                      | TYP | MAX |      |
| Frequency response<br>(switch on)                | A or B          | B or A         | $C_L = 50\text{ pF}$ , $R_L = 600\text{ }\Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (sine wave)<br>$20\log_{10}(V_O/V_I) = -3\text{ dB}$ (see Figure 6) | 2.3 V                      |                          | 30  |     | MHz  |
|                                                  |                 |                |                                                                                                                                                   | 3 V                        |                          | 35  |     |      |
|                                                  |                 |                |                                                                                                                                                   | 4.5 V                      |                          | 50  |     |      |
| Crosstalk<br>(between any switches)              | A or B          | B or A         | $C_L = 50\text{ pF}$ , $R_L = 600\text{ }\Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7)                                          | 2.3 V                      |                          | -45 |     | dB   |
|                                                  |                 |                |                                                                                                                                                   | 3 V                        |                          | -45 |     |      |
|                                                  |                 |                |                                                                                                                                                   | 4.5 V                      |                          | -45 |     |      |
| Crosstalk<br>(control input to<br>signal output) | C               | A or B         | $C_L = 50\text{ pF}$ , $R_L = 600\text{ }\Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8)                                        | 2.3 V                      |                          | 15  |     | mV   |
|                                                  |                 |                |                                                                                                                                                   | 3 V                        |                          | 20  |     |      |
|                                                  |                 |                |                                                                                                                                                   | 4.5 V                      |                          | 50  |     |      |
| Feed-through attenuation<br>(switch off)         | A or B          | B or A         | $C_L = 50\text{ pF}$ , $R_L = 600\text{ }\Omega$ , $f_{in} = 1\text{ MHz}$<br>(see Figure 9)                                                      | 2.3 V                      |                          | -40 |     | dB   |
|                                                  |                 |                |                                                                                                                                                   | 3 V                        |                          | -40 |     |      |
|                                                  |                 |                |                                                                                                                                                   | 4.5 V                      |                          | -40 |     |      |
| Sine-wave distortion                             | A or B          | B or A         | $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ ,<br>$f_{in} = 1\text{ kHz}$ (sine wave)<br>(see Figure 10)                                      | $V_I = 2\text{ V}_{p-p}$   | 2.3 V                    |     | 0.1 | %    |
|                                                  |                 |                |                                                                                                                                                   | $V_I = 2.5\text{ V}_{p-p}$ | 3 V                      |     | 0.1 |      |
|                                                  |                 |                |                                                                                                                                                   | $V_I = 4\text{ V}_{p-p}$   | 4.5 V                    |     | 0.1 |      |

**operating characteristics,  $T_A = 25^\circ\text{C}$**

| PARAMETER                              | TEST CONDITIONS                            | TYP | UNIT |
|----------------------------------------|--------------------------------------------|-----|------|
| $C_{pd}$ Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 4.5 | pF   |

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PARAMETER MEASUREMENT INFORMATION

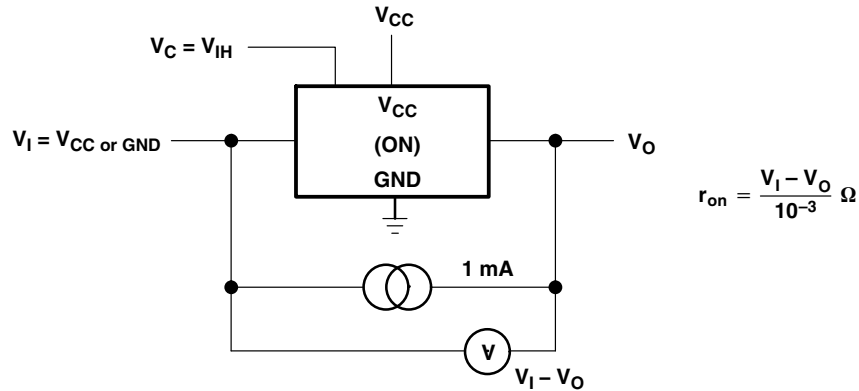


Figure 1. On-State Resistance Test Circuit

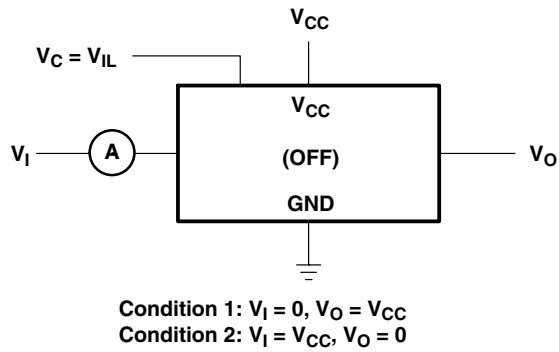


Figure 2. Off-State Switch Leakage-Current Test Circuit

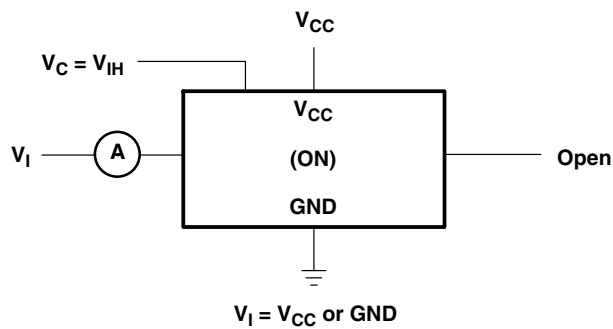


Figure 3. On-State Leakage-Current Test Circuit

SN54LV4066A, SN74LV4066A  
QUADRUPLE BILATERAL ANALOG SWITCHES

SCLS4271 – APRIL 1999 – REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION

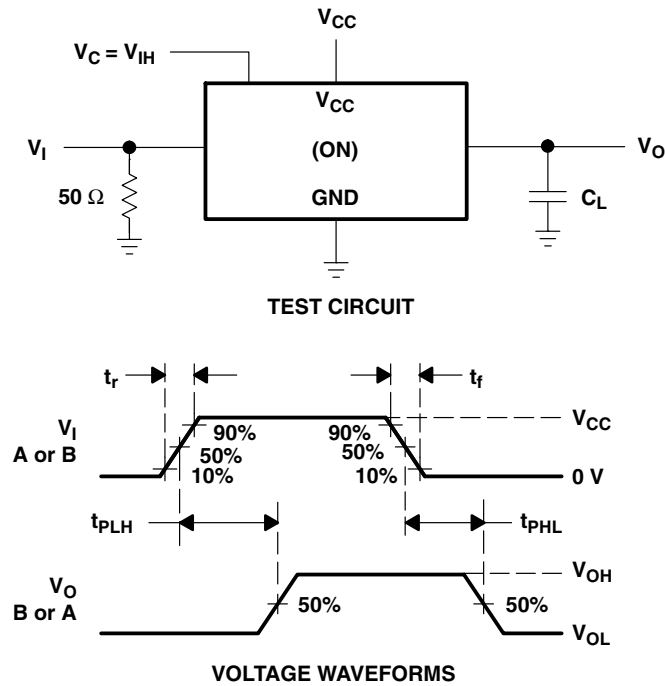
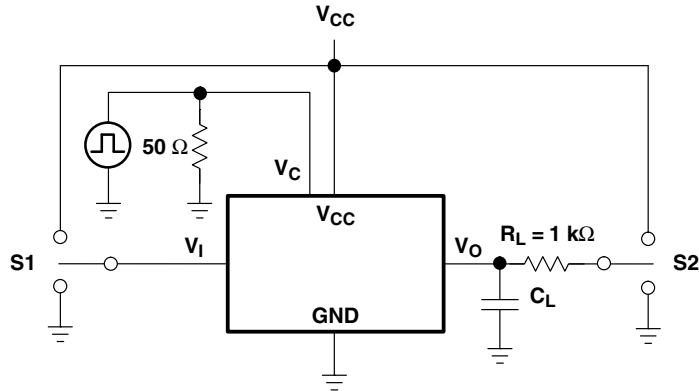


Figure 4. Propagation Delay Time, Signal Input to Signal Output

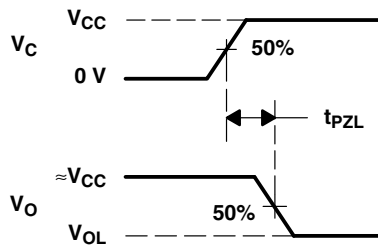


PARAMETER MEASUREMENT INFORMATION

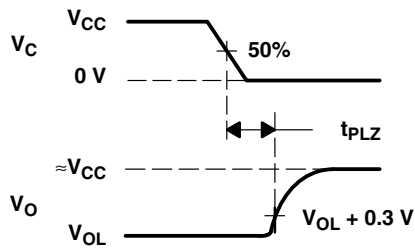
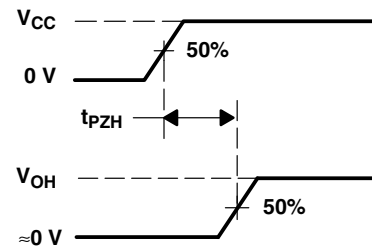


TEST CIRCUIT

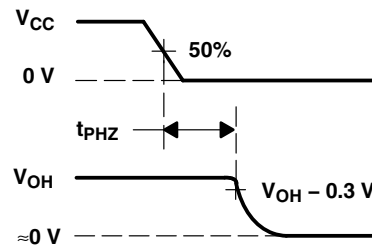
| TEST      | S1       | S2       |
|-----------|----------|----------|
| $t_{PZL}$ | GND      | $V_{CC}$ |
| $t_{PZH}$ | $V_{CC}$ | GND      |
| $t_{PLZ}$ | GND      | $V_{CC}$ |
| $t_{PHZ}$ | $V_{CC}$ | GND      |



( $t_{PZL}$ ,  $t_{PZH}$ )



( $t_{PLZ}$ ,  $t_{PHZ}$ )



VOLTAGE WAVEFORMS

Figure 5. Switching Time ( $t_{PZL}$ ,  $t_{PLZ}$ ,  $t_{PZH}$ ,  $t_{PHZ}$ ), Control to Signal Output

# SN54LV4066A, SN74LV4066A QUADRUPLE BILATERAL ANALOG SWITCHES

SCLS4271 – APRIL 1999 – REVISED APRIL 2005

## PARAMETER MEASUREMENT INFORMATION

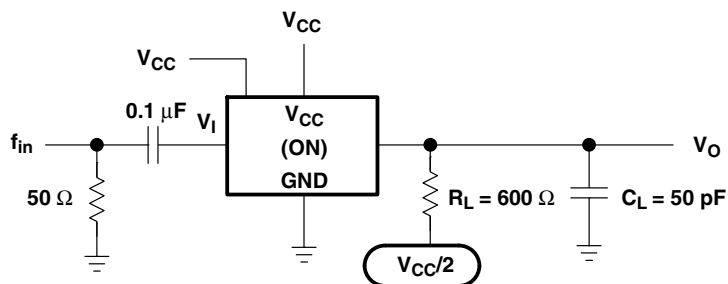


Figure 6. Frequency Response (Switch On)

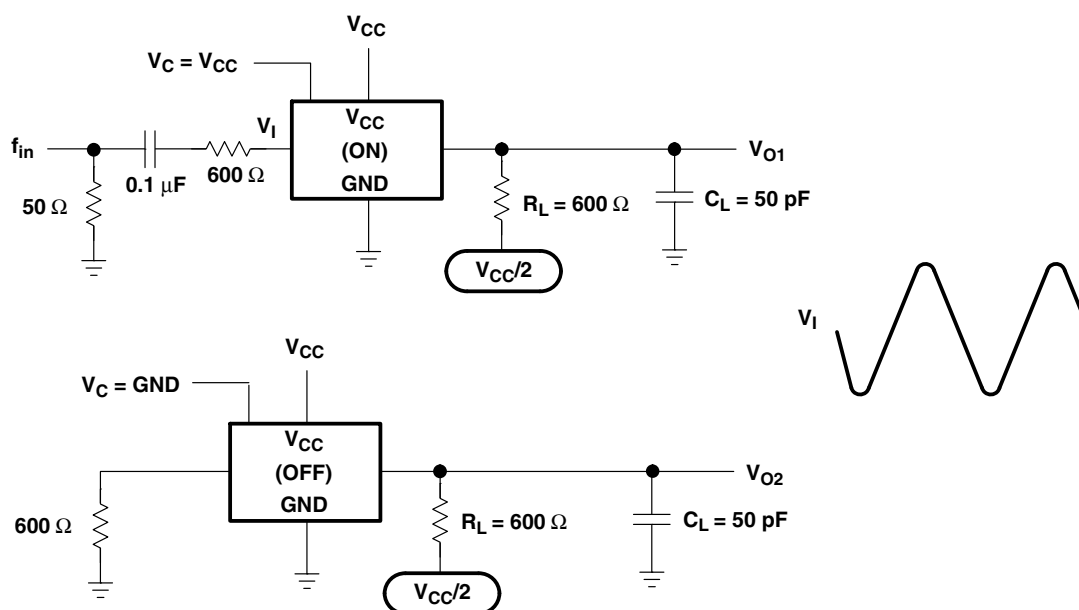


Figure 7. Crosstalk Between Any Two Switches

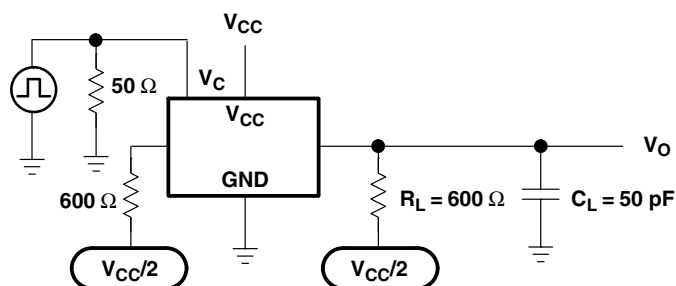


Figure 8. Crosstalk (Control Input – Switch Output)

## PARAMETER MEASUREMENT INFORMATION

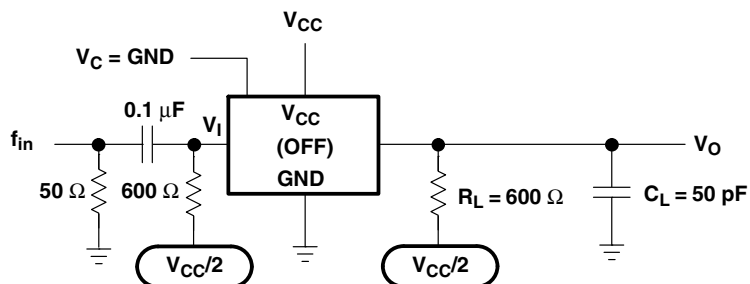


Figure 9. Feed-Through Attenuation (Switch Off)

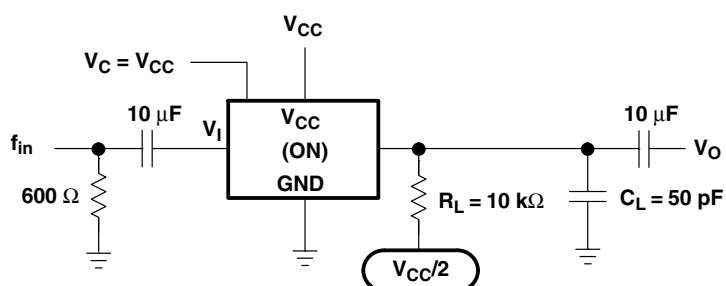


Figure 10. Sine-Wave Distortion

**PACKAGING INFORMATION**

| Orderable Device  | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LV4066AD      | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADBR    | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADBRG4  | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADE4    | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADG4    | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADGVR   | ACTIVE                | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADGVRE4 | ACTIVE                | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADGVRG4 | ACTIVE                | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADR     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADRE4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ADRG4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066AN      | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74LV4066ANE4    | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74LV4066ANSR    | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ANSRE4  | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066ANSRG4  | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APW     | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWE4   | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWG4   | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWR    | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWRE4  | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWRG4  | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWT    | ACTIVE                | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWTE4  | ACTIVE                | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LV4066APWTG4  | ACTIVE                | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

| Orderable Device  | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LV4066ARGYR   | ACTIVE                | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| SN74LV4066ARGYRG4 | ACTIVE                | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

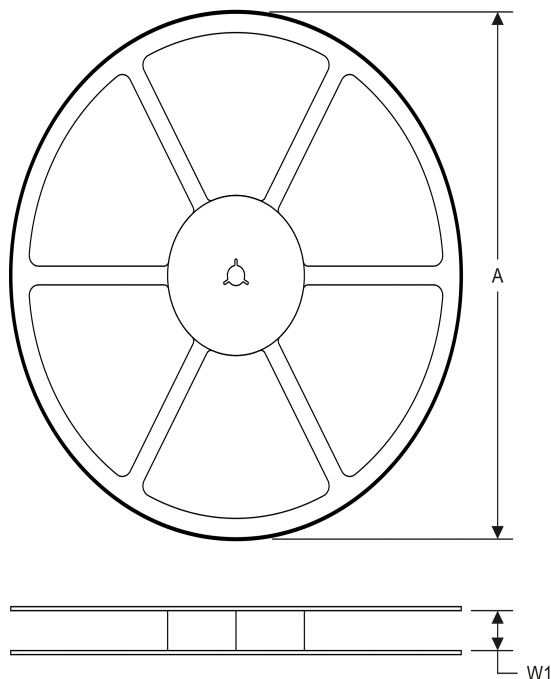
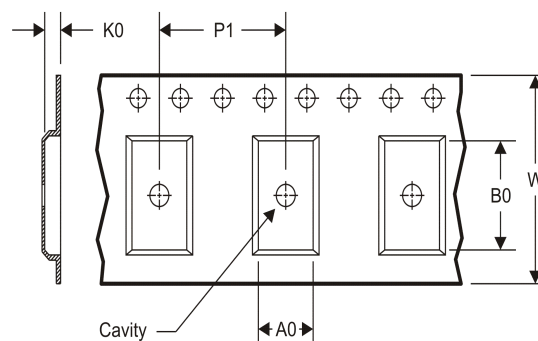
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


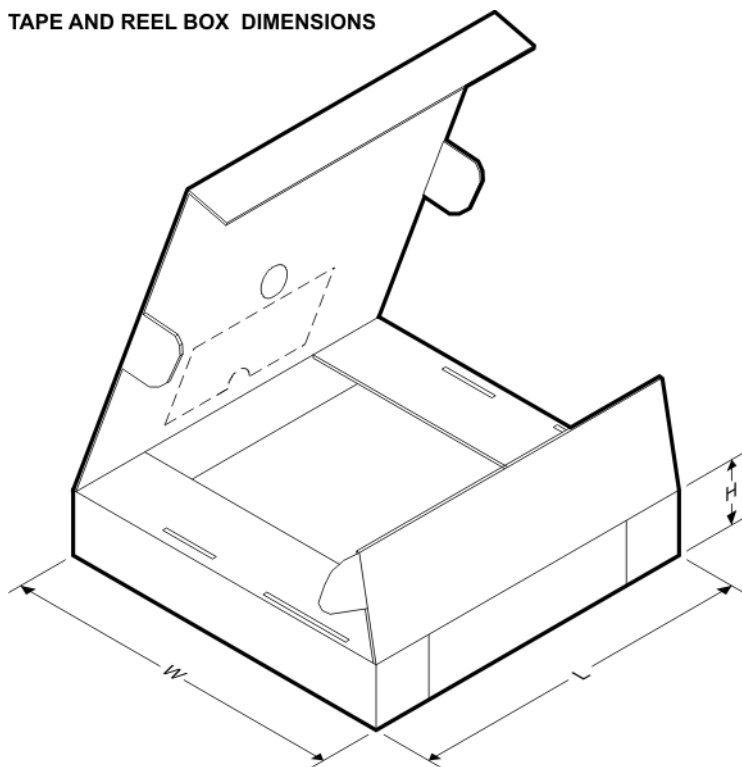
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV4066ADBR  | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 6.6     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV4066ADGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV4066ADR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV4066ANSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV4066APWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV4066APWT  | TSSOP        | PW              | 14   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV4066ARGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



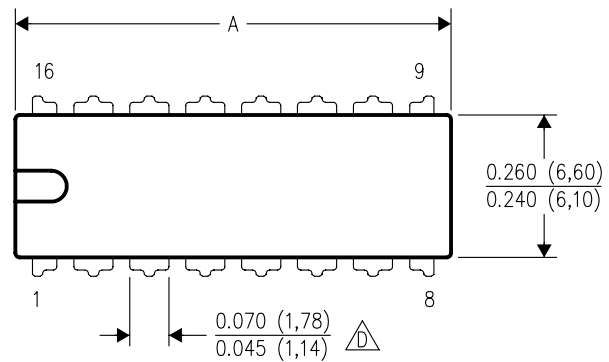
\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV4066ADBR  | SSOP         | DB              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LV4066ADGVR | TVSOP        | DGV             | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LV4066ADR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74LV4066ANSR  | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LV4066APWR  | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LV4066APWT  | TSSOP        | PW              | 14   | 250  | 367.0       | 367.0      | 35.0        |
| SN74LV4066ARGYR | VQFN         | RGY             | 14   | 3000 | 367.0       | 367.0      | 35.0        |

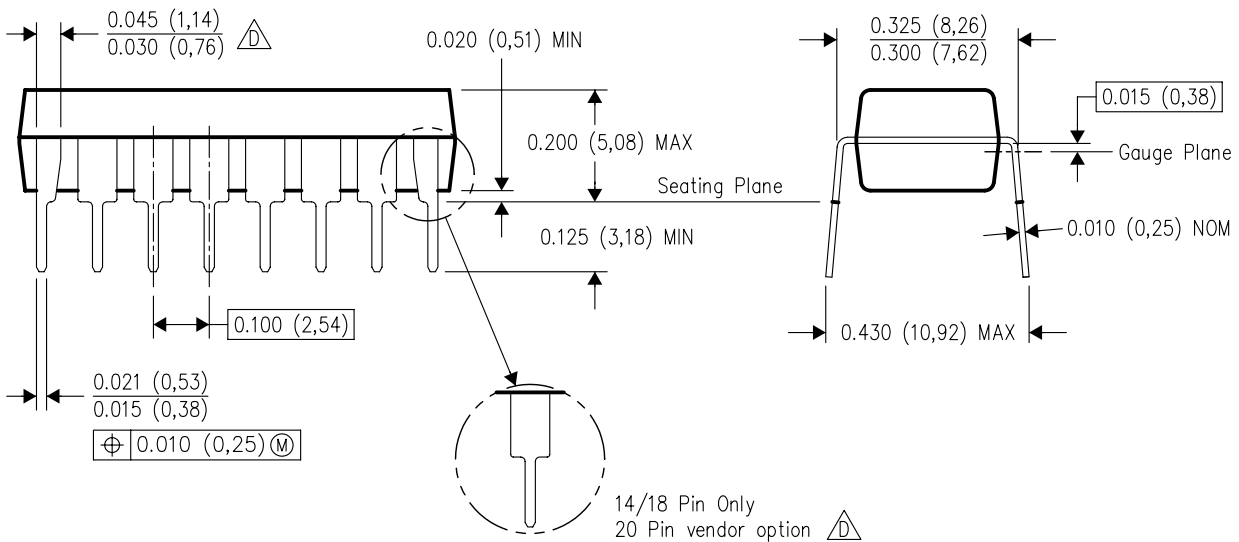
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

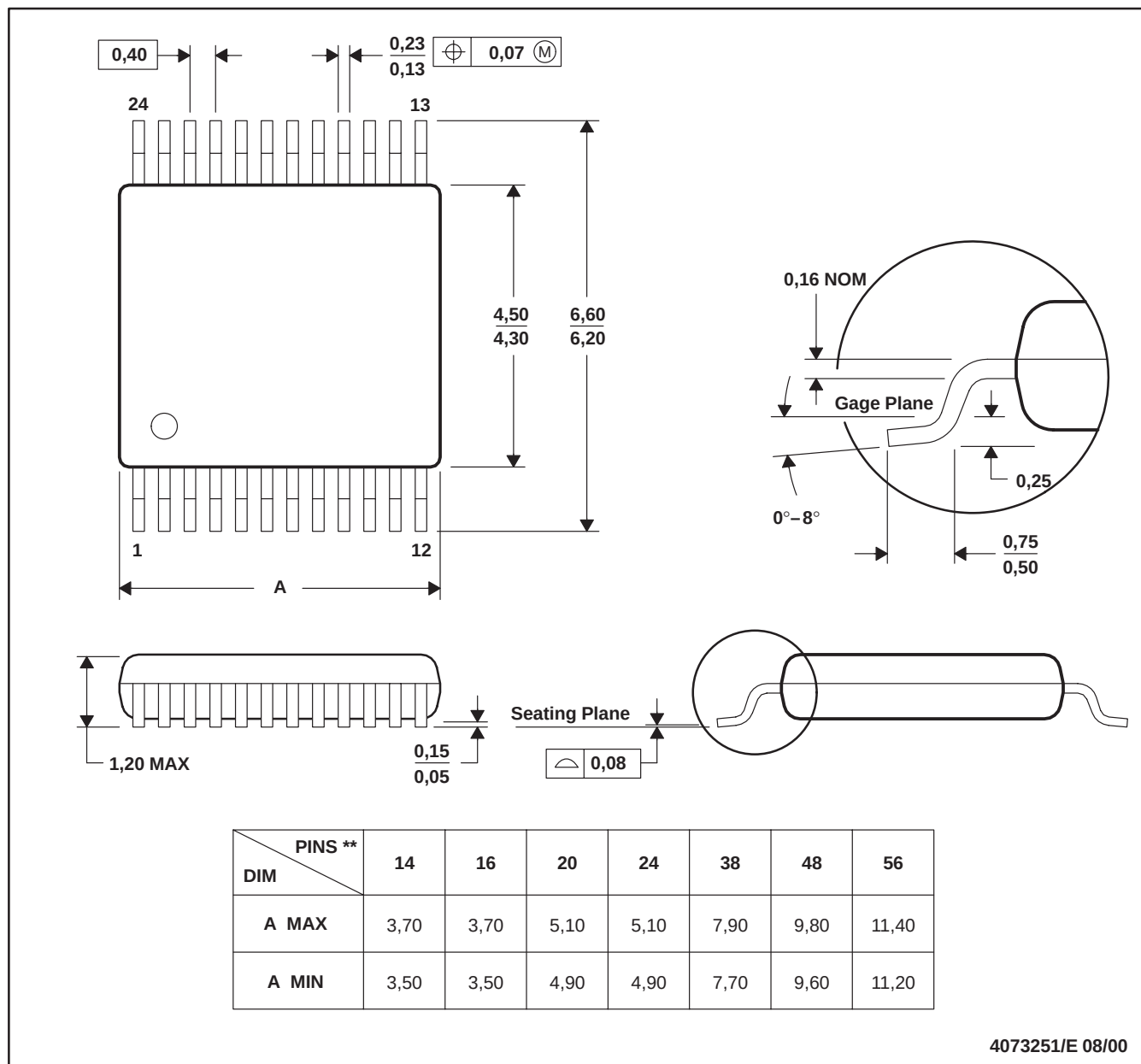
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

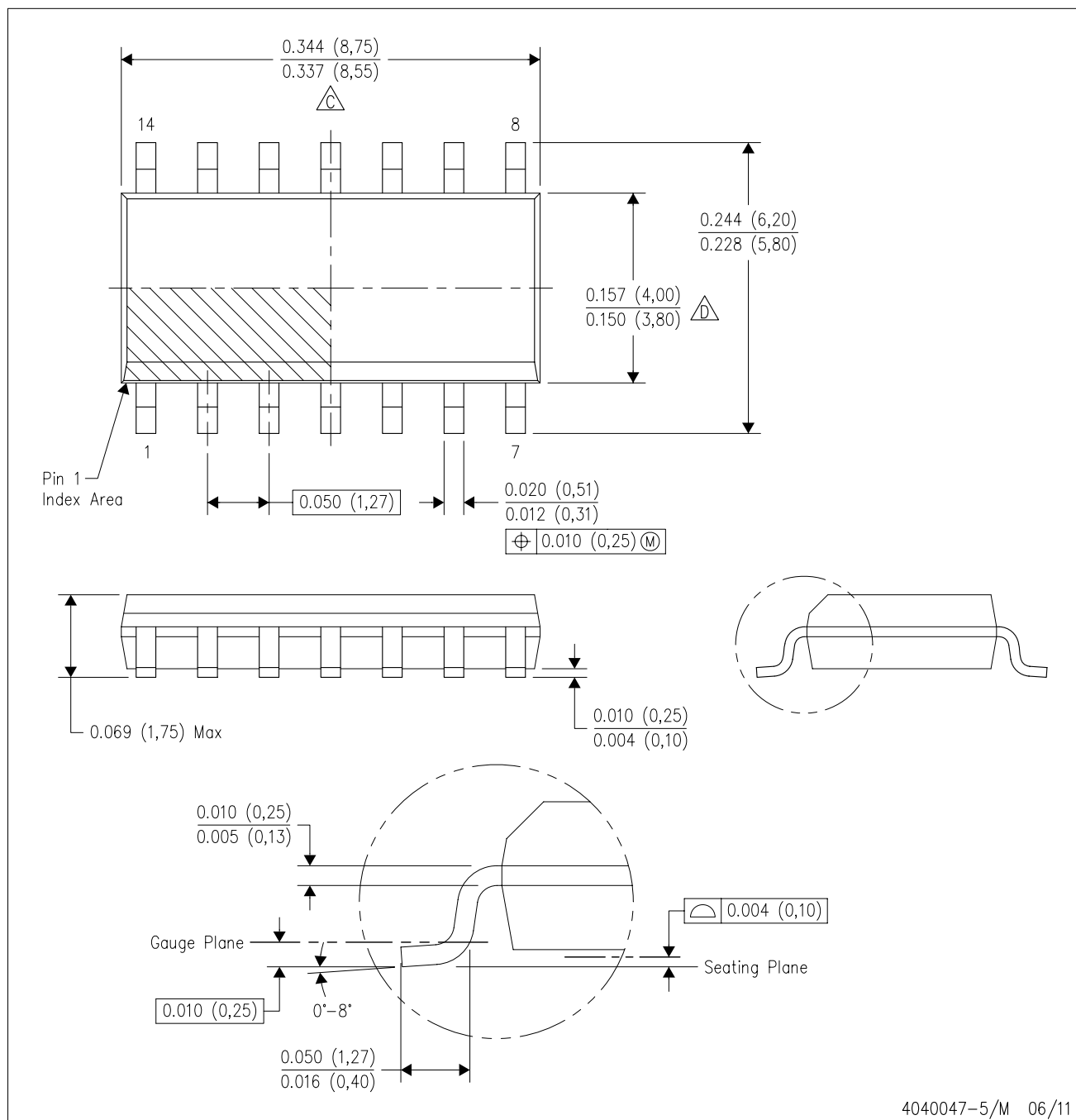
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

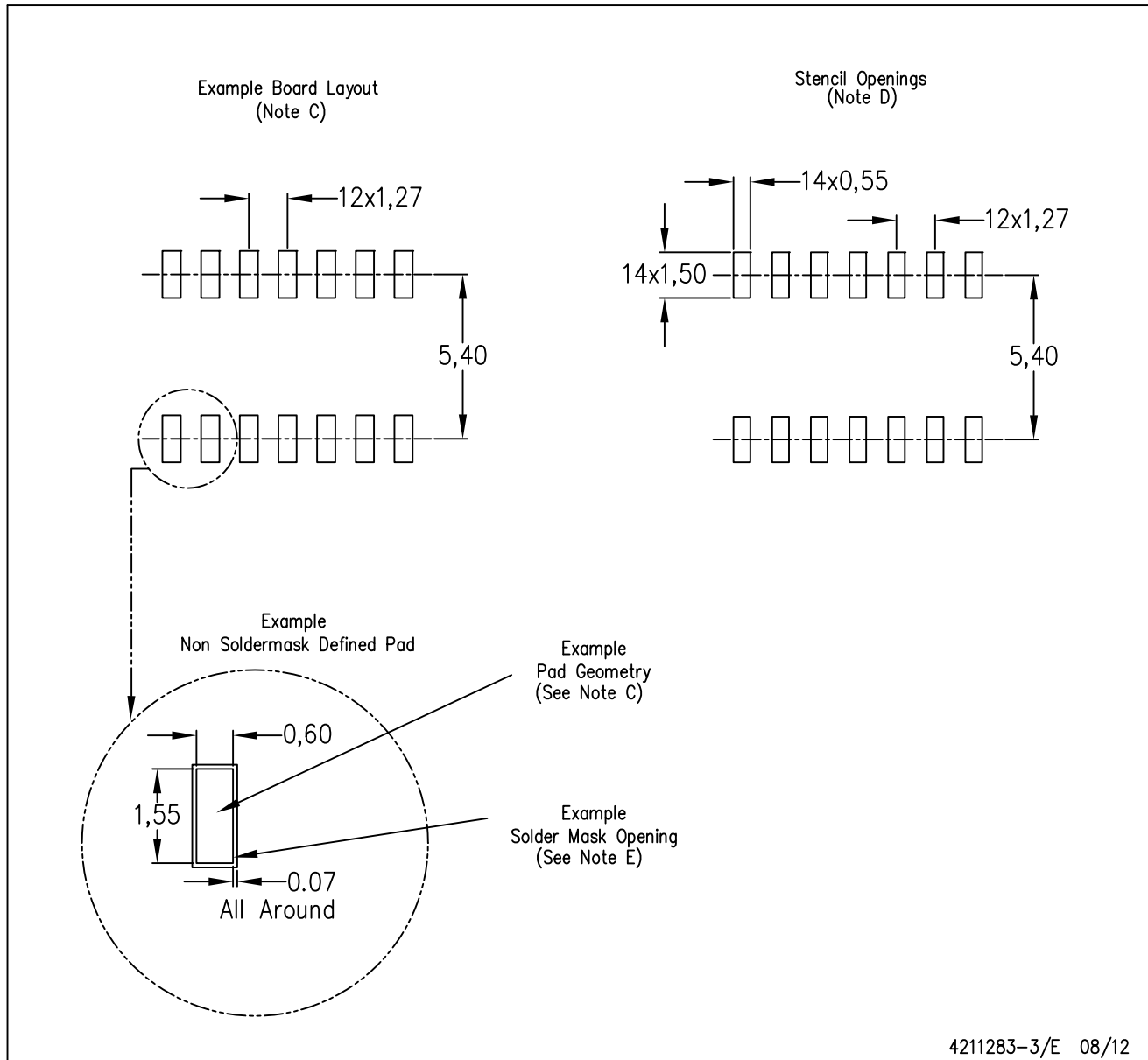


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

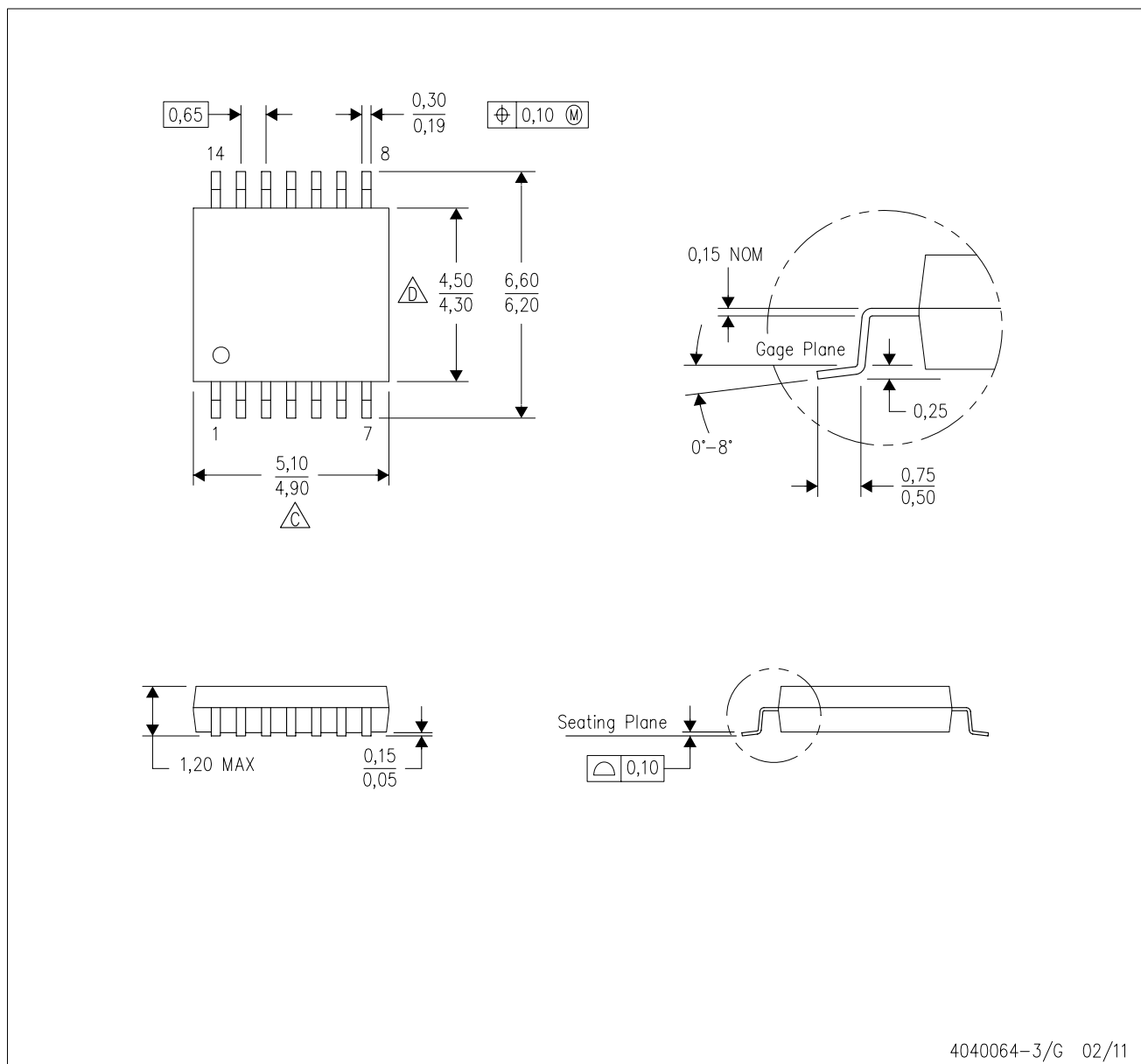
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

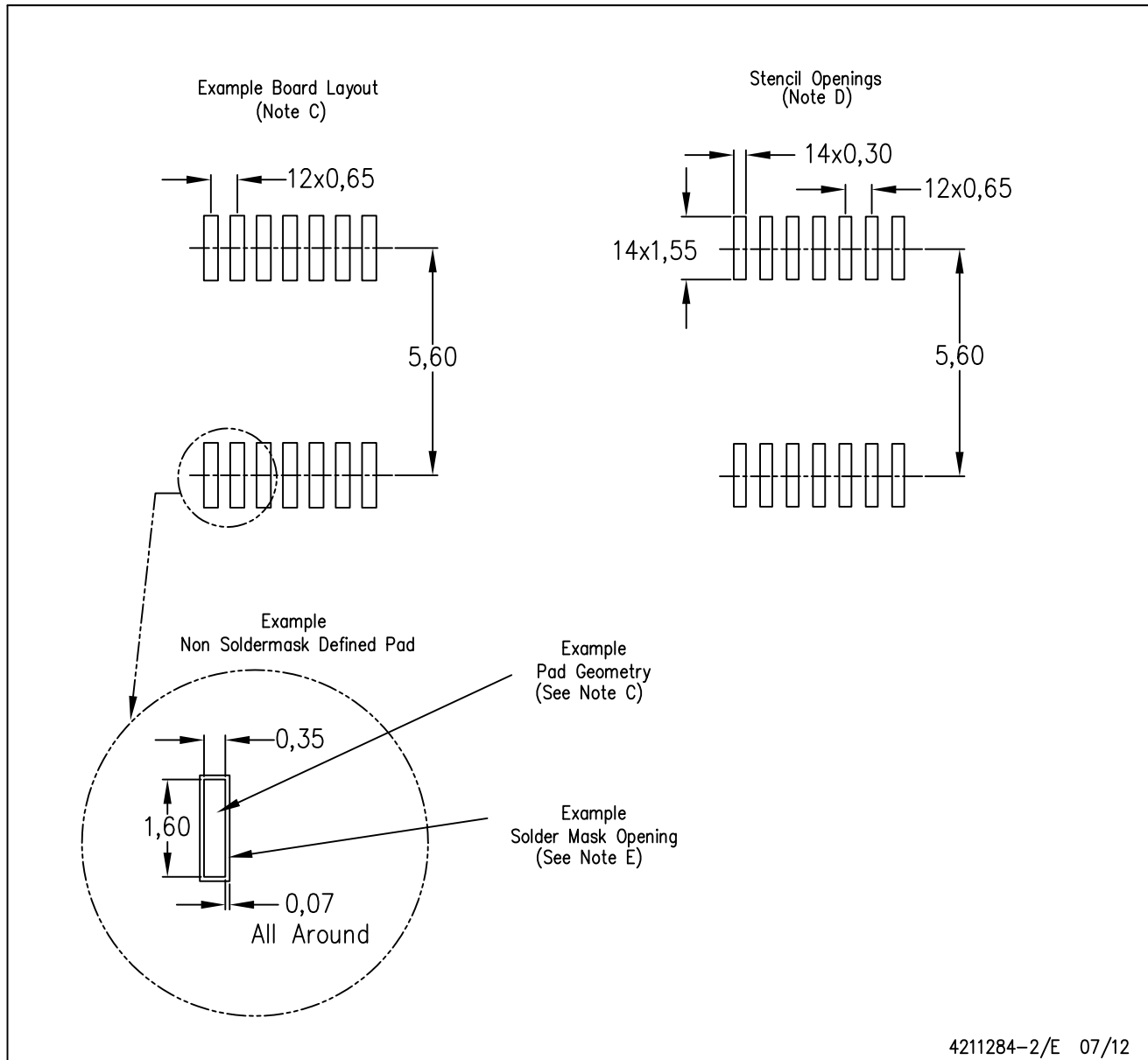
PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

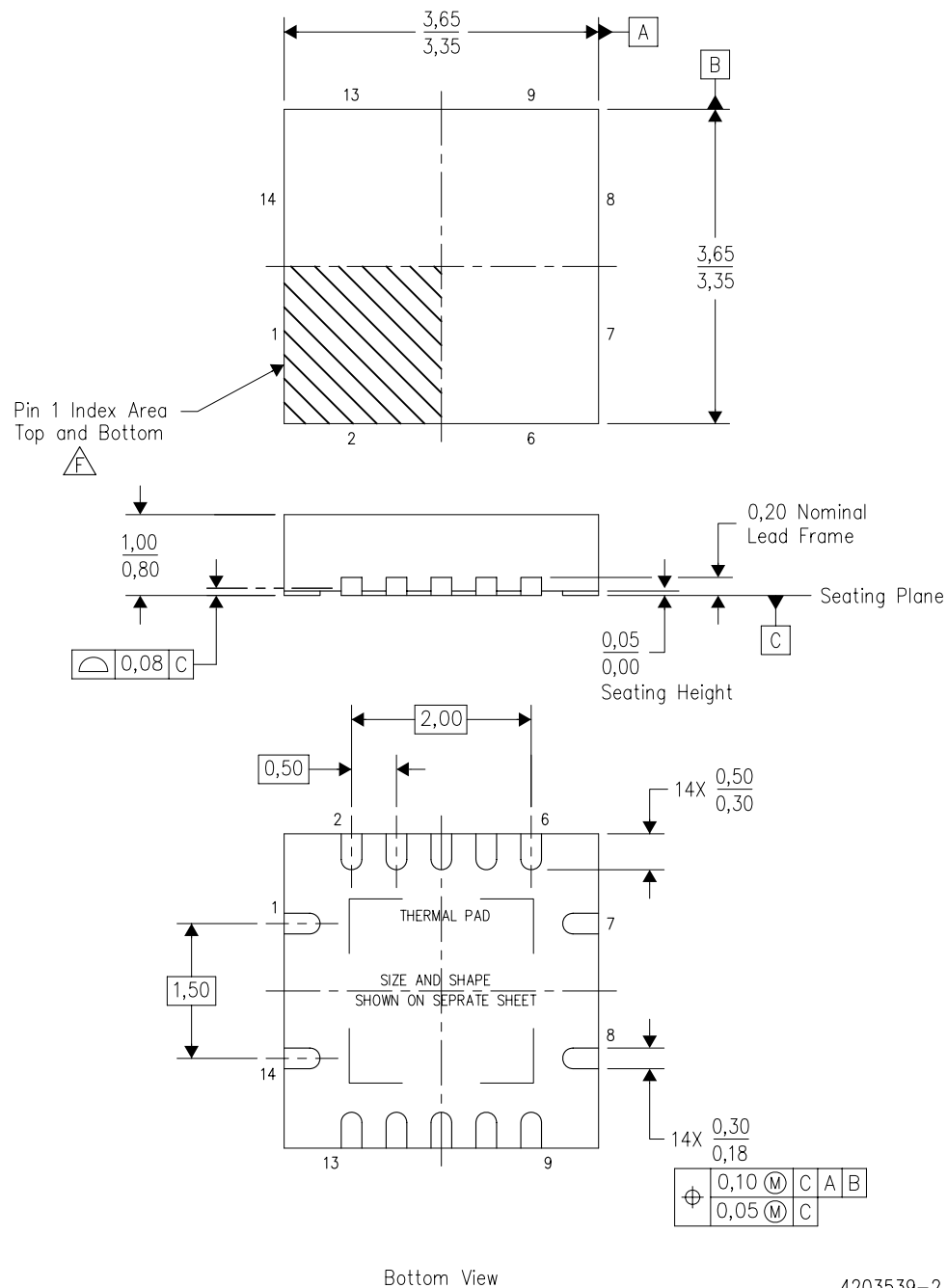
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

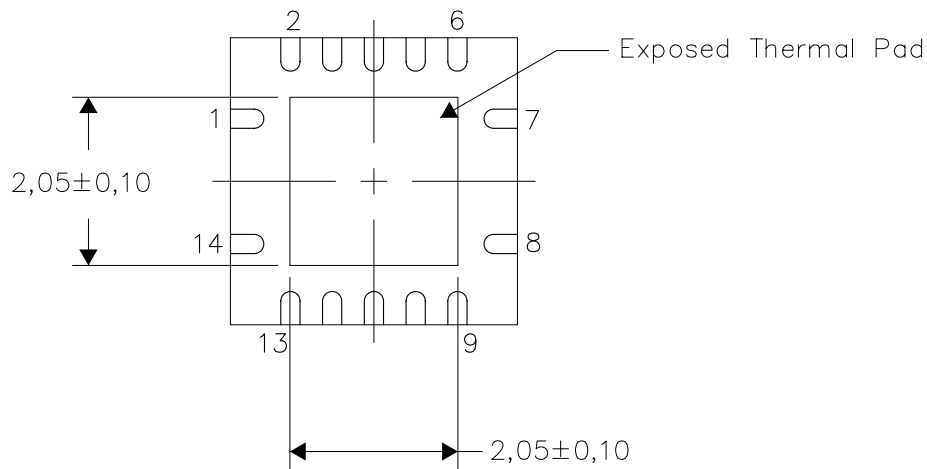
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

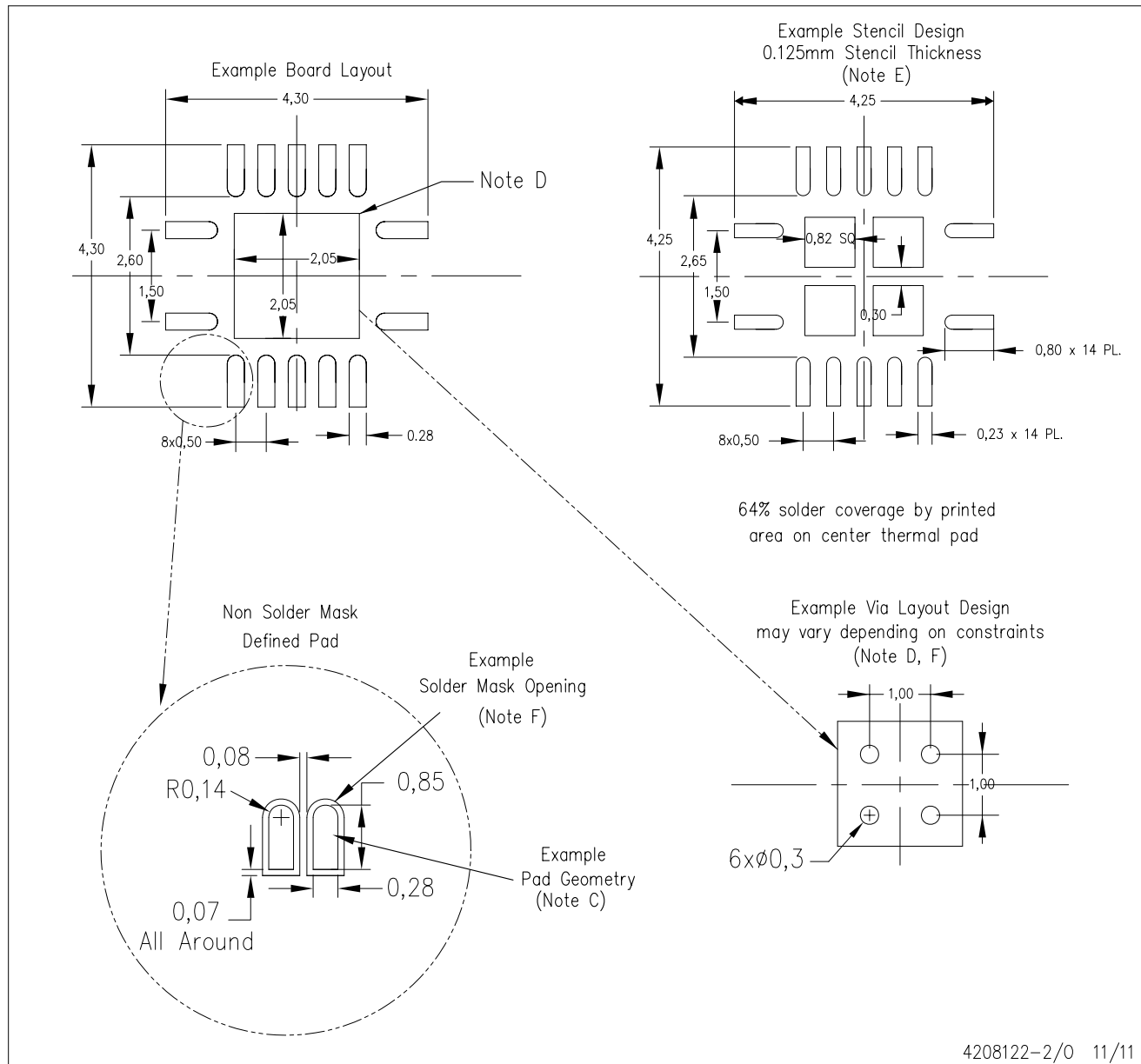
Exposed Thermal Pad Dimensions

4206353-2/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

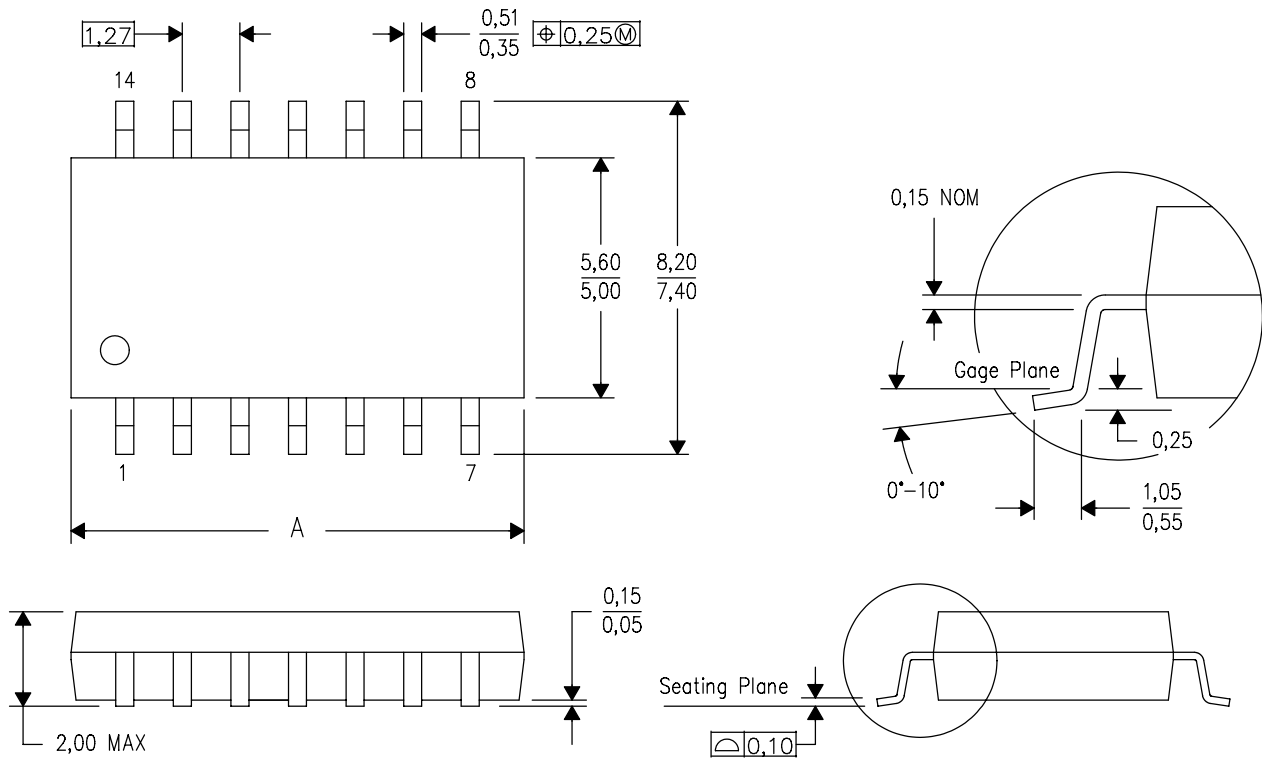


# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

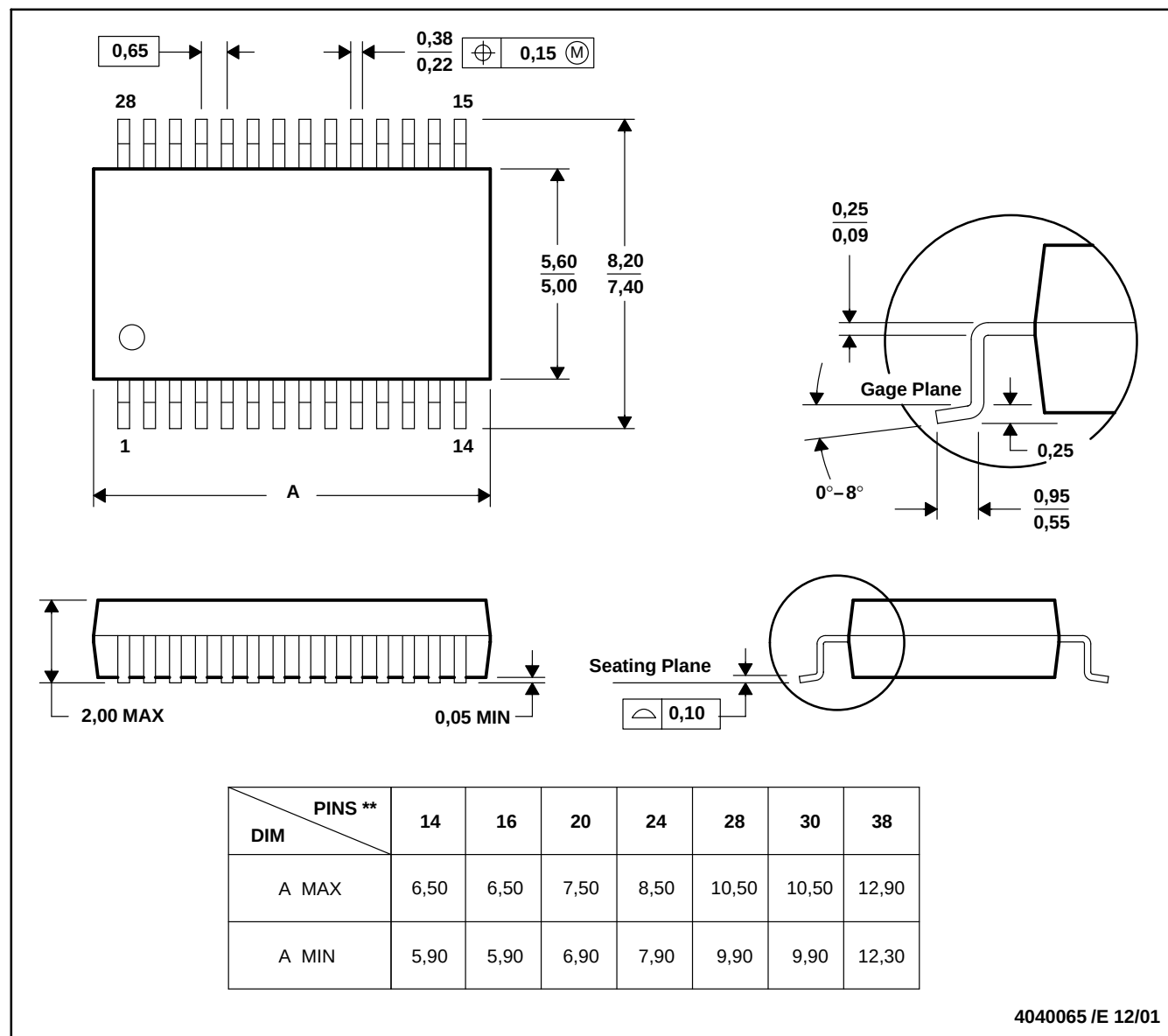
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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|                               |                                                                                          |
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