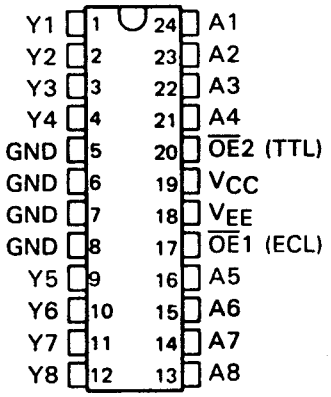
SN100KT5542, SN100KT5543
OCTAL TTL-TO-ECL TRANSLATORS WITH OUTPUT ENABLE

SDZS002A – D3134, AUGUST 1988 – REVISED JANUARY 1989

- **100K Compatible**
- **ECL and TTL Control Inputs**
- **P-N-P Inputs Reduce DC Loading**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC}, V_{EE} and GND Configurations to Minimize High-Speed Switching Noise**
- **ESD Protection Exceeds 2000 V, MIL-STD-883C Method 3015**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW, OR NT PACKAGE
(TOP VIEW)



description

These octal TTL-to-ECL translators are designed to provide an efficient translation function between a TTL signal environment to a 100K ECL signal environment. The designer has a choice of inverting ('5542) or true ('5543) outputs. Two pins, $\overline{OE}1$ and $\overline{OE}2$, are allowed for output enable control. These control inputs are ORed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment. The outputs, when disabled, go to a normal ECL logic low level.

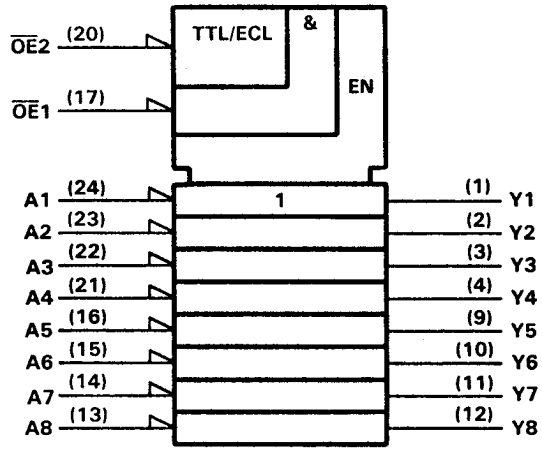
The SN100KT5542 and SN100KT5543 are characterized for operation from 0°C to 85°C.

FUNCTION TABLE

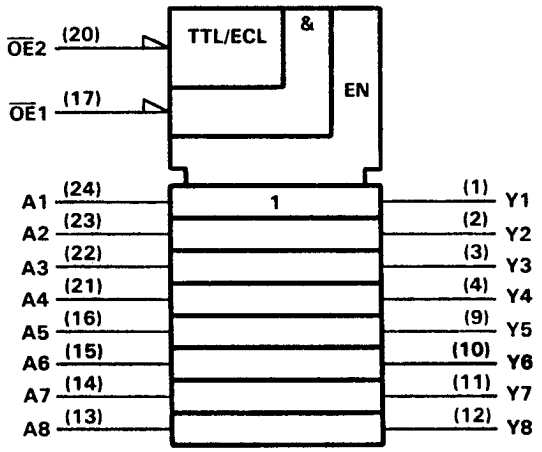
OUTPUT CONTROL		DATA INPUT	OUTPUT	
$\overline{OE}1$	$\overline{OE}2$	A	'5542	'5543
H	X	X	L	L
X	H	X	L	L
L	L	L	H	L
L	L	H	L	H

logic symbols†

SN100KT5542



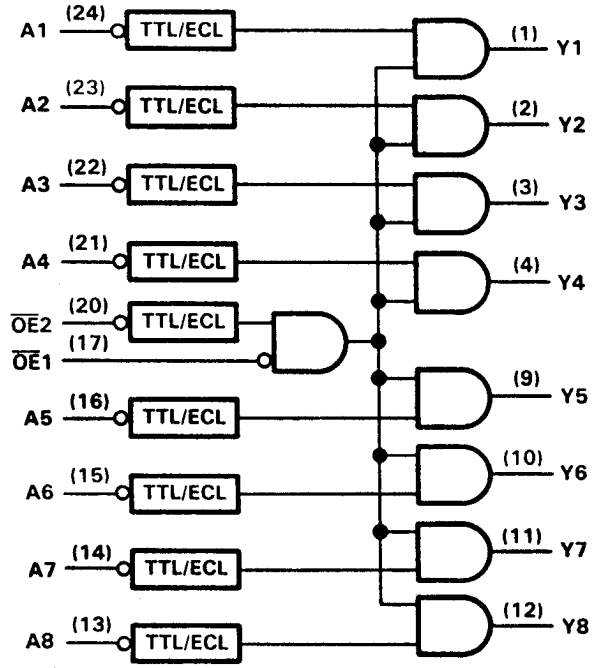
SN100KT5543



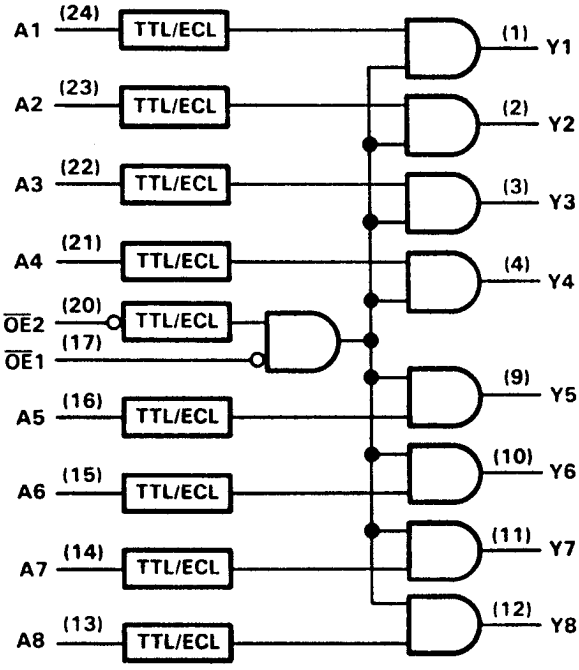
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN100KT5542



SN100KT5543



absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage, V_{EE} . . . . . −8 V to 0 V
Input voltage (TTL) (See Note 1) . . . . . −1.2 V to 7 V
Input voltage (ECL) . . . . . V_{EE} to 0 V
Input current (TTL) . . . . . −30 mA to 5 mA
Operating ambient temperature range . . . . . 0°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	TTL Supply voltage	4.5	5	5.5	V
V_{EE}	ECL Supply voltage	−4.2	−4.5	−4.8	V
V_{IH}	TTL High-level input voltage	2			V
V_{IL}	TTL Low-level input voltage			0.8	V
V_{IH}	ECL High-level input voltage‡	−1150		−840	mV
V_{IL}	ECL Low-level input voltage‡	−1810		−1490	mV
I_{IK}	TTL Input clamp current			−18	mA
T_A	Operating ambient temperature (see Note 3)	0		85	°C

‡The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

NOTES: 2. If unused, $\overline{OE}1$ should be tied directly to −2 V.
3. Each 100KT series circuit has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 3)

		PARAMETER	MIN	TYP†	MAX	UNIT
V_{IK}	A inputs and $\overline{OE}2$	V_{CC} = 4.5 V, V_{EE} = −4.2 V, I_I = −18 mA			−1.2	V
I_I	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = 7 V			0.1	mA
I_{IH}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = 2.7 V			20	μA
I_{IL}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = 0.5 V			−0.50	mA
I_{IH}	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = −840 mV			350	μA
I_{IL}	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = −1810 mV	0.50			μA
V_{OH}‡		V_{CC} = 4.5 V, V_{EE} = −4.5 V ± 0.3 V (see Note 4)	−1020		−840	mV
V_{OL}‡		V_{CC} = 4.5 V, V_{EE} = −4.5 V ± 0.3 V (see Note 4)	−1810		−1605	mV
I_{CCH}		V_{CC} = 5.5 V, V_{EE} = −4.8 V		14	22	mA
I_{CCL}		V_{CC} = 5.5 V, V_{EE} = −4.8 V		16	25	mA
I_{EE}		V_{CC} = 5.5 V, V_{EE} = −4.8 V		−67	−106	mA
C_i		V_{CC} = 5 V, V_{EE} = −4.5 V, F = 10 MHz		5		pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Figure 1 and Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.1	1.6	3.6	ns
t_{PHL}			0.1	1.4	3	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	0.8	2.7	4.6	ns
t_{PHL}			0.5	2.4	4.3	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	0.8	2.5	5.1	ns
t_{PHL}			0.7	2.3	4.3	
t_r		Y		1.5		ns
t_f				1.5		

†All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.
‡The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 3. Each 100KT series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.
4. Outputs are terminated through a 50-Ω resistor to −2 V.

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 3)

		PARAMETER	MIN	TYP†	MAX	UNIT
V_{IK}	A inputs and $\overline{OE}2$	V_{CC} = 4.5 V, V_{EE} = −4.2 V, I_I = −18 mA			−1.2	V
I_I	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = 7 V			0.1	mA
I_{IH}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = 2.7 V			20	μA
I_{IL}	A inputs and $\overline{OE}2$	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = 0.5 V			−0.50	mA
I_{IH}	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = −840 mV			350	μA
I_{IL}	$\overline{OE}1$ only	V_{CC} = 5.5 V, V_{EE} = −4.8 V, V_I = −1810 mV	0.50			μA
V_{OH}‡		V_{CC} = 4.5 V, V_{EE} = −4.5 V ± 0.3 V (see Note 4)	−1020		−840	mV
V_{OL}‡		V_{CC} = 4.5 V, V_{EE} = −4.5 V ± 0.3 V (see Note 4)	−1810		−1605	mV
I_{CCH}		V_{CC} = 5.5 V, V_{EE} = −4.8 V		17	25	mA
I_{CCL}		V_{CC} = 5.5 V, V_{EE} = −4.8 V		15	21	mA
I_{EE}		V_{CC} = 5.5 V, V_{EE} = −4.2 V		−72	−104	mA
C_i		V_{CC} = 5 V, V_{EE} = −4.5 V, F = 10 MHz		5		pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Figure 1 and Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	Any A	Y	0.1	1.3	3.2	ns
t_{PHL}			0.1	1.5	3.6	
t_{PLH}	$\overline{OE}1$ (ECL)	Y	0.5	2.1	4.4	ns
t_{PHL}			0.8	2.3	4.4	
t_{PLH}	$\overline{OE}2$ (TTL)	Y	0.6	2.2	4.5	ns
t_{PHL}			0.7	2.5	4.6	
t_r		Y		1.5		ns
t_f				1.5		

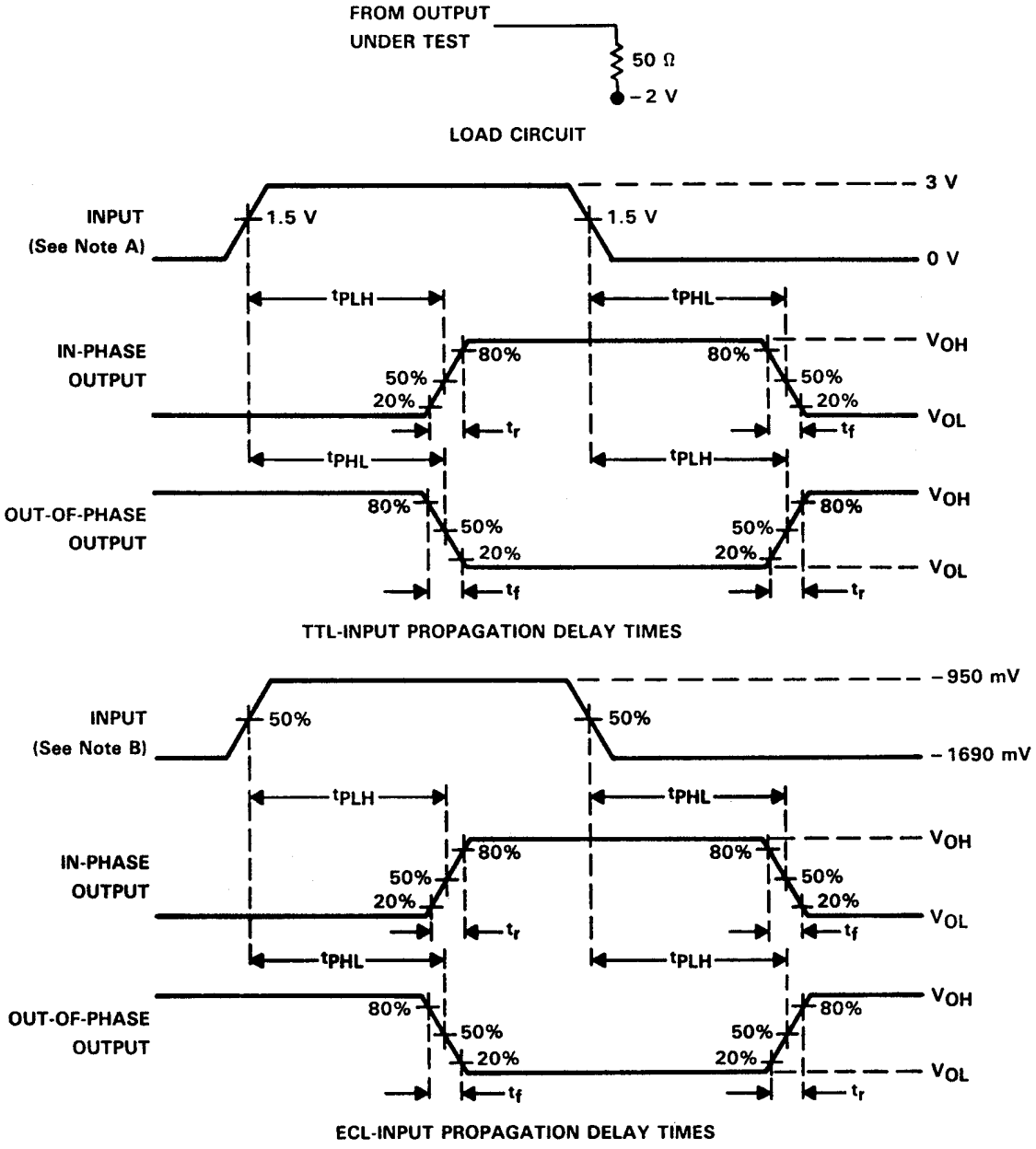
†All typical values are at V_{CC} = 5 V, V_{EE} = −4.5 V, T_A = 25°C.

‡The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 3. Each 100KT series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

4. Outputs are terminated through a 50-Ω resistor to −2 V.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
B. For ECL inputs, input pulses are supplied by generators having the following characterisitcs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 0.7 ns, t_f = 0.7 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN100KT5542DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN100KT5542NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN100KT5543DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN100KT5543NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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